CMOS current controlled fully balanced current conveyor*

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Abstract: This paper presents a current controlled fully balanced second-generation current conveyor circuit (CFBCCII). The proposed circuit has the traits of fully balanced architecture, and its X–Y terminals are current controllable. Based on the CFBCCII, two biquadratic universal filters are also proposed as its applications. The CFBCCII circuits and the two filters were fabricated with chartered 0.35-μm CMOS technology; with ±1.65 V power supply voltage, the total power consumption of the CFBCCII circuit is 3.6 mW. Comparisons between measured and HSpice simulation results are also given.

Key words: current mode circuits; fully balanced; differential; second-generation current conveyor; filters
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1. Introduction

As current-mode active devices, second generation current conveyors (CCIIs) are versatile building blocks for a variety of circuits[1–6]. Many modifications[7–11] have been introduced to increase the versatility of the CCII element. Differential difference current conveyors (DDCCs)[7], differential voltage current conveyors (DVCCs)[8], and fully differential second generation current conveyors (FDCCIIs)[9] are a few examples of these elements. In modern VLSI applications, balanced-mode structures are increasingly used. This is because non-ideal signals are generated in A/D mixed-mode circuits, and digital sections are the most serious source of noise due to clock feedthrough and charge injection. Moreover, in a balanced circuit, the output common-mode signal is kept constant, and it is entirely independent of the input signal. Therefore, performance of the circuit, such as dynamic range, noise restraining, and harmonic distortion can be greatly improved. A typical example of a balanced circuit, presented by Alzaher[10], is a fully balanced second generation current conveyor (FBCCII), which has a great effect on restraining the common-mode signals.

In a conventional CCII and also in its modifications there is a relatively significant voltage tracking error from terminal Y to terminal X because of the parasitic resistor in terminal X, which leads to transfer function errors in the application circuits. Moreover, these elements lack electronic programmability which is a key feature in recent applications. In 2006, Minaei proposed a new electronically tunable CCII (ECCII)[12] which employed continuous tuning between X and Z terminals. However, voltage tracking errors still exist in the circuit. In 1996, Fabre[13] proposed a current controlled current conveyor (CCCII) constructed by a bipolar translinear loop; by introducing an intrinsic resistor, this circuit could rectify the transfer error between X and Y terminals, and at the same time, the intrinsic resistor in the X terminal could be adjusted by the bias current. However, it has a crucial disadvantage of having only one high input voltage terminal, and when differential or floating signals are to be handled, this disadvantage becomes evident.

In 2007, Wang presented a differential current controlled CCII with multiple outputs (MO-DCCCII)[14]. In this circuit, the voltage relationship between the differential input Y and the terminal X can be tuned by the extra bias current, and the transconductance linear loop is composed of four bipolar transistors. This circuit has advantages of low noise and high operating frequency, but the proposed structure is not compatible with CMOS VLSI technology. The CMOS differential current-controlled CCII proposed in Ref. [15] can be integrated conveniently as it is totally composed of CMOS transistors. However, there is a fabrication limitation in the CMOS translinear circuit and its practical applications are rather restricted. In addition, neither of the two circuits[14, 15] is fully balanced, as the X terminals of the circuits are single-ended.

In this paper, a CMOS current controlled fully balanced second-generation current conveyor (CFBCCII) circuit is proposed. This circuit has continuous current tuning possibilities of its port characteristics, in addition to the merits of FBCCII. Consequently, its application circuits are electronically adjustable.

2. CFBCCII circuit realization

2.1. Circuit symbol and port characteristics

The circuit symbol of CFBCCII is shown in Fig. 1. It exhibits high input resistance at the Y terminals. Y_1, Y_2, Y_3, and Y_4 are the two pairs of differential input terminals. X_+ and X_- behave as voltage tracking terminals, and the current at the Z port is a replica of the current at the X port. Here, plus and minus signs denote the directions of currents in the Z port. I_B is the bias current of CFBCCII. The CFBCCII is represented

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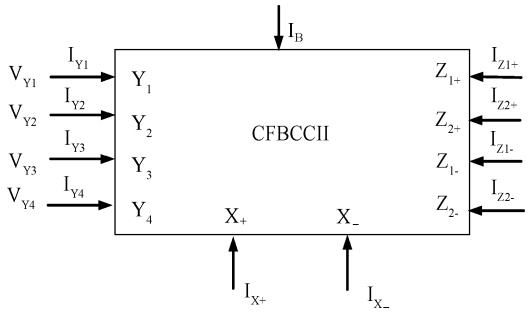

Fig. 1. Symbol of CFBCCII.

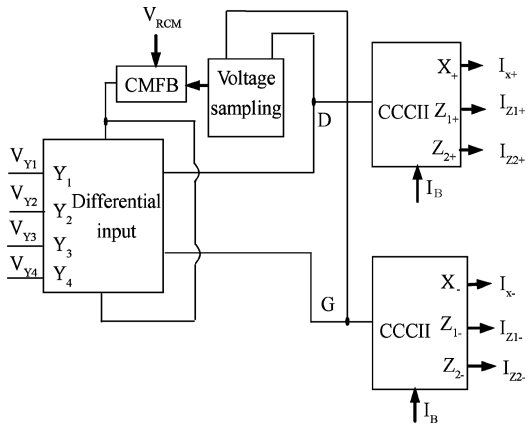

Fig. 2. Frame diagram of CFBCCII.

mathematically by

$$\begin{cases} I_{Y1} = I_{Y2} = I_{Y3} = I_{Y4} = 0, \\ V_{X+} - V_{X-} = (V_{Y1} - V_{Y2}) + (V_{Y3} - V_{Y4}) + (I_{X+} - I_{X-})R_X, \\ I_{Z+} - I_{Z-} = I_{X+} - I_{X-}. \end{cases} \tag{1}$$

$R_X = f(I_B)$ denotes the current controlled resistance which can be tuned by I_B. A circuit frame diagram of the CFBCCII is given in Fig. 2. The circuit is made up of four stages: differential voltage input stage, current controlled current conveyor, voltage-sampling circuit, and common-mode feedback circuit (CMFB). The feedforward path consists of a differential input stage and two CCCIIs. Input voltage signals are added to the differential input stage, and their voltage differences are transferred to points D and G. Current controlled current conveyors are employed to transfer V_D and V_G to the output terminals. The feedback path consists of a voltage sampling circuit and a CMFB circuit. The voltages of points D and G will be sampled in the voltage sampling module, where the common-mode (CM) voltage is generated. The CMFB circuit is employed to restrain the CM signals; by comparing V_m and V_{RCM}, V_m is forced to follow $V_m = V_{RCM}$. In this way, the CM signal can be effectively suppressed.

2.2. CFBCCII circuit configuration

The proposed CMOS fully balanced current controlled current conveyor circuit is depicted in Fig. 3. Transistors M1–M6 constitute three pairs of differential inputs. The input voltages are applied to the circuit by the gates of the MOS transistors, so $I_{Y1} = I_{Y2} = I_{Y3} = I_{Y4} = 0$. Following the analysis in Ref. [18], the following equations can be obtained: $I_{M1} = I_{M3} = I_{M5}$, $I_{M2} = I_{M4} = I_{M6}$. Assuming that all transistors operate in their saturation region, and channel-length modulation effects are not taken into consideration, the relationship between the drain current I_M of the transistor and the gate-source voltage is given by $I_M = (K'W/2L)(V_{GS} - V_T)^2$, where K' is the transconductance parameter, W and L are the width and length of the drain channel respectively, and V_T is the threshold voltage. When the channel dimensions of M1–M6 satisfy the following equations: $W_1/L_1 = W_3/4L_3 = W_5/4L_5$, $W_2/L_2 = W_4/4L_4 = W_6/4L_6$, it can be obtained that: $(V_{GS1} + V_T)/2 = V_{GS3} = V_{GS5}$, $(V_{GS2} + V_T)/2 = V_{GS4} = V_{GS6}$. According to the circuit shown in Fig. 3, one can obtain: $(V_{Y1} - V_A + V_T)/2 = V_D - V_B = V_{Y4} - V_C$, $(V_{Y2} - V_A + V_T)/2 = V_{Y3} - V_B = V_G - V_C$. Then the expressions for V_D and V_G become $V_D = V_{Y3} + (V_{Y1} - V_{Y2})/2$, $V_G = V_{Y4} - (V_{Y1} - V_{Y2})/2$.

Considering that the CCCII circuit proposed by Fabre[13] is not compatible for VLSI integration and the circuit in Ref. [16] has a fabrication limitation[17], in this paper, the CCCII proposed by Wang is used to make up the circuit[17]. In Fig. 3, M29–M36 and M44–M51 respectively constitute two translinear loops, M29–M36 transfer the voltage from point D to X_+ and M44–M51 transfer the voltage from point G to X_-. Now consider the translinear loop of M29–M36, following the analysis in Ref. [17], when the channel aspect ratios W/L of the NMOS transistors and PMOS transistors are identical, the voltage-current relationships are $I_X = \left(2\sqrt{2K_{eff}I_B}\right)V_{XY} = R^{-1}V_{XY}$, $R_X = (2\sqrt{2K_{eff}I_B})^{-1}$. R_X denotes the equivalent resistance of port X which is inversely proportional to the square root of bias current I_B. The voltages at points D and G are transferred to X_+ and X_-, so the relationships can be written as: $V_{X+} = V_{Y3} + (V_{Y1} - V_{Y2})/2 + I_{X+}R_X$, $V_{X-} = V_{Y4} - (V_{Y1} - V_{Y2})/2 + I_{X-}R_X$. So the differential voltage at port X can be obtained as

$$V_{X+} - V_{X-} = (V_{Y1} - V_{Y2}) + (V_{Y3} - V_{Y4}) + (I_{X+} - I_{X-})R_X. \tag{2}$$

M37–M39, M40–M42, M53–M55, and M56–M58 form four current mirrors, then $I_{Z1+} = I_{Z2+} = I_{X+}$, $I_{Z1-} = I_{Z2-} = I_{X-}$, so $I_{Z+} - I_{Z-} = I_{X+} - I_{X-}$. From the aforementioned analysis, it is clear that the proposed CFBCCII satisfies the characteristics shown in Eq. (1).

In the fully balanced system, it is necessary to include a common mode feedback circuit to prevent drifting of the common mode output. In Fig. 3, the common mode feedback circuit consists of Mc1–Mc8 in addition to two resistors (R) and two capacitors (C). The operation of the CMFB circuit is explained in Ref. [10] in detail.

3. Applications

3.1. Universal filter based on a single CFBCCII

From the wealth of knowledge on RC active filters, it is known that it is possible to design filter biquads using a single active element, two resistors and two capacitors. Such filters are known as the minimum component count circuits. By virtue of the characteristics of the CFBCCII, the filter depicted in Fig. 4 does not need any resistors, so the proposed filter is only composed of a single CFBCCII and two capacitors. This

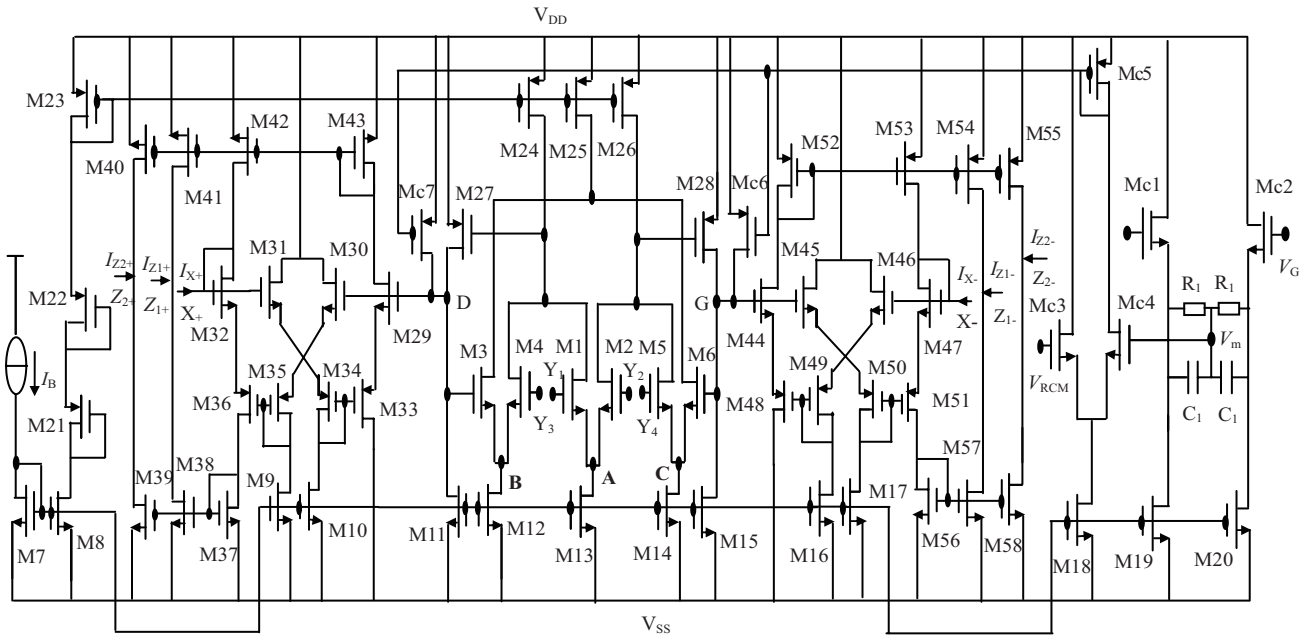

Fig. 3. The realization of the CFBCCII circuit.

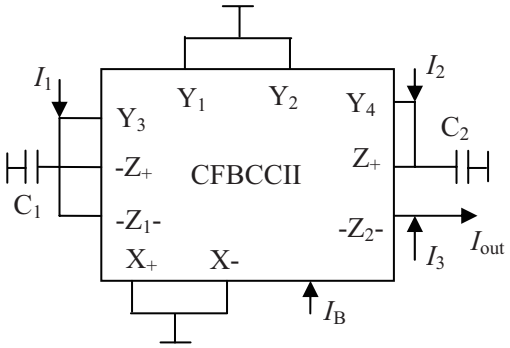

Fig. 4. Universal filter based on a single CFBCCII.

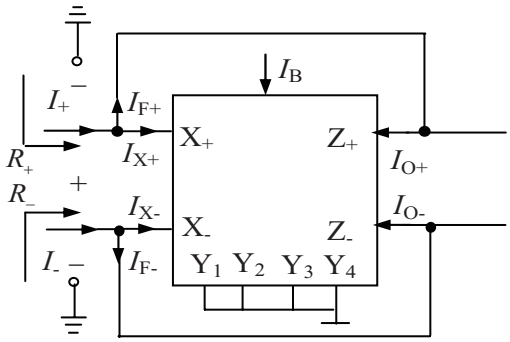

Fig. 5. CFBCCII based resistor.

circuit has the advantages of lower cost and power dissipation. As the figure shows, there are several extended terminals: $-Z_+$, $-Z_{1-}$, and $-Z_{2-}$, the current relationship is: $I_{-Z+} = -I_{X+}$, $I_{-Z1-} = I_{-Z2-} = -I_{X-}$. Circuit analysis yields the following filter transfer functions:

$$I_{\text{out}} = \frac{I_3 s^2 R_X^2 C_1 C_2 + I_3 s R_X C_2 - I_2 s R_X C_1 + I_3 - I_1 - I_2}{s^2 R_X^2 C_1 C_2 + s R_X C_2 + 1}. \quad (3)$$

Numerous filtering functions can be obtained depending on the status of the input current. Table 1 shows the five statuses of the proposed filter. The ω_0 and Q values of the filter are given by $\omega_0 = \frac{1}{R_X}\sqrt{\frac{1}{C_1 C_2}}$, $Q = \sqrt{\frac{C_1}{C_2}}$. It is clear that ω_0 and Q are orthogonally adjustable.

3.2. Current-controlled second-order universal filter

A CFBCCII based current controlled differential filter is proposed shown in Fig. 6. This circuit employs only three CFBCCIIs and two capacitors. The third CFBCCII is configured as two active resistors, whose configuration is shown in Fig. 5, and its resistance is equal to $R_+ = R_- = \frac{1}{2}R_X = \frac{1}{2}(2\sqrt{2K_{\text{eff}} I_B})^{-1}$. Circuit analysis yields the following filter transfer functions:

$$I_{O1+} - I_{O1-} = \frac{2(I_{1+} - I_{1-}) + sC_1 R_{X3}(I_{2+} - I_{2-})}{2s^2 C_1 C_2 R_{X1} R_{X2} + sC_1 R_{X3} + 2}, \quad (4)$$

$$I_{O2+} - I_{O2-} = \frac{2sC_2 R_{X2}(I_{1+} - I_{1-}) + s^2 C_1 C_2 R_{X3} R_{X2}(I_{2+} - I_{2-})}{2s^2 C_1 C_2 R_{X1} R_{X2} + sC_1 R_{X3} + 2}. \quad (5)$$

According to the two equations above, the transfer functions of the filter can be obtained. Table 2 shows the three statuses of the filter.

So the quality factor and the natural frequency ω of the filter can be written as $\omega = \sqrt{\frac{1}{R_{X1} R_{X2} C_1 C_2}}$, $Q = \frac{2}{R_{X3}}\sqrt{\frac{R_{X1} R_{X2} C_2}{C_1}}$.

From the above expressions, it is clear that the natural frequency ω and the quality factor can be orthogonally tuned by varying the bias current of the CFBCCII.

4. Simulation and measurement results

The CFBCCII circuit, the single CFBCCII based filter, and the fully differential second-order filter based on three CFBCCIIs are fabricated in chartered 0.35-μm CMOS technology. A photomicrograph of these three blocks occupying an area of 2.41 × 1.05 mm^2 is shown in Fig. 7. The dimensions of the CFBCCII transistors are listed in Table 3. The supply voltages of the CFBCCII and the filter based on a single CFBCCII are ±1.65 V, while the supply voltage of the filter based

Table 1. Five statuses of the single CFBCCII based filter.

Type	Input status	Value of the capacitor	Transfer function
Low-pass	$I_1 = I_{in}, I_2 = I_3 = 0$		$\frac{I_{out}}{I_{in}} = -\frac{1}{s^2R_X^2C_1C_2 + sR_XC_2 + 1}$
Band-pass	$I_1 = -I_2 = I_{in}, I_3 = 0$	$C_1 = C_2 = C$	$\frac{I_{out}}{I_{in}} = \frac{sR_XC}{(sR_XC)^2 + sR_XC + 1}$
High-pass	$I_2 = I_3 = I_{in}, \quad I_1 = 0$	$C_1 = C_2 = C$	$\frac{I_{out}}{I_{in}} = \frac{(sR_XC)^2}{(sR_XC)^2 + sR_XC + 1}$
Band-reject	$-I_1 = I_2 = I_3 = I_{in}$	$C_1 = C_2 = C$	$\frac{I_{out}}{I_{in}} = \frac{(sR_XC)^2 + 1}{(sR_XC)^2 + sR_XC_2 + 1}$
All-pass	$-I_1 = I_2 = 2I_3 = 2I_{in}$	$C_1 = C_2 = C$	$\frac{I_{out}}{I_{in}} = \frac{(sR_XC)^2 - sR_XC + 1}{(sR_XC)^2 + sR_XC + 1}$

Table 2. Three statuses of the single CFBCCII based filter.

Type	Input status	Output status	Transfer function
Low-pass	$I_{1+} - I_{1-} = I_{in+} - I_{in-}, I_{2+} - I_{2-} = 0$	$I_{O1+} - I_{O1-}$	$\frac{2}{2s^2C_1C_2R_{X1}R_{X2} + sC_1R_{X3} + 2}$
Band-pass	$I_{2+} - I_{2-} = I_{in+} - I_{in-}, I_{1+} - I_{1-} = 0$	$I_{O1+} - I_{O1-}$	$\frac{sC_1R_{X3}}{2s^2C_1C_2R_{X1}R_{X2} + sC_1R_{X3} + 2}$
High-pass	$I_{2+} - I_{2-} = I_{in+} - I_{in-}, I_{1+} - I_{1-} = 0$	$I_{O2+} - I_{O2-}$	$\frac{R_{X3}}{2R_{X1}} \frac{2s^2C_1C_2R_{X1}R_{X2}}{2s^2C_1C_2R_{X1}R_{X2} + sC_1R_{X3} + 2}$

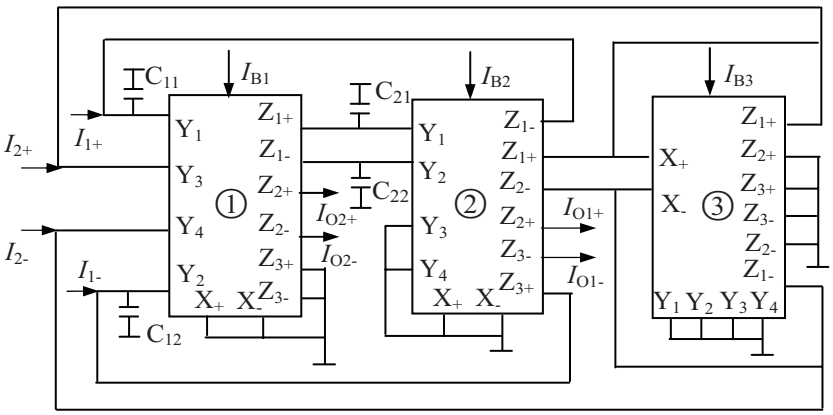

Fig. 6. CFBCCII based current controlled differential filter.

Table 3. Channel sizes of MOS transistors in the CFBCCII circuit.

MOS transistors	W/L (μm)	MOS transistors	W/L (μm)
M1, M2	2/0.35	M3–M6	8/0.35
M7–M17	16/0.35	M21–M22, M19–M20	10/0.35
M23–M26	14/0.35	M27, M28	20/0.35
M29–M32, M44–M47	10/0.35	M33–M36, M48–M51	40/0.35
M40–M43, M52–M55, M18	80/0.35	M37–M39, M56–M58	4/0.35
Mc1–Mc4	1/0.35	Mc5–Mc7	2/0.35

on three CFBCCIIs is ±1.8 V, and all the capacitors in the two filters are set to be 40 pF. The total power consumption of the CFBCCII circuit is 3.6 mW. To verify the performance of the three circuits, measurements are made on the chip. The measured relationship between R_x and

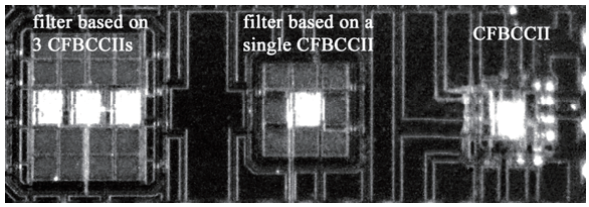

Fig. 7. Die photo of CFBCCII and CFBCCII filters.

I_B of the CFBCCII compared with the HSpice simulation result is displayed in Fig. 8. Terminals X_+, X_-, and terminals Z_{1+}, Z_{2+}, Z_{1-}, and Z_{2-} are all connected to grounded resistors of 1 kΩ. The curves represent R_X with three different values of I_B: 30, 40, and 55 μA. According to Eq. (2), the theoretical values of R_X would be 1.5, 1.3, and 1 kΩ respectively. Figure 9 illustrates the measured and simulated frequency response of the Z–X current. Both figures show that the measurement results are in accordance with the simulation results. It is seen that in the frequency range 0–40 MHz, the differential output current (I_{Z+}–I_{Z-}) is consistent

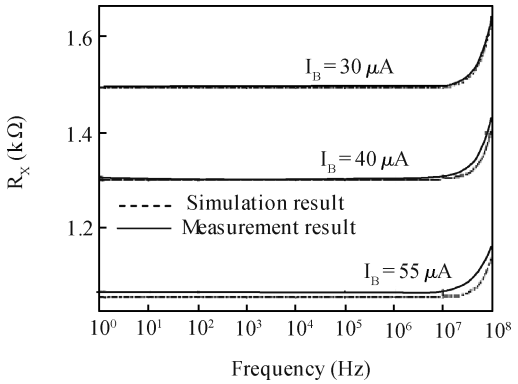

Fig. 8. Measured relationship between R_x and I_B.

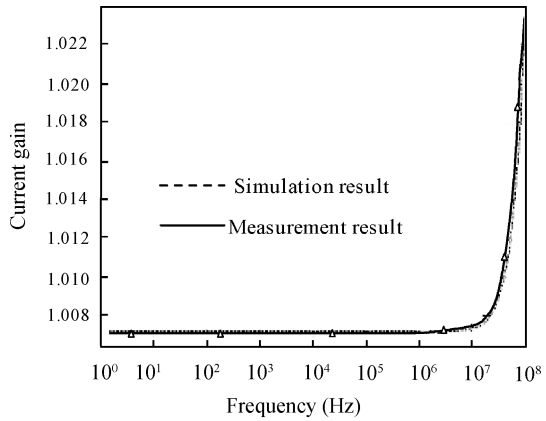

Fig. 9. Measured frequency response of Z-X current.

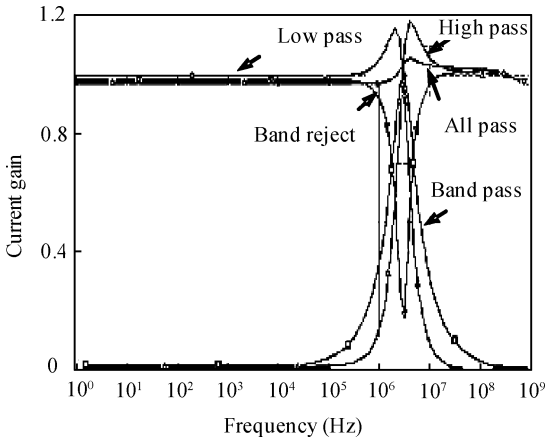

Fig. 10. Measured frequency response of the filter based on a single.

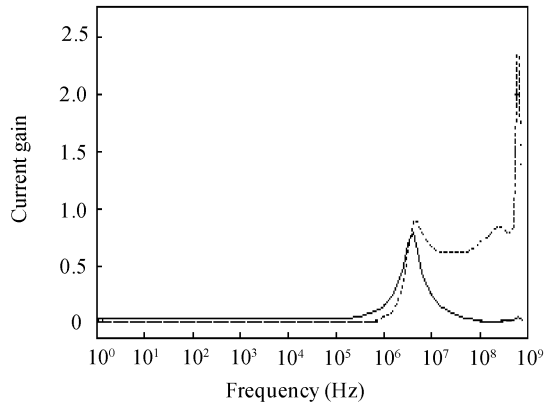

Fig. 11. Simulated frequency characteristics of BP and HP responses of the proposed filter.

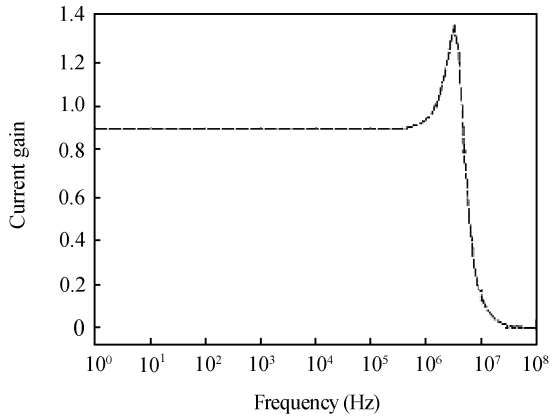

Fig. 12. Simulated frequency characteristic of the LP response of the proposed filter.

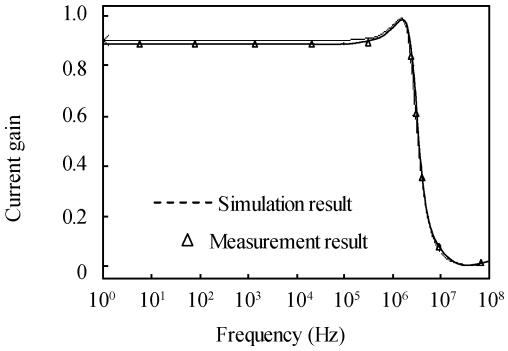

Fig. 13. Measured frequency characteristic of LP response of the filter based on a single CFBCCII.

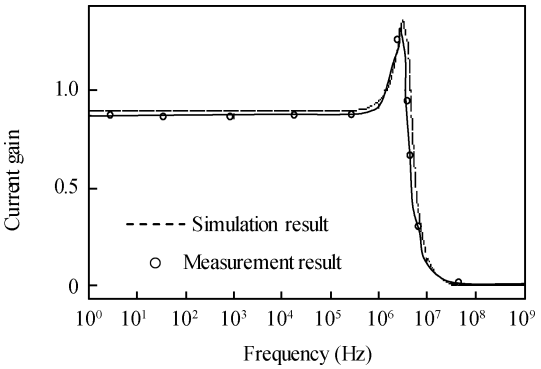

Fig. 14. Measured frequency characteristic of LP response of the filter based on three CFBCCIIs.

with the differential input current (I_{i+}–I_{i-}). Figures 10, 11 and 12 are the simulated ac frequency responses of the filtering responses of the two CFBCCII based filters. The ac frequency responses of these filters are also measured. For simplicity, only the low-pass filtering responses of the two filters are given. Figure 13 shows the measured frequency characteristic of the LP response of the filter based on a single CFBCCII, while Figure 14 gives a comparison of the simulated and measurement results of the filter based on three CFBCCIIs.

5. Conclusion

The design and implementation of a fully balanced current controlled current conveyor (CFBCCII) is presented. Its fully differential architecture and current controllability makes

this element more attractive in analog applications using modern VLSI technology. The CFBCCII realization is implemented in a 2.41×1.05 mm^2 CMOS chip, and its characteristics are experimentally verified in the lab. Application examples in designing CFBCCII based filters are also presented.

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