A fractional-*N* frequency synthesizer for WCDMA/Bluetooth/ZigBee applications*

Zhou Chunyuan(周春元)[1,†], Li Guolin(李国林)[2], Zhang Chun(张春)[1], Chi Baoyong(池保勇)[1], Li Dongmei(李冬梅)[2], and Wang Zhihua(王志华)[1]

(1 Institute of Microelectronics, Tsinghua University, Beijing 100084, China)

(2 Department of Electronic Engineering, Tsinghua University, Beijing 100084, China)

Abstract: A triple-mode fractional-*N* frequency synthesizer with a noise-filter voltage controlled oscillator (VCO) for WCDMA/Bluetooth/ZigBee applications has been implemented in 0.18-μm RF-CMOS technology. The proposed synthesizer achieves a good phase noise lower than –80 dBc/Hz in band and –115 dBc/Hz @ 1 MHz for the three modes, and only draws 21 mA from a 1.8 V supply. It has a high hardware sharing and a small size, only 1.5×1.4 mm^2. The system architecture, circuit design, and measured results are also presented.

Key words: multi-standard; PLL; frequency synthesizers; VCO
DOI: 10.1088/1674-4926/30/7/075008 **EEACC:** 1200; 1265B; 2570D

1. Introduction

With the spread of wireless applications, demands for radios, which can support multiple standards and multiple bands, are increasing rapidly these days. Obviously, we can use multiple sets of RF blocks to handle the bands we need; however, the number of components will increase and the chip size will be larger. One of the best ways to mitigate these issues is to design only one set of RF blocks to support multiple bands.

As one of the most important blocks in radios, frequency synthesizers are widely used to provide precise local oscillation. Multi-standard radios need multi-band frequency synthesizers. So, many researchers focus their attention on these synthesizers. For example, dual-mode and triple-band frequency synthesizers are proposed in papers[1, 2], respectively.

Because WCDMA is the 3rd generation standard, Bluetooth is important for short-distance transmission, and ZigBee has prospects in different areas in the near future; a triple-mode fractional-*N* frequency synthesizer for these applications is very useful. In this paper, the authors develop an architecture, which can enhance the hardware sharing and reduce the size of the chip. Starting from the next part, the system architecture, circuit design, as well as measured results will be shown.

2. Frequency plan and system architecture

In this section we will show how to plan the frequency range and which system architecture should be chosen for this synthesizer.

2.1. Frequency plan

The frequency ranges for WCDMA/Bluetooth/ZigBee applications are listed in Table 1. It can be seen that the range is from 1.9 to 2.5 GHz, which can be realized using only one VCO. With temperature and process variation considered, the VCO tuning range should be designed much larger with sufficient margin. Therefore, a digital and analog tuning technique has been adopted in this design, which will be illustrated in more detail in Section 3.

2.2. System architecture

As the channel spacing among these standards is different, fractional-*N* frequency synthesizers are better than integer ones and become one of the best solutions for multi-standard applications. The fractional-*N* frequency synthesizers also have the following advantages:

(1) Realizing high frequency resolution;

(2) Higher reference frequency used, avoiding higher division ratios;

(3) Bandwidth of the loop not limited by the channel spacing.

A 20 MHz reference frequency leads to division ratios ranging from 96 to 125. In this case, we can use the constant charge pump current and loop filter for the three modes without changing the bandwidth of the loop too much. So, all parts can be reused in this design. The hardware sharing in this work is higher than in the structure proposed in Ref. [1].

Table 1. Requirements of WCDMA/Bluetooth/ZigBee.

Standards	Frequency range (MHz)	Channel spacing (MHz)
WCDMA	2110–2170(RX)	5
	1920–1980(TX)	5
Bluetooth	2400–2478	1
ZigBee	2405–2480	5

* Project supported by the Beijing Municipal Science & Technology Development Program (No. D0305003040111) and the National Natural Science Foundation of China (No. 90407006).

† Corresponding author. Email: zhoucy06@mails.tsinghua.edu.cn

Received 16 January 2009, revised manuscript received 20 February 2009

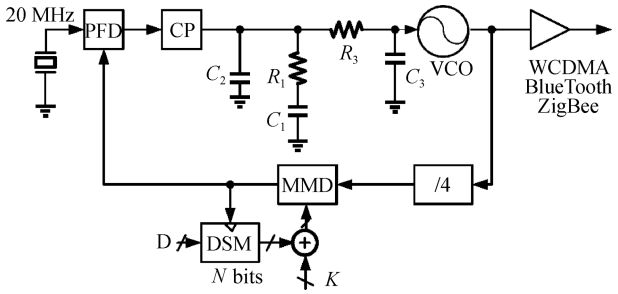

Fig. 1. Block diagram of proposed synthesizer.

To mitigate the working speed problem of multi-mode dividers (MMD), a divide-by-4 prescaler is added. Assuming the frequency of the VCO output signal is 2.4 GHz, then after the prescaler, the frequency is lower than 1 GHz, which is not high for a static divider. However, the phase noise caused by the modulator can increase $20\lg N_{\text{fix}}$ ($N_{\text{fix}} = 4$ in this design)[3] and may be higher than that caused by the VCO at high frequencies. That is why a MASH1-1-1-1, Δ–Σ modulator (DSM) is applied.

The structure block of the whole proposed triple-standard frequency synthesizer is shown in Fig. 1. Using verilog AMS, behavioral models have been built, and a top simulation has been done, which shows that the loop is stable and locks very well within the required settling time.

3. Circuit design

This section describes an LC VCO using an noise filter technique, which has a large tuning range and a low phase noise. It also describes, in general terms, some other blocks comprising the frequency synthesizer.

3.1. Wide range VCO with low phase noise

The VCO is one of the most significant blocks in the synthesizers. In this work, an LC-tuned VCO rather than a ring-VCO is preferred, as the former has a better phase noise performance. The schematic is shown in Fig. 2. It uses a PMOS as the tail current considering the lower flicker noise and less substrate noise pick-up. A cross-coupled PMOS transistor pair is added to form a negative resistance, which is equal to $-2/g_{\text{m}}$, where g_{m} is the transconductance of each transistor. We make sure that it is large enough to start and sustain oscillation during the design. In general, $2/g_{\text{m}}$ must be less than the resonator tank equivalent resistance to allow for some design margin[1].

Frequency covering is one of the most important specs in VCO design. In order to cover the whole frequency range of the three modes, a digital tuning technique is applied and the block is composed of 4-bit binary weighted capacitors and switches. When the switches are on, the capacitors are added to the tank. However, the resistors of the switches will decrease the Q-factor and worsen the phase noise. If the size of the switches is large enough, the resistance can be small and the effect can be neglected. But a large size means a large parasitic capacitance. These capacitors are in series with the binary weighted capacitors and cause the total capacitance not

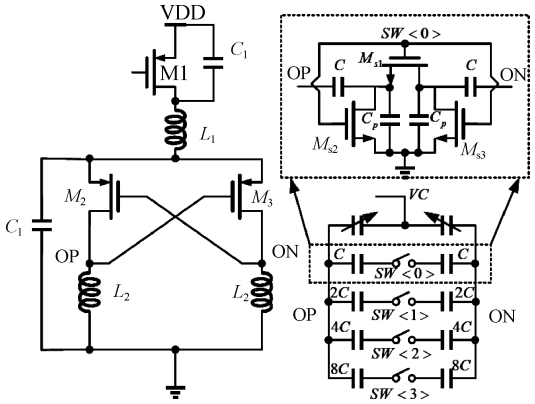

Fig. 2. Schematic of VCO with noise filter.

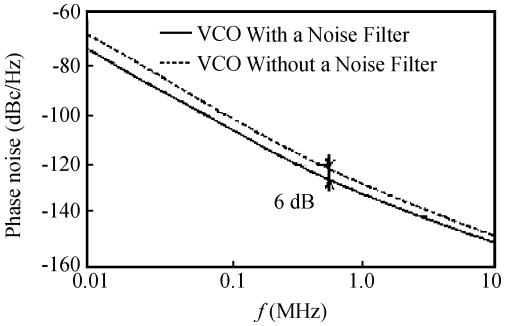

Fig. 3. Contrast of phase noise.

to be equal to zero when the switches are off. So, the size of the switches should be a trade off.

Another important spec of a VCO is the phase noise. According to the Leeson model, the phase noise can be expressed as

$$L(\Delta\omega) = 10\lg\left\{\frac{2FkT}{P_{\text{sig}}}\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left(1+\frac{\Delta\omega_{1/f^3}}{\Delta\omega}\right)\right\}, \quad (1)$$

where F is a factor to account for the increased noise in the $1/(\Delta\omega)^2$ region, ω_0 is the center frequency, $\Delta\omega$ is the frequency offset, and $\Delta\omega_{1/f^3}$ is the boundary between the $1/(\Delta\omega)^2$ and $1/(\Delta\omega)^3$ regions, which is precisely equal to the $1/f$ corner of the device noise.

From the model showed above, we can use an inductor with a high Q-factor to improve the phase noise. However, the Q-factor of the inductor on chip in this design is not high. So, a noise filter technique is applied to improve the phase noise, which is similar to the one presented in Ref. [4]. The schematic is shown in Fig. 2. A capacitance C_1 is added to shorten the noise frequency around $2\omega_0$ to ground. Inductor L_1 is put between the tail source and common sources of the cross-coupled pair. It is chosen to resonate at $2\omega_0$ in parallel with C_2, and provides a high impedance, which is limited only by the quality factor of the inductor L_1 at a narrow band frequency around $2\omega_0$. This noise filter composed of L_1 and C_1 stops the noise at $2\omega_0$, affecting the VCO phase noise. Based on the simulation, the phase noise is lower than –121 dBc/Hz at 600 kHz offset frequency from 2 GHz, which improves by 6 dB with a noise filter technique as show in Fig. 3.

The power consumption of the VCO is 16.2 mW, according to the figure of merit (FOM) definition of a VCO in Eq. (2)

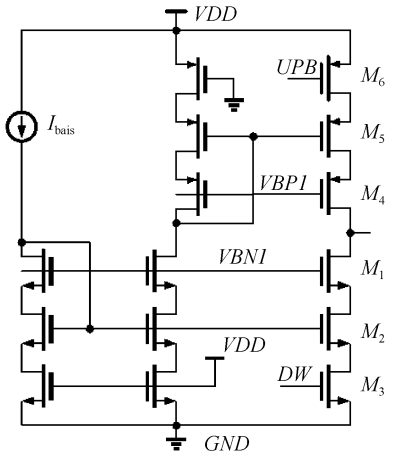

Fig. 4. Schematic of charge pump.

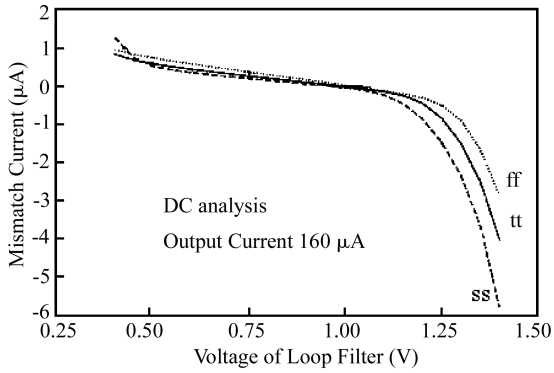

Fig. 5. Current mismatch of the proposed charge pump.

in Ref. [5]. The FOM of this VCO is equal to about –181. The data illustrates that the performance of this VCO is good.

$$\mathrm{FOM} = L(f_{\mathrm{m}}) + 10\lg\left[\left(\frac{f_{\mathrm{m}}}{f_0}\right)^2 P_{\mathrm{DC}}\right], \tag{2}$$

where $L(f_{\mathrm{m}})$ is the SSB phase noise measured at the offset frequency f_{m} from the oscillation frequency f_0, and P_{DC} is the DC power dissipation in mW.

3.2. Charge pump design

Charge pumps (CP) are also key blocks in the design of frequency synthesizers based on PLLs. Their function is to transform time information into current with a phase frequency detector (PFD). They actually operate in a discrete-time manner, which causes spectrum folding. This folding effect produces phase noise around offset frequencies of N-times the reference frequency $\omega_{\mathrm{ref}}(N = 1, 2, 3, \ldots)$. The reference spur is the phase noise around the offset frequency ω_{ref}.

As the current mismatch generates deterministic and periodic ripples of the VCO control voltage[6], a high performance charge pump with a cascode transistor added to improve the current mismatch and increase the output resistor is designed in this work. The schematic is shown in Fig. 4, where M1, M4 are the cascode transistors, M3, M6 are the switches, and M2, M5 are the current sources.

The simulation result is shown in Fig. 5. Considering the corners (ff, tt, ss), the current mismatch can be lower than 4% with a linear range of 0.4–1.4 V.

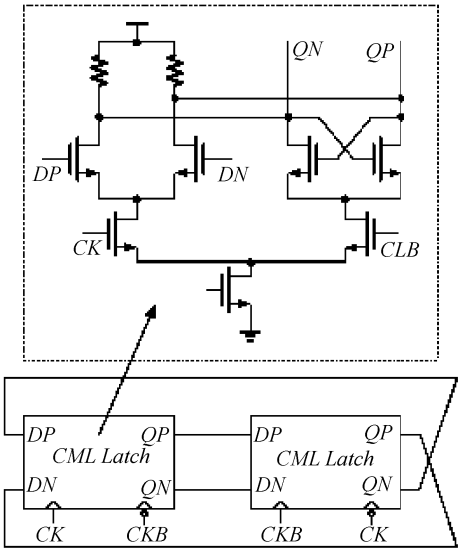

Fig.6. Divide-by-2 divider.

3.3. Prescaler, multi-mode divider, and DSM design

As the frequency of the VCO output signal can reach around 2.5 GHz, a higher speed divider must be chosen. The divider based on a true single-phase clocked register (TSPCR) can work at high speeds. However, a divider of this kind is sensitive to the amplitude of the signal. In general, the signal from a VCO buffer is not rail-to-rail. If a TSPCR divider is applied, it is probable that the divider cannot work well. So, in many papers, the authors use another kind of divider based on current mode logic (CML), such as in Ref. [7]. This structure can work with a small signal amplitude (high sensitivity), although it draws more current. In order to reduce the power, Reference [7] presented a current-reused method by combining two conventional level CML latches with a single current source and one pair of clock transistors. To simplify the design, we just use conventional CML dividers to form a divide-by-4 prescaler. From Fig. 6, it is easy to see that the divide-by-2 divider consists of two CML latches.

After the prescaler, a digital MMD follows, seen in Fig. 1. A simple way to realize a programmed divider is a train of divide-by-2/3 divider, which is similar to the one described in Ref. [8]. The minimum division ratio of an N-stage train is 2^N and the maximum ratio is $2^{N+1}-1$. According to the frequency range analysis in section 2, an MMD should realize a division ratio of 24–32; however, the ratio range must be larger if we consider the output levels of the Δ–Σ modulator. With the output levels of MASH1-1-1-1 from –7 to 8, the actual division ration is 17–40. It is hard to realize this ratio without any change of this 2/3 train structure. For example, using a 5-stage of the simple train, we get ratios of 32–63 (2^5 to 2^6-1). If the fifth stage is a 2/1 block not a 2/3 block, the division ratios are 16–47. The structure is shown in Fig. 7.

In order to realize a fractional division ratio, a delta-sigma modulator is added. With the stability and noise shaping considered, a four-order MASH1-1-1-1 is chosen. The structure is shown in Fig. 8. In this design, we chose D data with

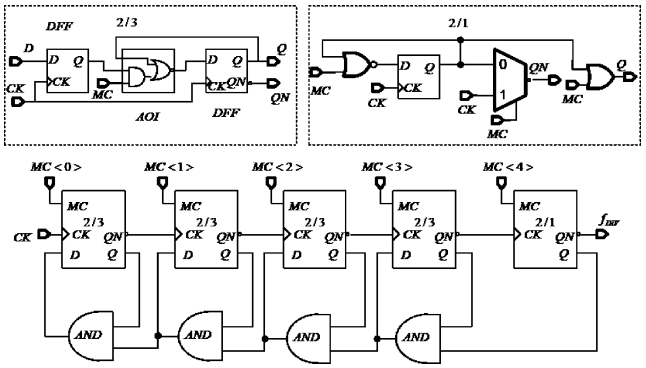

Fig. 7. MMD.

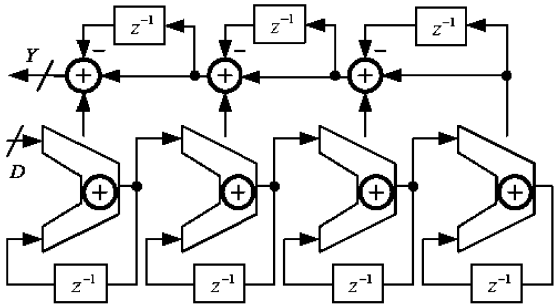

Fig. 8. MASH1-1-1-1.

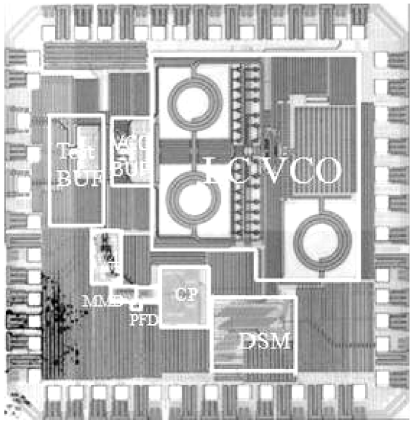

Fig. 9. Microphotograph of the proposed synthesizer.

24 bits and realize a frequency resolution up to 1.19 Hz.

4. Measured results

The proposed frequency synthesizer is implemented using 0.18 μm RF-CMOS process. The microphotograph of the die is shown in Fig. 9.

The frequency range of the free VCO (Fig. 10) is measured to be from 1.9200 to 2.57554 GHz which is enough for the applications.

The whole loop locks well and has a good phase noise performance when it is closed with a channel selection data. Figure 11 shows the measured phase noise at a frequency offset of 100 kHz–10 MHz from the center frequencies 2.314 and 2.031 GHz, respectively.

Based on the measured results above, the performance of the proposed synthesizer is listed in Table 2.

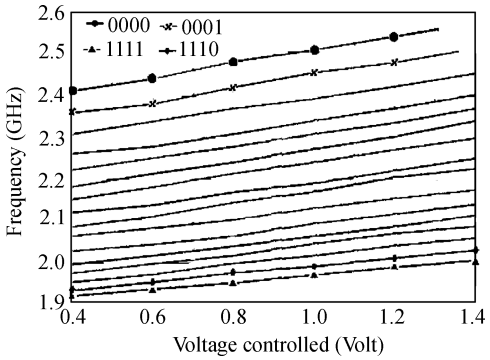

Fig. 10. Frequency range of the VCO.

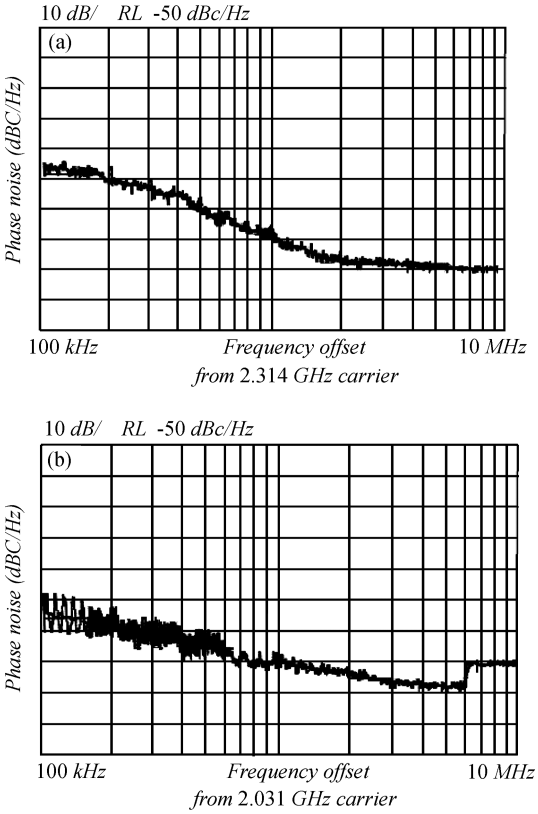

Fig. 11. Phase noise of the frequency synthesizer: (a) The loop locks at 2.314 GHz; (b) The loop locks at 2.031 GHz.

Table 2. Performance of the proposed synthesizer.

Parameter	Value
Frequency range	1.9200–2.5755 GHz
Frequency resolution	< 2 Hz
Integrated noise	3 degree
Phase noise @ 1 MHz	–120 dBc/Hz for WCDMA, –115 dBc/Hz for BlueTooth and ZigBee
Power	38 mW
Area	1.5×1.4 mm^2
Technology	0.18 μm RF-CMOS

5. Conclusions

In this paper, a triple-standard fractional-N frequency synthesizer for WCDMA/Bluetooth/ZigBee has been imple-

mented in 0.18-μm RF-CMOS technology. This frequency synthesizer has a low phase noise with a wide range. In the synthesizer, a high performance VCO with a noise filter and a low current mismatch charge pump is adopted. The measured results show that the frequency synthesizer proposed meets the demands of the three standards.

References

[1] Tang Y, Aktas A, Ismail M, et al. A fully integrated dual-mode frequency synthesizer for GSM and wideband CDMA in 0.5 μm CMOS. Circuits and System, 2001, 2: 14

[2] Wu P, He K. A CMOS triple-band fractional-*N* frequency synthesizer for GSM/GPRS/EDGE applications. ISCAS, 2001, 4: 70

[3] Perrott M H, Trott M D, Sodini C G. A modeling approach for Σ–Δ fractional-*N* frequency synthesizers allowing straightforward noise analysis. IEEE J Solid-State Circuits, 2002, 37(8): 1028

[4] Hegazi E, Abidi A A. A filtering technique to low LC oscillator phase noise. IEEE J Solid-State Circuits, 2001, 36(12): 1921

[5] Yun S J, Shin S B, Choi H C, et al. A 1 mW current-reuse CMOS differential LC-VCO with low phase noise. ISSCC, 2005, 1: 540

[6] Rhee W. Design of high-performance CMOS charge pump in phase-locked loops. ISCAS, 1999, 2: 545

[7] Usama M, Kwasniewski T A. A 40-GHz frequency divider in 90-nm CMOS technology. Circuits and Systems, 2006: 41

[8] Vaucher C S, Ferencic I, Locher M, et al. A family of low-power truly modular programmable dividers in standard 0.35-μm CMOS technology. IEEE J Solid-State Circuits, 2000, 35(7): 1039