Low-cost low-power UHF RFID tag with on-chip antenna

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Abstract: This paper presents an EPC Class 1 Generation 2 compatible tag with on-chip antenna implemented in the SMIC 0.18 μm standard CMOS process. The UHF tag chip includes an RF/analog front-end, a digital base-band, and a 640-bit EEPROM memory. The on-chip antenna is optimized based on a novel parasitic-aware model. The rectifier is optimized to achieve a power conversion efficiency up to 40% by applying a self-bias feedback and threshold compensation techniques. A good match between the tag circuits and the on-chip antenna is realized by adjusting the rectifier input impedance. Measurements show that the presented tag can achieve a communication range of 1 cm with 1 W reader output power using a 1×1 cm^2 single-turn loop reader antenna.

Key words: RFID; tag; on-chip antenna; rectifier; low-cost; low-power

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1. Introduction

The cost and size reduction of radio frequency identification (RFID) tags is one of the keys to the wide adoption of RFID systems. A revolutionary method of low-cost small-size tag fabrication is to use an on-chip antenna (OCA). Integrating an OCA with RFID tags has significant advantages not only in saving a major portion of the tag assembly cost but also in enhancing the system reliability and allowing small tags to be applied in various applications, especially item-level tagging (ILT). There have been several publications on RFID tags with an OCA embedded[1−4]. However, many existing OCA implementations need extra procedures in addition to the standard fabrication process, such as gold plating[2] and thick oxide[3]. Also their communication ranges are short, e.g. 4 mm[4]. In this work, an optimized OCA design is achieved based on a novel model, which takes fabrication process parasitics into account.

Power consumption is vital to the successful integration of an OCA with passive tags, because of the extremely weak input power received by an OCA. In recent years, various optimization methods have been introduced to reduce the tag power consumption[5, 6]. However, the prevalent method of energy harvesting still employs the conventional Dickson AC–DC charge pump. In order to increase the power conversion efficiency (PCE) of a Dickson charge pump, expensive fabrication processes with low-threshold MOSFETs or Schottky diodes were widely used. In this work, a high efficiency rectifier made using a standard CMOS process is proposed. It exploits self-bias feedback and threshold compensation techniques to reduce the energy wasted during rectification, thereby greatly improving the tag communication range.

2. System architecture

The proposed tag architecture is illustrated in Fig. 1. A high efficiency rectifier harvests energy from the interrogating RF field to supply the whole system. A low voltage PTAT circuit generates voltage and current references. The system clock (Clk) is generated by a current controlled ring oscillator. A power-on-reset (Por) signal turns high when the supply voltage (V_{dd}) reaches the threshold for proper operation. The reader-to-tag (R–T) data are demodulated from the envelope of the carrier. The modulation of the tag-to-reader (T–R) data is achieved by changing the tag input impedance according to the FM0 coded signal from the digital base-band. An energy storage capacitor C_s is employed to supply the tag chip during the interrogating energy gap.

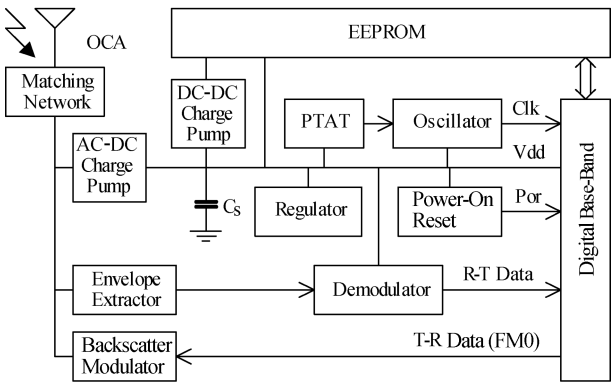

Fig. 1. Tag system architecture.

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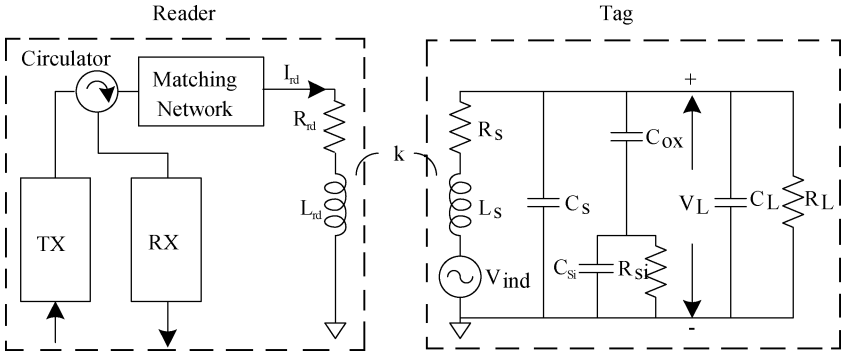

Fig. 2. Power link model incorporated with the OCA model.

3. On-chip antenna

3.1. On-chip antenna modeling

An OCA can be regarded as being immersed in the oxide layer. The guided wavelength in the oxide, which is 16.7 cm at 900 MHz and far larger than the normal chip size, which is on the order of mm, has the largest influence on the OCA. As a result, an electrically-small loop antenna is a good and maybe the only choice for an OCA operating in the UHF band.

In order to co-design the OCA with tag circuits, it is necessary to establish an OCA model. The conventional loop antenna model is fairly simple, and includes L_s and R_s, as shown in Fig. 2. However, this model cannot be applied to the OCA directly because of the lossy nature of the standard CMOS substrate. By analogy with on-chip spiral inductors, a single-ended single-π model is used as shown in Fig. 2, where a shunt branch composed of C_{ox}, R_{si}, and C_{si} accounts for the parasitic effects of the stacked oxide and substrate. Additionally C_s models the overlap between the loop and the underpass, together with the crosstalk between adjacent turns. The parasitic elements C_{ox}, R_{si}, C_{si}, and C_s can be extracted by curve-fitting with the simulation or measurement results.

3.2. Power link modeling

Due to the electrically-small feature, the radiation resistance of the OCA is quite small. Therefore, an effective far field radiation cannot be achieved here and the wireless transmission is confined within the near field of the OCA, which is on the order of cm in the UHF band.

In order to achieve the best performance for such an OCA, the electrically-large reader antenna, like the popular microstrip patch antenna, is replaced by one electrically-small loop antenna on the PCB board, which is modeled by L_{rd} and R_{rd} in Fig. 2[7]. As a result, a near field communication link is formed, which takes advantage of the near field magnetic coupling and can be modeled as a loosely coupled transformer. The key parameter to characterize the magnetic coupling is the coupling factor k, which is a function of the geometry of both the reader antenna and the OCA, together with their separation distance. The coupling factor can be calculated by the Biot–Savart law or simulated by an electromagnetic simulator, like HFSS. Then the induced voltage upon the OCA, V_{ind}, can be calculated as

$$V_{ind} = \omega k I_{rd} \sqrt{L_{rd} L_s}, \tag{1}$$

where ω is the angular frequency, and I_{rd} is the current flowing through the reader loop antenna. Here, the OCA is regarded as a voltage source, while other tag circuits as its load are modeled by C_L and R_L in Fig. 2.

Figure 2 focuses on the forward power link, i.e., the power transmission from the reader to the tag. This is reasonable since the communication range of most passive RFID systems is determined by the sensitivity of the tags. Owing to the parallel-connection topology of R_L and C_L, the voltage across the tag circuits, V_L, and the power into the tag circuits are maximized at the same time. A parasitic-aware OCA optimization procedure is necessary and promising in order to maximize V_L[8].

It is worth mentioning the differences between the design of the OCA in the UHF band and that of on-chip spiral inductors. First, the optimum operation frequency of the OCA in the UHF band is slightly lower than its self-resonant frequency (SRF), while an on-chip spiral inductor works better in the frequency band where its equivalent inductance remains stable and its equivalent quality factor is maximized; this is normally lower than its SRF. Second, the optimization of an on-chip spiral inductor focuses on the improvement of its equivalent quality factor. However, for the OCA in the UHF band, a maximized equivalent quality factor does not guarantee a maximized V_L. These differences are rooted in the appearance of V_{ind}, which requires insight into the OCA instead of regarding it as a black box or a macro model.

4. High efficiency rectifier with threshold compensation

A rectifier (i.e., an AC–DC charge pump in Fig. 1) is used to convert the AC power received by the OCA into a DC voltage. Usually, a charge pump using diodes or diode-connected MOSFETs and capacitors is applied to multiply the output DC voltage. Due to the threshold voltage of diodes or diode-

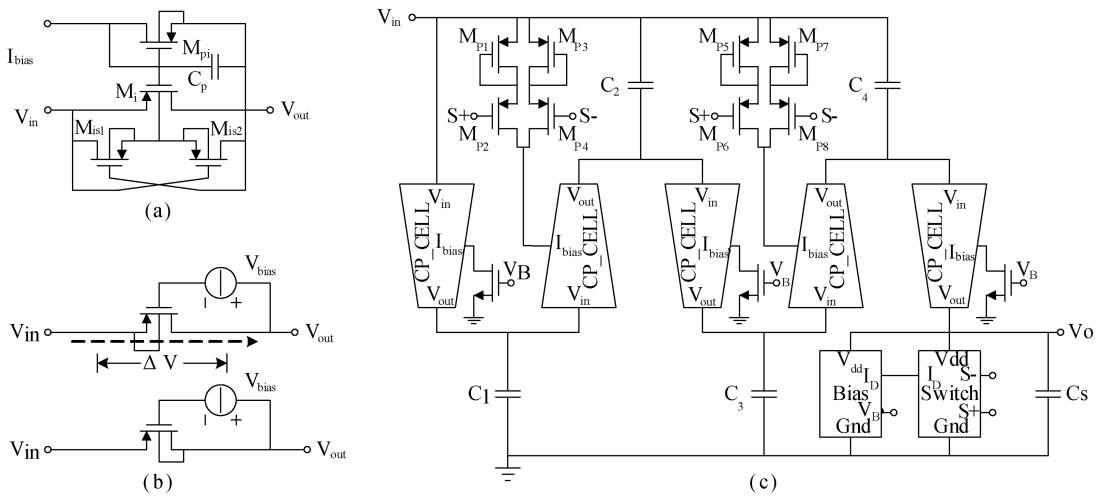

Fig. 3. Schematic of the proposed rectifier.

connected MOSFETs, the voltage drop and power loss on each stage seriously decrease the output DC voltage and the PCE. Although zero-threshold or low-threshold MOSFETs or Schottky diodes can mitigate this problem to some extent, at the same time they lead to more reverse leakage current and more power consumption in the substrate. Furthermore, they restrict the fabrication process adaptability and hence raise the fabrication cost. Since the power received by the OCA is much lower than that received by the off-chip antenna, there is a big challenge for the charge pump design, especially on the specification of the start-up voltage (the minimum input voltage to get a high enough output DC voltage) and the PCE. Moreover, the impedance match between the OCA and the charge pump is more difficult as the quality factor of the charge pump is much higher than that of the OCA. Limited by the fabrication process, the input impedance of an OCA is not very flexible. A better way to achieve a proper impedance match is to tune the input impedance of the charge pump. Assume the input admittance of the charge pump is $Y_{\text{in}} = Y_{\text{c}} + \text{j}\omega C_{\text{c}}$, where Y_{c} and ωC_{c} are the conductance and susceptance, respectively. The parasitic capacitor C_{c} is fixed under careful circuit design and layout; therefore, Y_{c} must be optimized to a higher value for a better impedance match, and it can be expressed by

$$Y_{\text{c}} = P_{\text{in}} \Big/ V_{\text{in}}^2 = P_{\text{c}} \Big/ \eta V_{\text{in}}^2, \tag{2}$$

where P_{in} is the input power of the charge pump, P_{c} is the total power consumption of the analog front-end, the digital baseband, and the EEPROM, η is the PCE, and V_{in} is the input AC voltage. In order to achieve the best performance, P_{c} must be as low as possible and η as high as possible, which means V_{in} must be minimized to optimize the impedance match. This puts more restrictions on the start-up voltage. Although we can easily reduce the start-up voltage by increasing the number of stages, the corresponding PCE will decrease due to the wasted power on the extra stages. A modified charge pump, with an internal feedback bias voltage to compensate the threshold voltage, is presented here.

The *i*th stage of the proposed rectifier, which is CP_CELL, is shown in Fig. 3(a). Two auxiliary MOSFETs Mis1 and Mis2, as switch transistors, are introduced to update the body voltage of the charge-transfer MOSFET M*i*. A diode-connected PMOS MP*i* is introduced to provide a bias voltage V_{bias}, which is lower than the threshold voltage V_{TH}. C_{p} is used to filter the high frequency components. Figure 3(b) presents the equivalent model of CP_CELL. If V_{in} is higher than V_{out}, M*i* is on and V_{bias} is used to cancel the threshold voltage; so the voltage drop in each stage, V, can be reduced. When V_{bias} is optimized to approach V_{TH} according to the equivalent load and input power, V will be minimized. The architecture of the proposed rectifier with five stages is shown in Fig. 3(c). The bias block is a PTAT circuit and provides current bias for the odd stages and the switch block. The even stages are biased by bias resistors (diode connected MP1, 3, 5, 7). MOSFETs MP2, 4, 6, 8 are switch transistors. The switch block chooses bias resistors (diode connected MP1, 3, 5, 7) according to the output voltage magnitude, in order to ensure the stabilization of the bias voltage on even stages[9].

A transient analysis shows that the output voltage rise process of the proposed rectifier resembles a positive feedback process. Figure 4 shows a comparison of the output voltage rising process between the proposed rectifier and the conventional one with 0.5 V AC input. During the period t_1, when the output voltage of this proposed rectifier is not high enough to start-up the bias block, the charge-transfer transistors have no compensation voltage; so the rectifier operates just as the conventional one. During the period t_2, once the output voltage is high enough to start-up the PTAT, the threshold voltage is cancelled and the output voltage rises quickly until its stabilization. The output voltage of the proposed rectifier is 2.5 times higher than that of the conventional one. The start-up voltage of the PTAT needs to be optimized as low as possible, in order to reduce the set-up time of the output voltage. Simulation results show that the PCE of the proposed rectifier can reach a maximum value of 40%. A good performance with

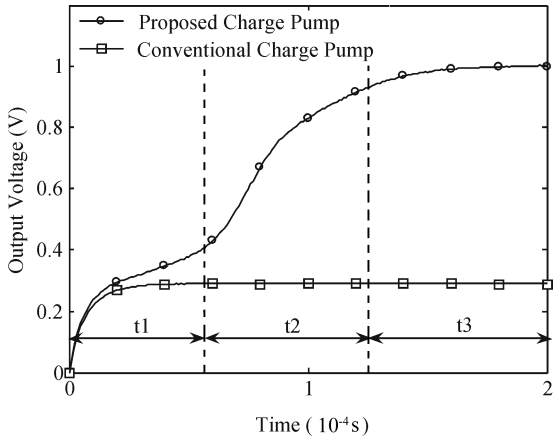

Fig. 4. Comparison of the simulated rising process between the conventional charge pump and the proposed one.

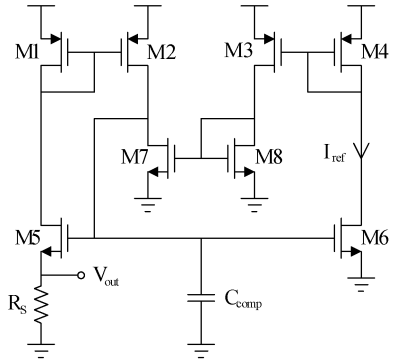

Fig. 5. PTAT generator.

both low start-up voltage and high PCE is obtained by using self-bias feedback and threshold compensation.

5. PTAT generator

The tag supply voltage, V_{dd}, varies a lot with the ASK modulated carrier. In order to maintain a correct operation state when the supply voltage fluctuates, a low-voltage high-PSRR reference generator is necessary. This work employs a PTAT generator[10]. The circuit topology is illustrated in Fig. 5. In this circuit, the power supply gain is degenerated by a feedback loop instead of by cascade current mirrors. The reduction of the overall transfer function from the power supply to the output is trivial; however, in this work we have $g_m = g_{m1} = g_{m2} \approx g_{m5}$, and $r_{ds} = r_{ds1} \approx r_{ds2} \approx r_{ds5} \approx r_{ds7}$, a PSRR on the order of $(g_m r_{ds})^2$ is observed, where g_{mi} and r_{dsi} are the transconductance and output resistor of MOSFET Mi, respectively.

6. Experimental results

In order to verify the OCA modeling method, a separated version of the OCA is fabricated, as shown in Fig. 6. The presented OCA is fabricated with the top metal layer of an SMIC 0.18 μm standard CMOS process with a thickness of 2.17 μm. It is in a roughly square shape with four corners cut to slightly reduce the radiation resistance for a better quality factor.

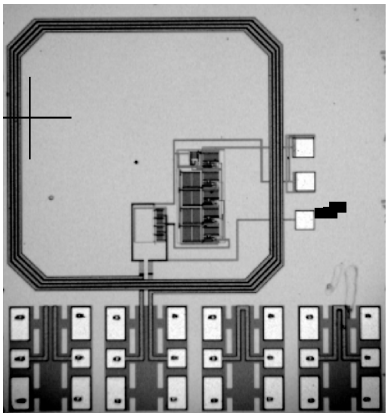

Fig. 6. Microphotograph of the OCA.

Table 1. OCA geometry.

Parameter	Value
Wire width	11 μm
Space between adjacent wires	2 μm
Outermost diameter	1 mm
Number of turns	4

Table 2. Summary of OCA characterization.

	OCA characterization at 900 MHz			Self resonant frequency (GHz)
	L (nH)	R (Ω)	Q	
Model	69.20	183.62	2.13	1.34
Simulation	64.66	148.56	2.46	1.30
Measurement	71.46	160.91	2.51	1.34

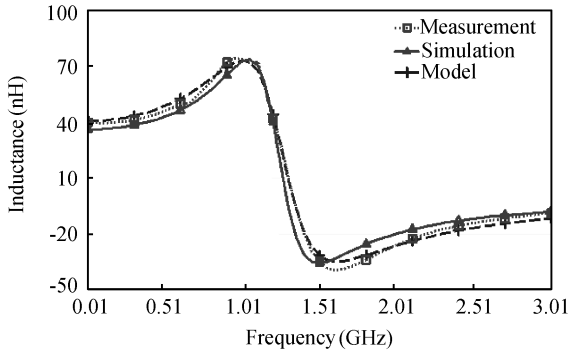

Fig. 7. Comparison of the OCA equivalent inductance between model, simulation, and measurement.

The detailed geometry of the presented OCA is listed in Table 1. Its measurement is carried out with a probe station and a vector network analyzer.

As listed in Table 2, the measured single-ended equivalent inductance and quality factor of this OCA are 71.46 nH and 2.51, respectively. A good match between model, simulation, and measurement is achieved as shown in Fig. 7.

Embedded with the OCA discussed above, a fully-integrated EPC Class 1 Generation 2 (C1G2) compatible tag is implemented in an SMIC 0.18 μm standard CMOS process, with a total area of 1 × 1 mm^2. The tag chip includes

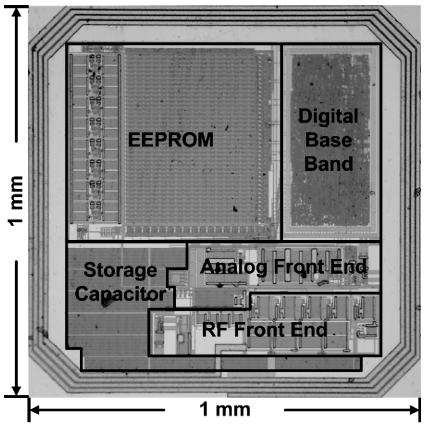

Fig. 8. Microphotograph of the tag chip.

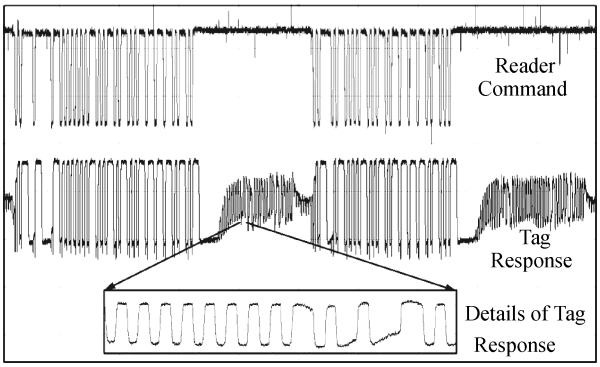

Fig. 9. Reader command transmitted and tag backscatter response.

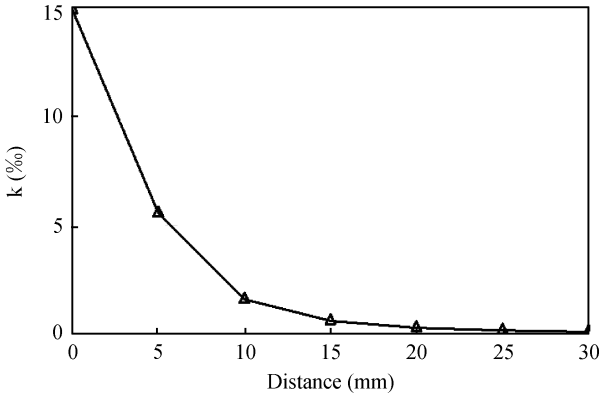

Fig. 10. Simulated coupling factor as a function of distance.

an RF/analog front-end, a digital base-band, and a 640-bit EEPROM memory. Its microphotograph is shown in Fig. 8, where the OCA surrounds the tag circuits.

The presented fully-integrated tag is tested with a near-field reader antenna which is a 1×1 cm^2 single-turn square loop antenna printed on an FR4 board. The reader antenna is matched to 50 Ω by inserting a matching network. Measurement results show that the communication range of the presented tag is up to 1cm with a 1 W reader output power. The reader command transmitted and tag backscatter response are shown in Fig. 9. Simulation results of the coupling factor k, the induced voltage upon the OCA $V_{\rm ind}$, the voltage across the tag circuits $V_{\rm L}$, and the power into the tag circuits are shown in Figs. 10, 11, and 12, respectively. As shown in Fig. 10, the coupling factor between the off-chip single-turn loop antenna

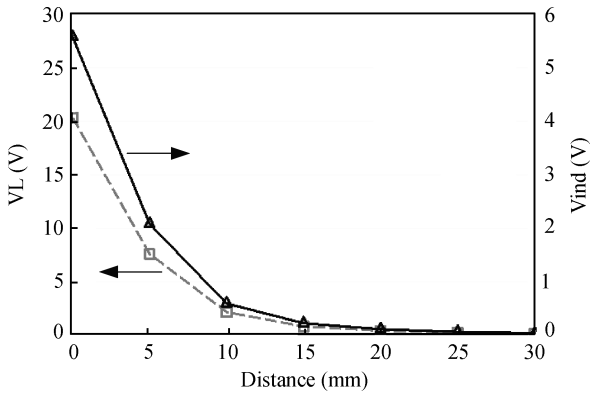

Fig. 11. Simulation results of the induced voltage upon the OCA and the voltage across the tag circuits as a function of distance.

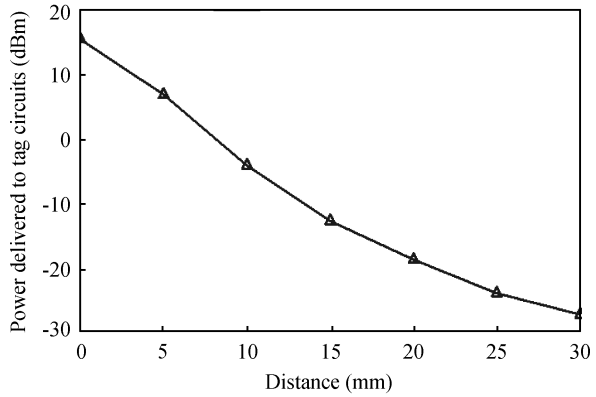

Fig. 12. Simulation results of the power delivered to the tag circuits as a function of distance.

and the OCA is on the order of 1‰, which is far less than the typical coupling factor of HF (13.56MHz) RFID systems. As shown in Fig. 11, the voltage boost from $V_{\rm ind}$ to $V_{\rm L}$ is demonstrated because the optimized OCA resonates well with the tag circuits at 900 MHz. It is worth mentioning that a dangerously high $V_{\rm L}$, say larger than 5 V, will be bypassed and actually will not appear at the input of the rectifier. The simulation was carried out with the same reader output power used in the measurement, with an assumed fixed $R_{\rm L}$ for simplicity. The simulated $V_{\rm ind}$, $V_{\rm L}$, and the power delivered to the tag circuits are a little overestimated after comparing with the measurement, mainly because of the underestimation of the loss of the reader matching network.

7. Conclusions

An EPC C1G2 compatible tag with an OCA, including a high efficiency rectifier, an RF/analog front-end, a digital base-band, and a 640-bit EERPOM memory, is implemented in the SMIC 0.18 μm standard CMOS process. The OCA for the UHF RFID falls into the category of electrically-small loop antennas. An optimized OCA design is achieved based on a novel model taking process parasitics into account. The PCE of the rectifier is vital to the successful integration of the OCA with tags, because of the extremely weak input power received

by the OCA. Self-bias feedback and threshold compensation techniques are applied to the rectifier to achieve a simulated PCE up to 40%. A good match between the tag circuits and the OCA is achieved by adjusting the rectifier input impedance. Since the high efficiency rectifier reduces the power requirement of the tag chip, the presented OCA succeeded in supporting a communication range up to 1 cm with 1 W reader output power using a near-field reader antenna. This work serves as a meaningful attempt to reduce the size and the cost of tags to a minimum for ILT.

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