

# A multi-standard active-RC filter with accurate tuning system

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**Abstract:** A low-power, highly linear, multi-standard, active-RC filter with an accurate and novel tuning architecture is presented. It exhibits IEEE 802.11 a/b/g (9.5 MHz) and DVB-H (3 MHz, 4 MHz) application. The filter exploits digitally-controlled polysilicon resistor banks and a phase lock loop type automatic tuning system. The novel and complex automatic frequency calibration scheme provides better than 4 corner frequency accuracy, and it can be powered down after calibration to save power and avoid digital signal interference. The filter achieves OIP3 of 26 dBm and the measured group delay variation of the receiver filter is 50 ns (WLAN mode). Its dissipation is 3.4 mA in RX mode and 2.3 mA (only for one path) in TX mode from a 2.85 V supply. The dissipation of calibration consumes 2 mA. The circuit has been fabricated in a 0.35  $\mu\text{m}$  47 GHz SiGe BiCMOS technology; the receiver and transmitter filter occupy 0.21 mm<sup>2</sup> and 0.11 mm<sup>2</sup> (calibration circuit excluded), respectively.

**Key words:** multi-standard; low pass filter; phase lock loop; frequency calibration; BiCMOS

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## 1. Introduction

Integrated continuous-time high-frequency baseband filters are essential building blocks in a wide variety of applications such as video and data transmission, which are pushing research toward the implementation of fully-integrated multi-standard transceivers. In order to allow the user to switch seamlessly between different standards, for both digital video broadcast and data applications, all the considered standards have to be supported by an integrated transceivers. The implementation of an integrated multi-standard transceiver has several advantages, such as minimization of silicon area and static power consumption and maximum possible hardware sharing among the transceivers<sup>[1]</sup>; in addition, an accurate calibration system is critical for efficient adjacent channel rejection. In active-RC filters, the frequency characteristics are determined in the form of RC time constants that might change according to variations in the fabrication process, operating temperature, supply voltage and aging. Accurate on-chip tuning schemes should be incorporated within the filter in order to compensate for the above variations and maintain the frequency responses to be within the desired specification. There are two possible ways to tune the RC time constant: active and passive component tuning. However, passive component tuning suffers from the mismatch between the tuning system and main filter, because only passive C or R components are adjusted within a set of discrete values, while not taking the nonideal factor of the operational amplifier into account. In order to guarantee a perfect match between them, this is usually done using a master-slave tuning system to lock the filter's response; the slave tuning system consists of a second-order low-pass filter which is replicated from the main filter. The slave filter response is locked by an external reference which is usually a

stable resistor or a clock signal.

This paper focuses on two core components: a low-power, high linearity, multi-standard filter, and an accurate automatic tuning system.

## 2. BB tunable filter

### 2.1. Main filter

In a direct-conversion receiver, the lack of channel filtering before the baseband filter limits the gain of the RF front-end as well as any baseband gain before the filter. The sixth-order Butterworth filter is used in the analog baseband and is implemented by the active-RC method. A block diagram of the active-RC filter is shown in Fig. 1(a). A 5-bit programmable binary-weighted capacitor array [Fig. 1(b)] with a  $\pm 50\%$  programmable range of values was employed to calibrate process and temperature drift. The gain, quality factor, and pole

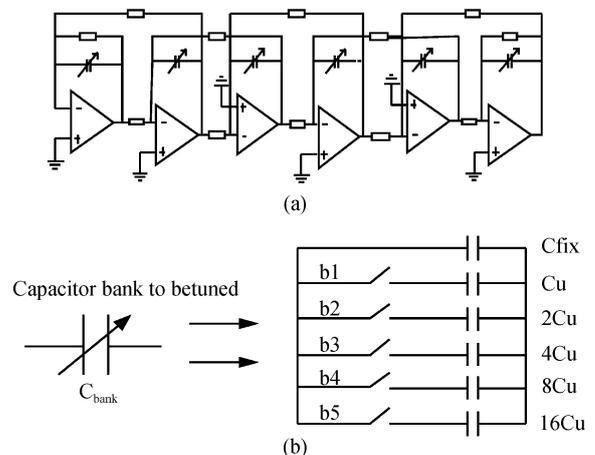


Fig. 1. (a) Schematic of the six-order main filter; (b) A programmable capacitor bank.

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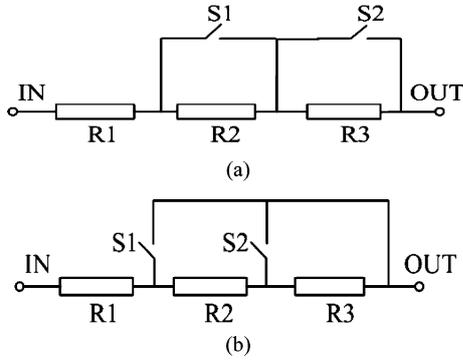


Fig. 2. (a) Ordinary series resistor; (b) One-hot variable resistor.

location of the filter are all determined by the MIM Caps and poly resistances. The active-RC filter can achieve better linearity than  $G_m$ -C filters, although the open-loop configuration of the  $G_m$  makes it possible to achieve low power consumption especially for wide-band filtering, but severely deteriorates the linearity. In order to decrease the passband sensitivity which results from element value variations, the leapfrog technique is used to synthesize the filter; the configuration of the filter is obtained from the RLC ladder prototype. The core of the tunable baseband filter has three modes of operation: two DVB-H modes with 3 MHz and 4 MHz corner frequency, and one WLAN mode with 9.5 MHz corner frequency. Switching between the three modes is accomplished by designing a series resistor which is shown in Fig. 2(b)<sup>[2]</sup>.

Figures 2(a) and 2(b) show a 2-bit ordinary resistor bank and one-hot variable resistor, respectively. The resistance of the variable resistor can switch to four difference values, and three of these are what we want. The gate widths of the nMOS switches should be large enough to ensure that on-resistances remain negligible with respect to the value of the resistor bank. The frequency response of the one-hot resistor is much better than that of the ordinary series resistor, since half of the parasitic capacitance is connected to virtual ground of an active-RC filter and it does not contribute to the frequency response. When the resistance is small, the equivalent pole frequency is very high, since most of the parasitic capacitance has no effect<sup>[2]</sup>.

As the GBW of the operational amplifier decreases, the  $Q$  of the filter increases abruptly from that of its LCR prototype. The required GBW for the Butterworth filter is about half that of the Chebyshev filter, so Butterworth filters can get higher cutoff frequency under the condition of lower GBW. For a 10 MHz 6th Butterworth, to keep the increase of the  $Q$  smaller than 5% ( $= 0.42$  dB), the GBW must be 120 ( $Q_{max} = 3$ ) times as large as the cutoff frequency of 10 MHz. So the GBW of the amplifier is not less than 1.2 GHz. Equation (1) can be applied to high-order filters, since a high-order filter can be divided into second- and first-order filters.

$$\frac{Q_L - Q_I}{Q_I} \approx \frac{1}{A_{amp} w_{amp} / 2w_1 Q_I - 1} \quad (1)$$

$Q_L$  is the  $Q$  factor of the lossy integrator which has a non-ideal amplifier;  $Q_I$  is the  $Q$  factor of the integrator with ideal

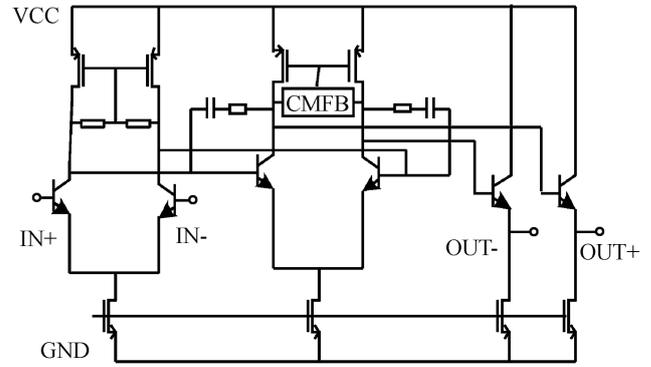


Fig. 3. Schematic of operational amplifier.

amplifier.  $w_1$  is the bandwidth of the filter.  $Q$  is defined as the gain at the cutoff frequency<sup>[2]</sup>.

The implementation of the OPAMP is shown in Fig. 3<sup>[3]</sup>. It is a typical two-stage Miller-compensation OPAMP with common feedback circuit. The simulation shows that the OPAMP can achieve a GBW of 1.2 GHz, phase margin of 70°, DC gain of 70 dB, and power consumption of 1.4 mW with a load capacitor of 500 fF (parasitic capacitor value of the capacitor-bank in the main filter, which is less than 10% of the total value of the capacitor-bank) and a load resistor of 10 kΩ.

## 2.2. Automatic frequency tuning for filters

In continuous-time filters, accurate on-chip tuning schemes should be incorporated with the filter in order to compensate for process and temperature variations and maintain the frequency responses to be within the desired specification. A corner frequency accuracy of 5% is needed to guarantee adjacent channel selectivity. In the active-RC filter implementation, the capacitors can be utilized for on-chip tuning operations and there are several efficient methods to implement this scheme. The digital control codes are sequentially generated and applied to the capacitor array until the desired outputs of the active-RC integrator are available and the tuning control is completed with this digital control code.

The whole automatic frequency tuning loop (ATL) is shown in Fig. 4(a)<sup>[4]</sup>. In order to verify the function, a second-order reference low-pass filter was made with the same unit elements as the main filter. Such a filter has a phase shift of exactly 90° at its resonant frequency  $f_0$ . A reference frequency  $f_{ref}$ , derived from the system clock, is divided by four in toggle flip-flop to obtain two signals with a phase difference of 90°. When tuned correctly, the reference filter's  $f_0$  equals  $f_{ref}/4$ . The tuning scheme therefore tries to make the phase shift through the filter exact 90° at  $f_{ref}/4$ . After a resistive attention, the 0° signal is fed through the reference filter, where it gets phase shifted through the filter by exactly 90°. After the filter, the signal is converted back to digital form by a comparator, and its phase is compared against the previously obtained 90° in a digital phase detector. The phase detector controls a charge pump, which is shown in Fig. 4(b). Its output is integrated on a capacitor. After a few cycles, a comparator makes a decision on the integrator output: whether  $f_0$

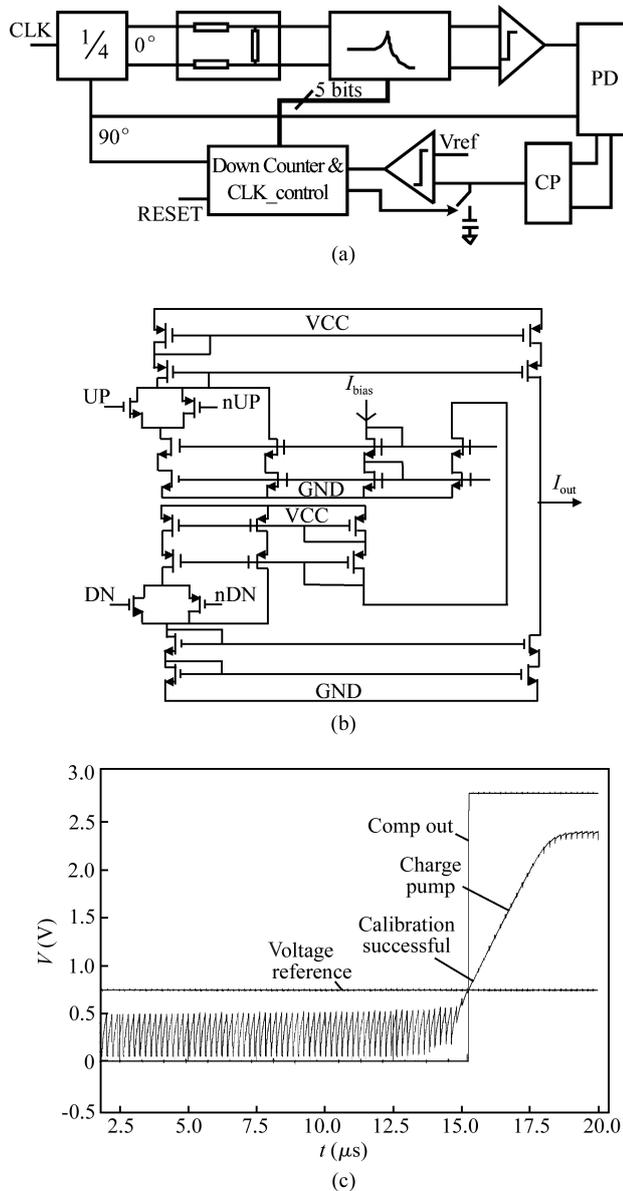


Fig. 4. (a) Calibration circuit schematic for the BB filter; (b) Charge pump schematic of the tuning system; (c) Calibration operation.

is too low or too high. The tuning setting is then updated, and the integrator is reset while the filter is allowed to settle to its new steady-state response. A down-counter is used for calibration. The automatic frequency tuning loop takes about 20  $\mu\text{s}$  to complete a 5 bit tuning period. The tuning operation is shown in Fig. 4(c); the tuning process occurs in a serial manner. In the initial state, all the tuning control bits are high and all feedback capacitors are connected, and the current of the charge pump output flows in, applying the minimum voltage of the integrator capacitor. The control bits and corresponding capacitors sequentially become low and disconnected from the circuit. At the moment when the current flows out, the voltage of the integrator capacitor immediately increases. When it is large enough for the output to reach the reference value during the four clk signal cycle (because the frequency of the control word clk signal is four times smaller than that of the clk signal) the tuning process is finished. At this point, the corresponding

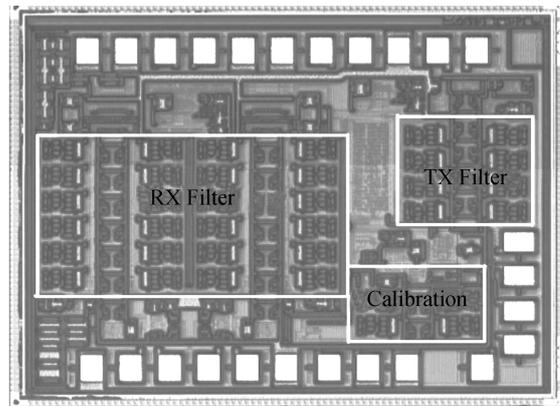


Fig. 5. Die photograph of the baseband RFIC.

control is acquired; in this way, the worst-case total number of clock cycles for tuning operation is  $2^N$  for a tuning accuracy of  $N$  bits. The tuning system can be turned off after tuning is complete.

The accuracy of the tuning is limited by excess delay in the filter path due to the compactor. A cascade of two differential low-gain stages following a digital inverter provides a bandwidth of 300 MHz and more than 35 dB dc-gain for a delay of less than 1 ns with a 200 mV 5 MHz input sine wave. This delay corresponds to a phase error of  $\Delta\phi = 2\pi f\Delta T$ , with a filter  $Q$  of 3; this translates into a frequency error  $\Delta f = \Delta\phi/2Q$ , well below the resolution of the programmable capacitors, which is about 4%.

### 3. Measurement results

The circuit is designed and fabricated in a 0.35  $\mu\text{m}$  47 GHz SiGe technology. Figure 5 gives the die photograph of the filter RFIC; the receiver and transmitter filters occupy 0.21  $\text{mm}^2$  and 0.11  $\text{mm}^2$ , respectively. Figure 6(a) shows the frequency characteristic of receiver filter; the left figure shows the DVB-H mode, and the right figure shows the WLAN mode; the AC response changes according to the control word. The filter's corner frequency deviates less than 3% for a temperature change from 0 to 85  $^{\circ}\text{C}$ ; therefore, as a result of the tuning schematic's 4%, the digital tuning word is not adjusted. Figure 6(b) shows the frequency characteristic of the transmitter filter. Its cutoff frequency is 12 MHz. Figure 7(a) illuminates the in-band linearity performance of a VGA (variable gain amplifier) and filter combination; the input two tone signals are at 4 MHz and 5 MHz of  $-23$  dBm for cutoff frequency 9.5 MHz and the VGA gain of 16 dB, so the calculated in-band IIP3 value of the filter is about 6 dBm. Figure 7(b) shows the group delay variation of the filter, which is 50 ns for the WLAN mode and 100 ns for the DVB-H mode. Table 1 gives the measurement result summary of the baseband filters.

### 4. Conclusion

This paper presents a low power multi-mode filter for a direct-conversion WLAN transceiver and DVB-H receiver. It was realized in 0.35  $\mu\text{m}$  SiGe BiCMOS technology. The receiver filter consumes 3.4 mA and the transmitter filter consu-

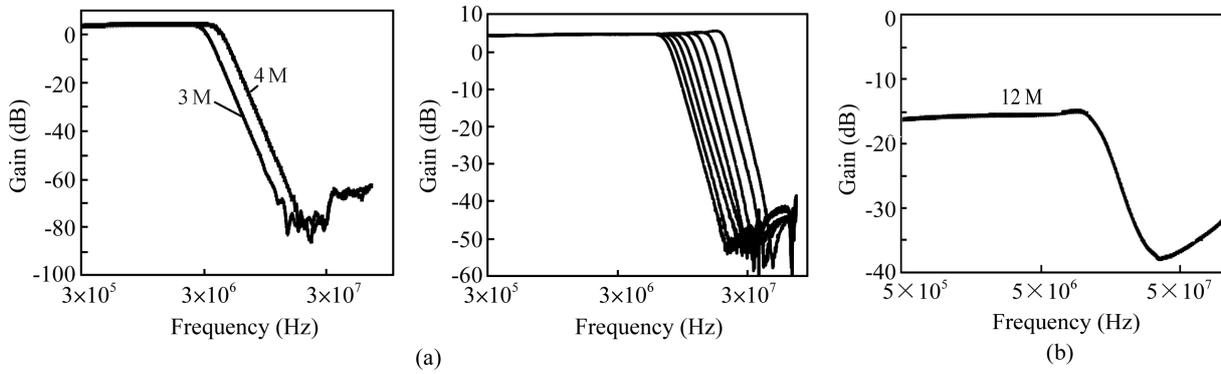


Fig. 6. Measured frequency characteristics of the filter with calibration results: (a) Receiver filter; (b) Transmitter filter.

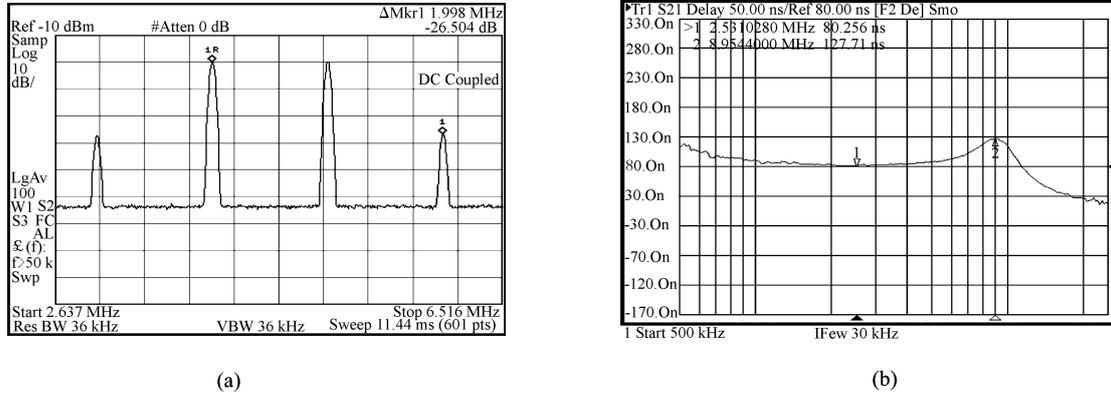


Fig. 7. (a) Measured in-band OIP3 of 5.7 dBm; (b) Measured group delay for the WLAN mode.

Table 1. Summary of baseband filters.

Parameter	Value
RX Filter's out-of-band IIP3	26 dBm
( $f_0 = 9.5$ MHz, $f_{\text{single}} = 15$ MHz, 28 MHz)	
Filter's in-band IIP3	6 dBm
( $f_0 = 9.5$ MHz, $f_{\text{single}} = 4$ MHz, 5 MHz)	
Filter's stopband attention	26 dB @ 15 MHz
( $f_0 = 9.5$ MHz, WLAN mode)	39 dB @ 19 MHz
Filter's stopband attention	23 dB @ 4.5 MHz
( $f_0 = 3$ MHz, DVB-H mode)	37 dB @ 6 MHz
Filter's stopband attention	23 dB @ 6 MHz
( $f_0 = 4$ MHz, DVB-H mode)	37 dB @ 8 MHz
TX Filter's stopband attention	16 dB @ 18 MHz
( $f_0 = 12$ MHz, WLAN mode)	25.5 dB @ 24 MHz
Filter's out-of-band IIP3	25 dBm
( $f_0 = 12$ MHz, $f_{\text{single}} = 20$ MHz, 41 MHz)	

mes 2.3 mA (only for one path) under a 2.85 V supply. The novel and complex automatic frequency calibration scheme, which provides better than 4% corner frequency accuracy, has

been successfully realized. The main filters achieve good linearity under low power dissipation. The measurement results show that the filter satisfies multi-standard specification.

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