Design of a high-performance PJFET for the input stage of an integrated operational amplifier*

Shui Guohua(税国华)[1], Tang Zhaohuan(唐昭焕)[1,†], Wang Zhikuan(王志宽)[1], Ou Hongqi(欧红旗)[1,2], Yang Yonghui(杨永晖)[1,2], Liu Yong(刘勇)[1,2], and Wang Xueyi(王学毅)[1]

(1 Sichuan Institute of Solid-State Circuits, CETC, Chongqing 400060, China)
(2 National Laboratory of Analog ICs, Chongqing 400060, China)

Abstract: With Shockley's approximate-channel theory and TCAD tools, a high-voltage, ultra-shallow junction PJFET for the input stage of an integrated operational amplifier (OPA) was realized. The high-performance PJFET device was developed in the Bi-FET process technology. The measured specifications are as follows. The top-gate junction depth is about 0.1 μm, the gate-leakage current is less than 5 pA, the breakdown voltage is more than 80 V, and the pinch-off voltage is optional between 0.8 and 2.0 V. The device and its Bi-FET process technology were used to design and process a high input-impedance integrated OPA. The measured results show that the OPA has a bias current of less than 50 pA, voltage noise of less than 50 nV/Hz$^{1/2}$, and current noise of less than 0.05 pA/Hz$^{1/2}$.

Key words: PJFET; operational amplifier; Bi-FET process; ultra-shallow junction; high input-impedance
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1. Introduction

With the rapid development of information technology, the requirements for system design are on the increase for high-performance integrated operational amplifiers (OPAs) in various fields such as satellite communications, infrared-guidance, precision instrumentation, smart sensors, high-fidelity audio and so on[1–3, 9]. To meet the needs, it is necessary to design and make a precision integrated OPA with excellent performances such as extremely low bias current, offset voltage, low-frequency noise and temperature drift[2, 7, 8].

Generally speaking, the bias current, noise, offset voltage, and temperature drift of an OPA are mainly determined by the input stage[2]. Therefore, the performances of an OPA mentioned above are dependent largely on the design of the input stage. A JFET is a kind of device in which the channel conductance is controlled by the gate voltage and realized by space charge region expansion of the gate-channel junction. Since a reversely-biased P–N junction has a very small leakage current, an integrated OPA with JFET used as an input stage has advantages such as high input-impedance (small bias current), low noise, and a small temperature drift.

In this paper, a set of new PJFET compatible bipolar processes (Bi-FET technology) is designed. The PJFET produced by the process is characterized by low gate leakage current, high breakdown voltage, and a 0.8–2.0 V adjustable pinch-off voltage, thus meeting the design requirements of the high input-impedance integrated OPA input stage. A cross section of the PJFET compatible with the bipolar devices merged in this process is shown in Fig. 1.

2. PJFET design and realization

To make a high-performance PJFET for the input stage of a high input-impedance integrated OPA, the key technologies of structure, process and layout need to be broken through.

2.1. Structure design

As shown in Fig. 2, the PJFET channel is controlled by both top-gate and back-gate voltages. Because the back-gate concentration is two orders of magnitude lower than that of the top-gate, single-gate pinch-off theory can be used to approximately analyze and numerically calculate it.

In the structure design, the main parameters to be considered are pinch-off voltage, gate leakage current, breakdown voltage, and output current density. The key is a smaller gate leakage current and a higher breakdown voltage. Our goal is a pinch-off voltage of 1.0 V as a typical value, and a gate leakage current of less than 5 pA.

The formula of the reversely-biased P–N junction leakage current (I_{leak}) is expressed as

$$I_{\text{leak}} = \frac{qD_{\text{A}}n_{\text{p0}}}{L_{\text{p}}}\left[\exp\frac{qv}{kT} - 1\right]A. \tag{1}$$

It can be seen that I_{leak} is directly proportional to channel doping concentration. Thus, in theory, it is hoped that the lower the doping is, the better the reduction of the leakage current will be.

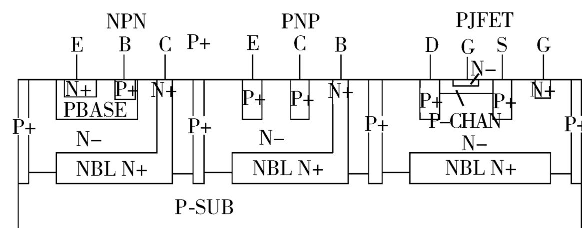

Fig. 1. Cross section of PJFET and bipolar devices.

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† Corresponding author. Email: sisc_tang@163.com
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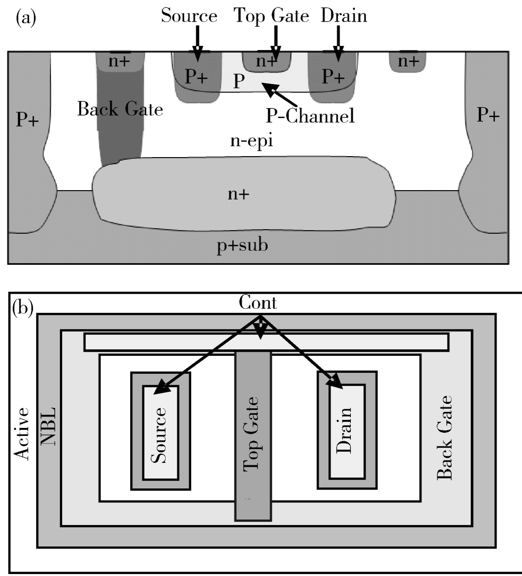

Fig. 2. (a) Cross section. (b) Layout of the PJFET.

Based on the low leakage current and low doping concentration process，current distribution at both sides of the channel and the thickness of the P–N junction depletion region between the top-gate and the channel can be ignored. In theoretical analysis and numerical calculation, Shockley's approximate-channel theory can be used. The intrinsic gate–source pinch-off voltage (V_{TH0}) can be given by Eq. (2)[5].

$$V_{TH0} = V_{DS} - V_{TH} = \frac{2qN_Aa^2}{\varepsilon\varepsilon_0}, \tag{2}$$

where V_{TH} is the gate–source pinch-off voltage at a drain-source voltage of V_{DS}, N_A is the doping concentration of the channel； a is the half thickness of the channel. From Eq. (2), N_A at different channel thicknesses can be obtained by Eq. (3).

$$N_A = \frac{\varepsilon\varepsilon_0 V_{TH0}}{2qa^2}. \tag{3}$$

From Eq. (3), it can be observed that the doping concentration (N_A) in the channel is inversely proportional to a^2.

Based on Shockley's approximate-channel theory, the maximum saturation drain–source current (I_{DSS}) can also be given, as shown in Eq. (4).

$$I_{DSS} = \frac{2a^3Wq^2\mu_pN_A^2}{6\varepsilon_r\varepsilon_0L} = \frac{2aW}{3\rho L}V_{TH0}. \tag{4}$$

From Eq. (4), it can be seen that I_{DSS} is the directly proportional to both a and N_A; that is, to improve I_{DSS} , it is best to increase both a and N_A . But there is another parameter to be considered, that is,

$$BV_{GS} = \frac{\varepsilon_s}{2qN_A}\varepsilon_{max}^2. \tag{5}$$

As shown in Eq. (5), BV_{GS} is inversely proportional to N_A.

Based on the above relations, to meet the requirements of the device design, a balance needs to be struck between the pinch-off voltage, breakdown voltage and output current density.

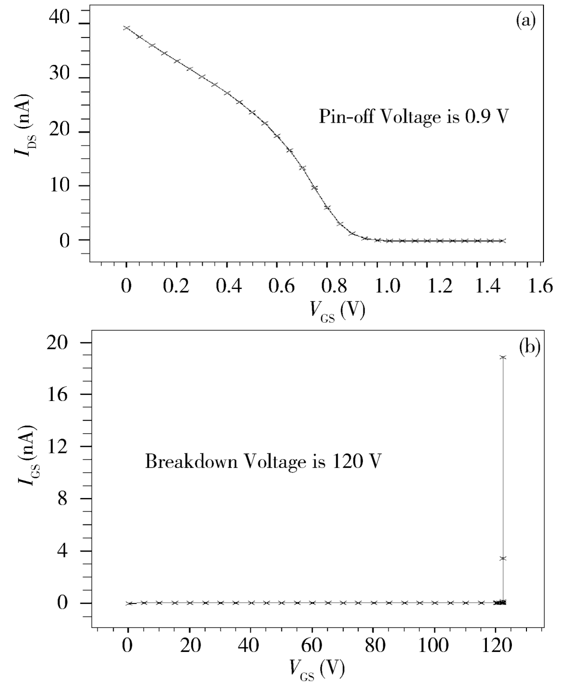

Fig. 3. (a) Simulated V_{GS}–I_{DS} curve of PJFET. (b) Simulated I_{GS}–V_{GS} curve of PJFET.

According to Eq. (5), to obtain a high enough BV_{GS} to meet the requirement first, the maximum concentration of the channel can be affirmed. Then in accordance with Eq. (3) the maximum thickness of the channel can be determined, and from Eq. (4) the output current can be obtained.

First of all, there is a rough engineering estimate. To obtain a BV_{GS} greater than 80 V, the channel doping concentration should be at the level of 10^{16}, about 3×10^{16} cm^{-3}. Also, it can be inferred that the channel thickness is about 0.2 μm; the output current density is about 1.5 μA/μm. In theory, the gate leakage current is very low, but the actual situation is related to the quality of the junction and the surface conditions.

Due to the low pinch-off voltage and thin channel thickness, the junction uniformity and flatness are essential. Therefore, the shallow junction process is necessary to produce the top-gate and the channel.

Using TCAD tools, the static parameters of the PJFET are simulated. As shown in Fig. 3, the value of the pinch-off voltage (V_{TH}) is about 0.9 V, the value of breakdown voltage reaches 120 V, and the saturated output current reaches 1.5 μA/μm (not shown). The results can meet the design requirements, and the simulated curves are shown in Fig. 3.

In terms of AC characteristics, in accordance with the input stage requirements of precision OPA, the main consideration is the noise characteristic. The noise in JFET devices consists mainly of thermal noise, gate shot noise, $1/f$ noise, and gate induced noise[1, 4, 10, 11]. Of the four types of noise, thermal noise and $1/f$ noise exist in all semiconductor devices, giving little room for performance optimization; gate induced noise mainly has an effect at high frequency; the key noise to be considered is therefore the gate shot noise. Its spectral density (S_{igl}) is given by Eq. (6)：

$$S_{igl} = 2qI_G. \tag{6}$$

It can be seen from the above discussion that the gate leakage current (I_G) of the PJFET is very low. Based on Eq. (6), the S_{igl} is very low too. Therefore, the JFET designed in this paper has inherent low-noise characteristics.

2.2. Process design

The Bi-FET process technology designed in this paper not only integrates the normal bipolar devices, but also provides the PJFET, Si_3N_4 MIS capacitor, trimmable metal-film resistor and so on. Of the various devices, the metal-film resistor with laser trimming is able to meet the low input offset requirements of the precision OPA.

The main process flow is shown as follows:

Initial silicon wafer → NBL → PBL → N^- epitaxy → N^+deep collector → P^+ ISO → base oxide → P^+(extrinsic base and PJFET S/D) implant → base implant → base anneal/oxide → N^+ emitter implant/anneal → PJFET active → thin oxide → P^- channel implant → N^- top-gate implant → anneal → LTO → CAP → cont → SICR → metal … .

The key technologies are as follows.

2.2.1. PJFET and bipolar compatible process

There are two difficulties in the Bi-FET process technology. On the one hand, the PJFET process module is relatively independent from the previous bipolar process, and is not influenced by it; on the other hand, the PJFET process module does not affect the characteristic of bipolar devices.

Firstly, the PJFET is produced based on the basically completed bipolar process, with three photolithographies added. The part flow is as follows: PJFET active area opening to expose the epitaxy layer; thin oxide growth to reduce damage and store impurities; P-type impurity implantation following channel photolithography; N-type impurity implantation following top-gate photolithography; finally low-temperature annealing to activate the impurities. A cross section of the device structure is shown in the Fig. 2(a).

Secondly, the bipolar device produced before the JFET is a deep-junction device which is formed at a high temperature of up to 1100 °C, making the concentration distribution in base and emitter basically fixed. The JFET in the later process is a shallow-junction device, the process for which is low-temperature annealing at about 850 °C. It is mainly used to active the dopant, but not to affect the previous bipolar devices. So the impact on the performance of the bipolar devices can be ignored.

In this way, not only can good device performance including both JFET and the bipolar device be ensured, but compatibility of the PJFET process with the bipolar process is also realized.

2.2.2. PJFET key process

As mentioned above, it is absolutely necessary to make shallow junctions with high uniformity and flatness. To get 0.2–0.3 μm shallow junctions for the channel, B^{11+} and F^+ ions were twice implanted into the channel with different energies and doses. The F^+ ion is used to inhibit boron from diffusing. The P^{31+}or As^+ ion at low energy is used to produce the ultra-shallow junction for the top gate, with a junction depth about 0.1 μm. Low temperature annealing is then carried out to activate both the channel and the top gate dopant.

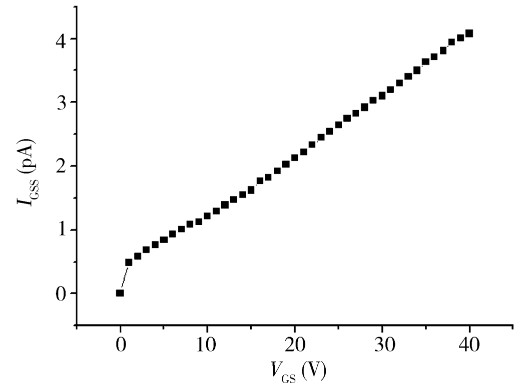

Fig. 4. I_{GSS}–V_{GS} curve of the PJFET.

In order to meet the requirements of different circuits, different values of gate–source pinch-off voltage were achieved by accurately adjusting the concentration distribution of the channel and also the top gate.

The gate leakage current consists of two parts. One is a gate-channel reversely-biased P–N junction leakage current, and the other is the surface leakage current. To obtain a very low gate leakage current, which serves as the input bias current and whose typical value reaches the order of pA, one method is to lower the junction defect density, and the other is to reduce the surface leakage, which is normally the main part. The thicknesses of Si_3N_4 and SiO_2 films and the annealing process menus were optimized to eliminate defects in the PN junction region, reduce the dielectric stress mismatch, and then decrease the gate leakage current. Strict pollution control is a normal practice as well.

The gate–source reverse bias current testing results are shown in Fig. 4. It is clear that the gate leakage current is lower than 5 pA.

2.3. Layout design

In layout design, the breakdown voltage and output current density are mainly taken into account. In fact, the breakdown voltage between drain and source (BV_{DSS}) is the reverse breakdown voltage of the PN junction between gate and channel. The space charge region of the reverse PN junction extends from channel to drain, so the breakdown voltage usually depends on the space between gate and source/drain. If the distance between gate and source is in the range from 0 to 12 μm, a BV_{DSS} of 10–120 V will be obtained. If the G–S/D space is larger, then D–S breakdown will be P–N junction avalanche breakdown; however, if the G–S/D space is smaller and P–N junction avalanche breakdown is not reached, then D–G punch-through breakdown will occur. Therefore, a different G–S/D space is designed based on the different breakdown voltage requirements of the PJFET used for the OPA.

In a practical device, affected by defects in the junction and on the surface, the breakdown voltage is usually fairly low. To further raise the breakdown point, RESURF-based electric field technology is used in the layout design in order to vary the distribution of the depletion layer on the device surface, thus varying the electric field strength and improving the breakdown voltage[6]. Using field-plate technology, the PJFET breakdown voltage can be increased by 5–10 V.

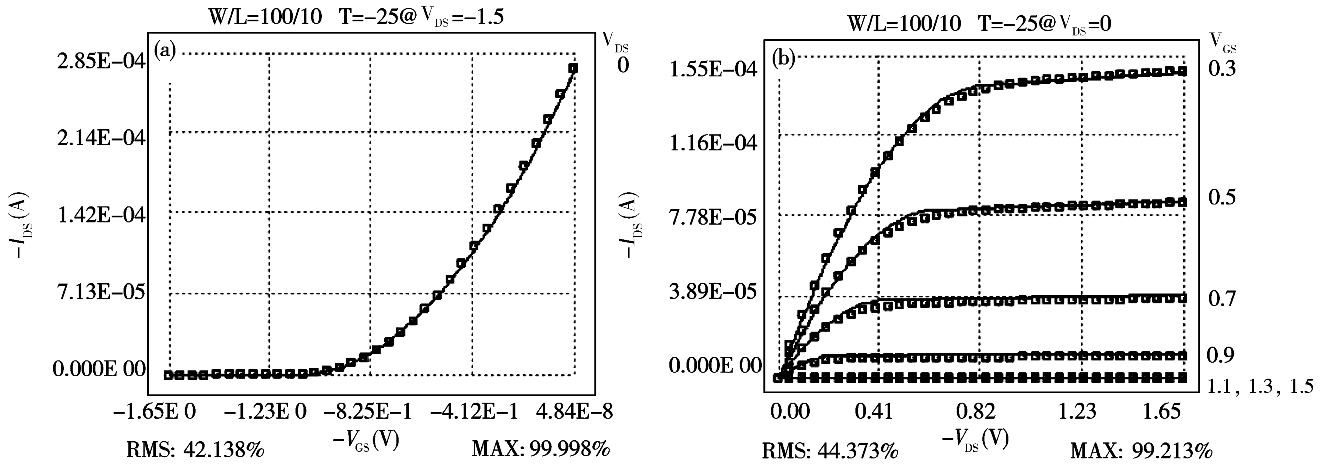

Fig. 5. (a) Measured V_{GS}–I_{DS} curve of PJFET. (b) Measured output characteristic of PJFET.

Table 1. Measured results of PJFET.

Parameter	Symbol	Value	Unit
Gate–source cutoff voltage	V_{GS}	1.0	V
Gate–source breakdown voltage	$BV_{GS(OFF)}$	105	V
Gate reverse current	I_{GSS}	1.2	pA
Zero gate voltage drain current	I_{DSS}	210	μA
Input impedence	Z_{IN}	4×10^{10}	Ω
On resistance	R_{ON}	8.5	kΩ
Forward transfer-conductance	G_{FS}	0.05	mS

From Eq. (3), the output current density can be improved by decreasing the channel length. In addition, the on-resistance consists of three parts (R_S, R_{CH}, and R_D):

$$R_{on} = R_S + R_{CH} + R_D, \tag{7}$$

where R_S/R_D is the bulk resistance from the S/D contact to the S/D end of channel, and R_{CH} is the resistance of the channel.

The intrinsic output current is expressed by Eq. (3), and the final output current density is still influenced by R_S and R_D. Therefore, in layout design, breakdown voltage and sufficient early voltage are required, and the effect of channel length and G–S/D spacing should be taken into consideration.

In addition, the top-gate junction depth of the PJFET is only 0.1 μm. The standard metallization process cannot solve problems such as PN junction puncture (diffusion of metal into silicon). In order to resolve these problems, the contact should be placed at the N^+ ring area, with which the top-gate is connected to the back-gate, as shown in Fig. 2.

3. Results and application

By researching the structure, process and layout, a PJFET that meets the specifications of the input stage of an integrated OPA is obtained. Figure 5 and Table 1 show parts of the testing curve. It can be seen that the measured DC parameters of the PJFET are basically consistent with the design values.

As mentioned above, the PJFET process is compatible with the bipolar process. Finally, the PJEFT process is used in a high-input impedance integrated OPA, the bias current of which is less than 50 pA at ± 35 V. Table 2 shows some of the measured results for the circuit.

Table 2. Bias current of the OPA at ±35 V.

I_b+ (nA)	I_b- (nA)	I_{OS} (nA)	A_{VO} (dB)	I_S (mA)	I_O+ (mA)
0.012	0.026	-0.014	106	7.85	27.9
0.010	0.028	–0.018	116	7.85	27.6
0.009	0.018	–0.009	106	7.85	27.7
0.012	0.019	–0.007	102	7.85	27.7
0.018	0.028	–0.10	109	7.84	27.9
0.014	0.027	–0.013	108	7.84	27.9
0.012	0.020	–0.008	107	7.84	27.6
0.013	0.021	–0.008	99	7.84	27.3

4. Conclusion

A high-performance PJFET, with the advantages of good compatibility with the bipolar process, high-input impedance, low noise and high breakdown voltage, has been successfully realized,. Moreover, the PJFET is used for the input stage of a high input-impedance Bi-FET integrated OPA, the bias current of which is less than 50 pA, the voltage noise is less than 50 nV/Hz$^{1/2}$, and the current noise is less than 0.05 pA/Hz$^{1/2}$.

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