Carrier stored trench-gate bipolar transistor with p-floating layer

Ma Rongyao(马荣耀)[1], Li Zehong(李泽宏)[1, 2, †], Hong Xin(洪辛)[1], and Zhang Bo(张波)[1]

(1 State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China)
(2 Wuxi China Resources Huajing Micro Electronics Co LTD, Wuxi 214061, China)

Abstract: A carrier stored trench-gate bipolar transistor (CSTBT) with a p-floating layer (PF-CSTBT) is proposed. Due to the p-floating layer, the thick and highly doped carrier stored layer can be induced, and the conductivity modulation effect will be enhanced near the emitter. The accumulation resistance and the spreading resistance are reduced. The on-state loss will be much lower than in a conventional CSTBT. With the p-floating layer, the distribution of electric fields of the conventional IGBT is reformed, and the breakdown voltage is remarkably improved. The simulation results have shown that the forward voltage drop (V_{CE-on}) of the novel structure is reduced by 20% and 17% respectively, compared with the conventional trench IGBT (TIGBT) and CSTBT under the same conditions. Moreover, an increment of more than 100 V of the breakdown voltage is achieved without sacrificing the SCSOA (short circuit safety operation area) compared with the conventional TIGBT.

Key words: p-floating layer; carrier stored layer; CSTBT; TIGBT
DOI: 10.1088/1674-4926/31/2/024004 **EEACC:** 2560

1. Introduction

since the invention of the power insulated gate bipolar transistor (IGBT) in the last century, its application has extended over more fields due to its many merits such as low losses, high switch speed, high reliability and easy modularization. In particular, when it is used in industrial high voltage systems, it is required to be resistant to high breakdown voltages and to have a low voltage drop in the on-state. The conventional trench IGBT (TIGBT)[1] was invented for lower on-state voltage drops and higher integration due to smaller cell pitches. However, the TIGBT exhibits weaker ruggedness such as a smaller short circuit safety operation area (SCSOA) and breakdown voltage degradation. The carrier stored trench-gate bipolar transistor (CSTBT)[2, 3] (Fig. 1(a)) which employs an n-type layer (carrier stored layer) provides a better trade-off between the forward voltage drop (V_{CE-on}) and SCSOA. The n-type CS layer improves the conductivity modulation by enhancing the lateral diffusion of electrons and placing a barrier to holes, whereas the breakdown voltage of the CSTBT is greatly influenced by the concentrated electric field near the p-base/CS-layer junction, especially when increasing the CS layer doping. When employing a p-floating layer in the TIGBT[4, 5] (P-FIGBT) (Fig. 1(b)), the breakdown voltage characteristic is improved. However, the V_{CE-on} increases sharply due to the parasitic JFET effect. For a better trade-off between V_{CE-on}, breakdown voltage, and SCSOA, we present a novel carrier stored trench IGBT with a p-floating layer (PF-CSTBT) (Fig. 1(c)). The proposed PF-CSTBT exhibits excellent on-state characteristics and a much higher breakdown voltage without reducing the SCSOA. These merits were proved by the 2D simulation tool, MEDICI[6].

2. Device structure and operation

Figure 1 shows a CSTBT, a P-FIGBT, and the proposed PF-CSTBT. Compared to the CSTBT, the proposed structure has a thicker and more highly doped CS layer between the deep trench gates, and a p-floating region is located at the bottom of the deep trench.

This is accomplished by additional boron implantation after the trench process. This implantation is performed right after the trench process, which means that no additional mask is required. The implantation step should not dope the sidewalls of the trenches, preventing threshold voltage shift and degeneration of the "carrier stored effect". As to the CSTBT, for achieving a better trade-off between V_{CE-on} and forward blocking voltage, a thin CS layer with a concentration of about 10^{15} cm^{-3} was chosen. The doping and the depth of the CS layer must be controlled accurately in high voltage applications, otherwise the blocking voltage will be seriously influenced by the elevated electric field near the p-base/CS layer junction. Being shielded by the p-floating layer in the PF-CSTBT, the voltage supported by a depletion region forming on both sides of the p-base/CS layer junction is much lower even within high voltage applications. Thus, a CS layer which is thicker and more highly doped compared with the CSTBT is introduced into the proposed structure.

During the on-state of the PF-CSTBT, the thick and highly doped CS layer performs excellently. First, the spreading angle of the electron current from the channel is increased obviously, while it is restricted in the TIGBT[7] and P-FIGBT due to the lightly doped N-drift region and the parasitic JFET elements. Second, the hole-barrier effect is much improved compared with the CSTBT, and the conductivity modulation effect is enhanced in the N-drift region. Third, the proposed CS layer is located at the region where the conductivity modulation effect is low in the conventional TIGBT. So the thick and highly doped CS layer compensates a part of the on-state loss near the p-base region. Moreover, with the more highly doped CS layer, the parasitic JFET effect between the p-base and the p-floating

† Corresponding author. Email: lizh@uestc. edu. cn
Received 22 August 2009, revised manuscript received 23 October 2009

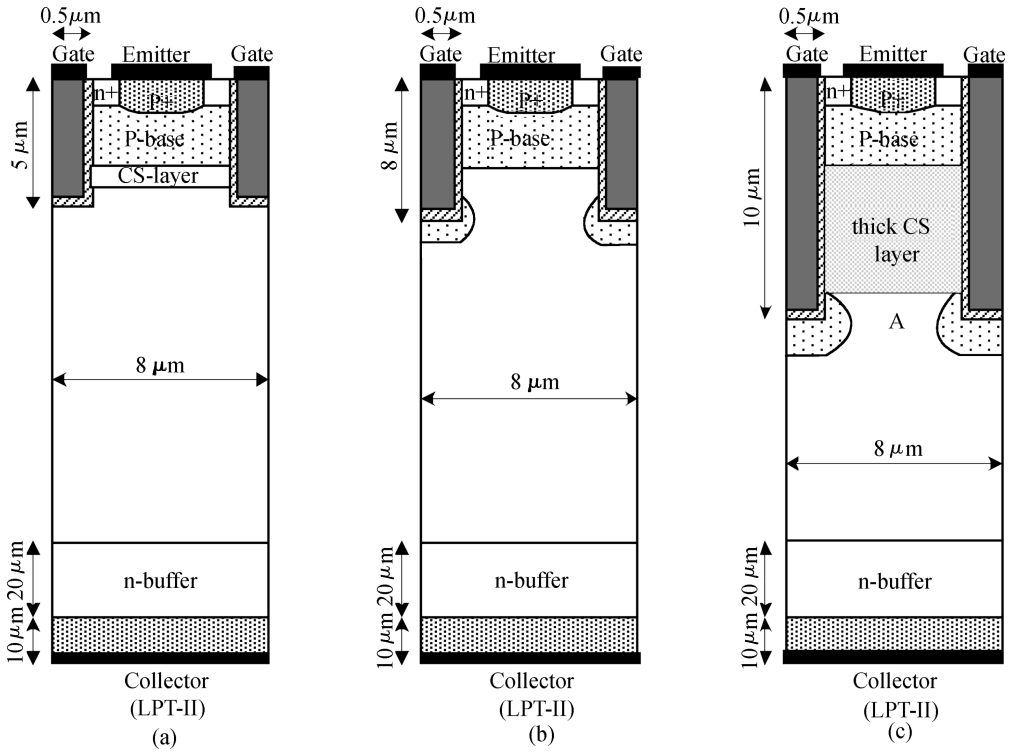

Fig. 1. (a) CSTBT. (b) P-FIGBT. (c) PF-CSTBT.

Table 1. Simulation parameters

Parameter	Size (μm)	Concentration (cm^{-3}) / Resistivity (Ω·cm)
PF-CSTBT trench gate	Depth is 10, width is 0.5	N/A
IGBT, CSTBT trench gate	Depth is 5, width is 0.5	N/A
P-FIGBT	Depth is 8, width is 0.5	N/A
Emitter	Etched silicon is 0.5	N/A
Gate oxide thickness	0.06	N/A
Drift region length	100 (from the surface)	86.5
n-buffer	20	1×10^{16}
p-type collector	8	1×10^{17}
p^+-type contact collector	2	1×10^{19}
p-base	Junction depth is 4.0	1×10^{17}
n^+ of emitter	Junction depth is 1.2	1×10^{20}
p^+ of emitter	1.3	5×10^{19}
Thick CS layer	5	$5 \times 10^{15} - 8 \times 10^{16}$
CS layer of CSTBT	1	1×10^{15}
p-floating layer (P-FIGBT)	Junction depth is 1.8	5×10^{17}
p-floating layer (PF-CSTBT)	Junction depth is 0.6–3	5×10^{17}

region can be neglected, and the JFET effect between the p-floating regions (region 'A' in Fig. 1(c)) is weakened due to the voltage drop from region 'A' to the emitter electrode being reduced. Furthermore, the accumulation resistance is reduced due to the more highly doped CS layer. More electrons enter into the p-floating layer, combining with the holes, which also alleviates the JFET effect between the p-floating layers.

In the forward blocking mode, the p-floating layer stops most of the electric field. With the increase of the collector voltage, the depletion region which spreads from the p-floating layer/N-drift junction pinches off the JFET region, producing a potential barrier at location 'A'. Consequently, a high electric field develops in the N-drift region below the p-floating shielding layer while the electric field at the p-base region and the CS layer remains low. This improves the forward blocking performance and the safety operating area (SOA) capability. Besides, a deeper p-floating layer can also enhance hole extraction when the gate voltage turns to negative bias during the turn-off period.

3. Results and discussion

The simulation software MEDICI is adopted to analyze the characteristics of the device. Light punch-through (LPT-II)[8, 9] collectors proposed by the Mitsubishi Electric Corporation are applied in the simulation. The simulated parameters of the P-FIGBT, CSTBT, conventional IGBT and the discussed structure PF-CSTBT are exhibited in Table 1 (the hole lifetime is 1 μs).

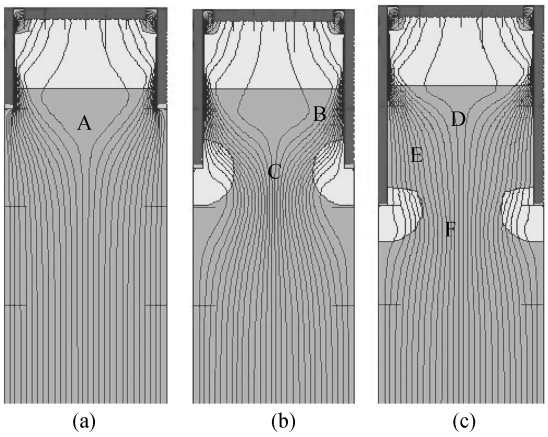

Fig. 2. Current distribution of (a) conventional IGBT, (b) P-FIGBT, and (c) PF-CSTBT at $V_{\text{gate}} = 12$ V, $V_{\text{collector}} = 8$ V.

3.1. Forward conduction

The conductivity modulation effect in the PF-CSTBT is enhanced due to the application of a thick and highly doped CS layer in the low conductivity modulation area. Thus, the disadvantage of a conventional IGBT that the conductivity modulation becomes weaker below the p-type base area is compensated. Figure 2 demonstrates the two-dimensional graph results of the current distribution during the on-state of the conventional IGBT, P-FIGBT and PF-CSTBT. For the conventional IGBT, a large depletion area emerges below the p-type base ('A' in Fig. 2) during the on-state period, limiting the area and triangle of current spreading. Figures 2(a) and 2(b) reveal that the current spreading triangles of the conventional IGBT and P-FIGBT are both less than 45°, while in the PF-CSTBT it is more than 45 °. Meanwhile, in the PF-CSTBT, the current spreading area below the p-type base is greatly enlarged compared with the other two device structures (area 'D' is smaller). Moreover, two JFET areas are introduced at locations 'B' and 'C' of the P-FIGBT (Fig. 2(b)), resulting in the convergence of current as well as an increase of voltage drop at the two locations. It can be concluded that no apparent JFET effect exists in the proposed PF-CSTBT and the current distributes uniformly in a larger area when comparing the current distribution at locations 'E' and 'F' in Fig. 2(c).

A comparison between the I–V characteristics of the PF-CSTBT, IGBT, CSTBT and P-FIGBT with different p-floating layers is given in Fig. 3. As shown in Fig. 3, the voltage drop of the PF-CSTBT is apparently decreased compared with the conventional IGBT and CSTBT, while the forward voltage drop of the P-FIGBT is the largest due to the JFET effect. Under current conditions of 200 A/cm^2, the voltage drops of the PF-CSTBT (the p-floating layer junction depth is 1.8 μm) are 16%, 20% and 27% lower, respectively, compared with the CSTBT, conventional IGBT and P-FIGBT. With the increase of p-type base depth (between 0.6 and 3 μm) in the PF-CSTBT, the JFET effect is enhanced, resulting in a voltage drop increment. However, when the depth reaches 3 μm, the VCE-on decreases by nearly 12% and 16% compared with the CSTBT and conventional IGBT. The saturation current of the PF-CSTBT does not increase while the forward voltage drop decreases as shown in Fig. 4. Thus, the PF-CSTBT has the same SCSOA as the

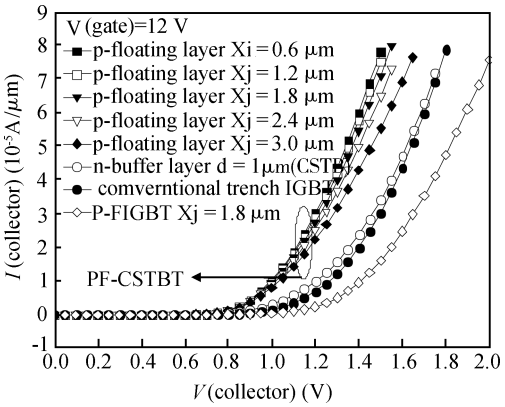

Fig. 3. Comparison between I–V characteristics of different p-floating layers.

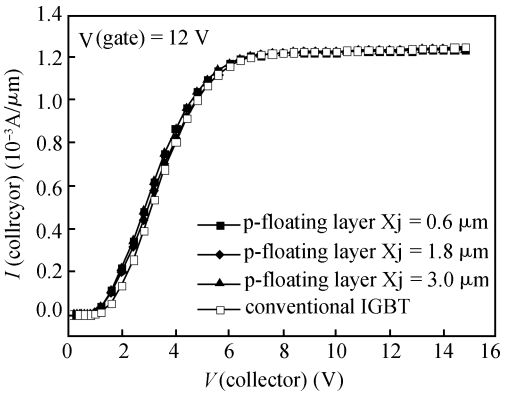

Fig. 4. Comparison of saturation current.

TIGBT when on-state dissipation declines.

3.2. Analysis of breakdown voltage

When a forward bias is applied to the conventional IGBT and CSIGBT in the blocking state, the electrical field peaks appear high at the p-type base and the corners of the trench gate, resulting in a decrease of the forward blocking voltage. Although the thick CS layer with high concentration reduces the breakdown voltage in the CSTBT, the blocking capacity is enhanced in the proposed device, because the p-floating layer stops the electrical field, leading to the electrical field peak transferring towards the p-floating layer as well as lowering the field at the p-type base junction and around the trench gate. Figure 5 indicates a lower breakdown voltage for the CSTBT compared with the conventional IGBT. However, an augmentation of breakdown voltage as large as 100 V can also be observed when comparing the PF-CSTBT (with the p-floating layer at a junction depth of 1.8 μm) with the conventional IGBT. Meanwhile, with the enlargement of the p-floating layer area, PF-CSTBT's breakdown voltage increases with an increment of up to 200 V compared with the conventional IGBT.

Figure 6 shows the two-dimensional potential distributions of the PF-CSTBT with various p-floating layers and the conventional IGBT (potential varies by 4 V every line). The depletion region of the p-base/n-drift junction supports the voltage applied to the conventional IGBT, while for the PF-CSTBT, it is the depletion region of the p-floating layer/n-drift junction

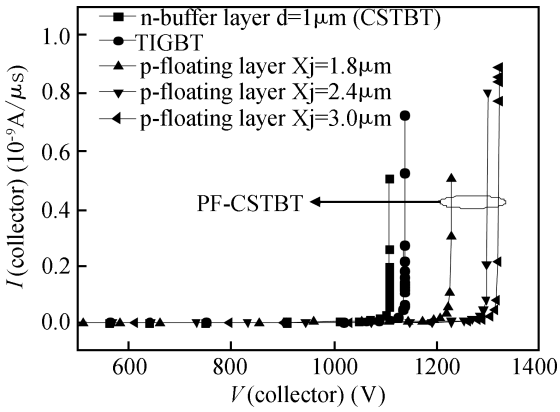

Fig. 5. Breakdown voltage of CSTBT, TIGBT and PF-CSTBT with different p-floating layers.

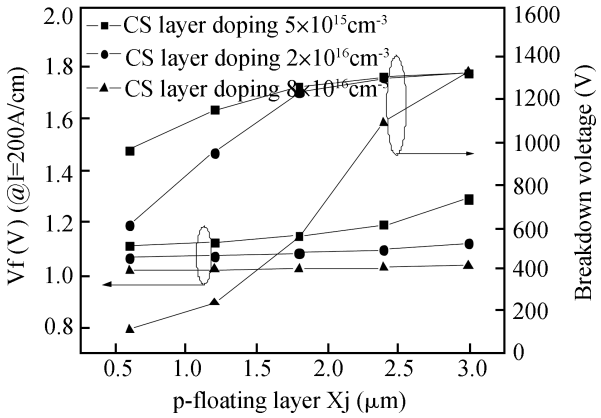

Fig. 7. Characteristics of PF-CSTBT with various p-floating areas and CS layer concentrations.

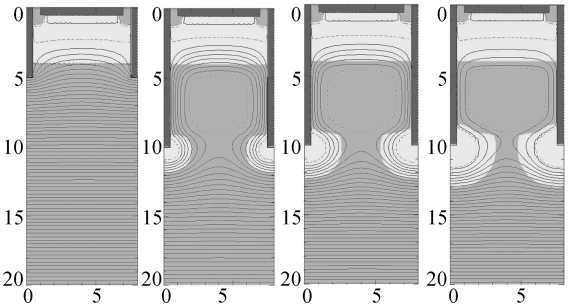

Fig. 6. Potential distribution of (a) conventional IGBT and various p-floating layers of PF-CSTBT [(b) X_j= 0.6, (c) X_j = 1.8, (d) X_j = 3.0].

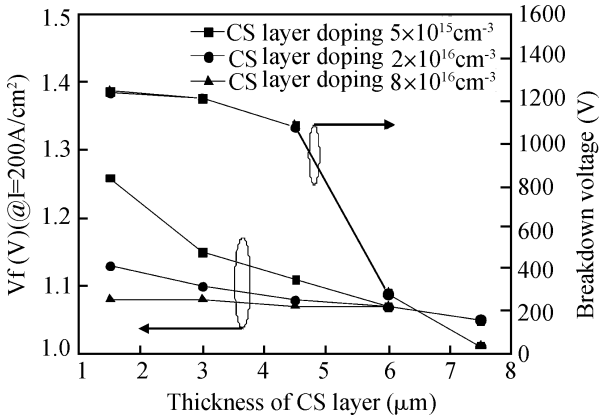

Fig. 8. Characteristics of PF-CSTBT with different thicknesses of CS layers when $X_j = 1.2$ μm.

that supports most of the voltage. As the p-floating layer area enlarges, the p-base bottom supports less voltage. In spite of the application of a thicker and more highly doped CS layer, the CS layer scarcely depletes or supports high voltage under the protection of the p-floating layer. So, none of the over high electrical field influencing the breakdown voltage will emerge here. As shown in Fig. 6, when the p-floating layer deepens to 3 μm, the area above this layer supports voltages as low as 12 V, and the forward voltage drop still decreases compared to the conventional IGBT as shown in Fig. 3.

3.3. Comparison

If the area of the p-floating layer is relatively small, its ability to stop electrical field becomes reduced. In this case, the breakdown voltage slumps sharply with increasing CS layer doping, although a slight decrease in the forward voltage drop can also be observed. Under such circumstances, the breakdown voltage, therefore, relates strongly to the doping of the n-type CS layer. However, with the enlargement of the p-floating layer, the correlation between breakdown voltage and CS layer doping is weakened. As the p-floating layer deepens, as shown in Fig. 7, the breakdown voltage climbs up to about 1320 V (200 V higher than the TIGBT) even when the CS layer concentration rises from 5×10^{15} cm^{-3} to 8×10^{16} cm^{-3}. On this occasion, the breakdown voltage is greatly affected by the p-floating layer rather than the CS layer. Moreover, for a relatively lightly doped CS layer, enlargement of the p-floating layer prompts the forward voltage drop to increase faster, mostly resulting from the more remarkable JFET effect.

With increasing CS layer depth, the forward voltage drop is reduced, especially when CS layer doping is low. However, the breakdown voltage is greatly affected when the thickness of the CS layer is more than 4.5 μm, as shown in Fig. 8. The results are obtained under conditions with the same p-floating layer (junction depth $X_j = 1.2$ μm).

Considering the practical difficulty in processing large p-floating layer areas, PF-CSTBT cell size can be reduced. In this case, even a relatively small p-floating layer can fully stop the electrical field and cause the breakdown voltage to increase. At the same time, a great decline in the forward voltage drop can also be achieved.

4. Conclusion

By analyzing the merits and disadvantages of the conventional IGBT, CSTBT and P-FIGBT, a new IGBT—a PF-CSTBT with a p-floating layer and a more effective CS layer—is proposed to achieve a lower forward voltage drop and higher breakdown voltage, while the short circuit current ability remains compatible with the conventional IGBT. Simulation results indicate that the forward voltage drop of this new IGBT decreases by about 20% and 17% respectively when compared with the TIGBT and CSTBT, and the blocking

capability is improved by about 200 V, while the SCSOA is not negatively influenced.

References

[1] Baliga B J. Power semiconductor devices. Boston: Boston PWS Publishing Company, 1996

[2] Takahashi H, Haruguchi H, Hagino H, et al. Carrier stored trench-gate bipolar transistor (CSTBT)—a novel power device for high voltage application. ISPSD, 1996: 349

[3] Kang X, Lu L, Wang X, et al. Characterization and modeling of the LPT CSTBT—the 5th generation IGBT. 38th IAS Annual Meeting, 2003: 982

[4] Lee J S, Shin H H, Lee H S, et al. The effect of a shielding layer on breakdown voltage in a trench gate IGBT. ICPE, 2007: 62

[5] Hwang S J, Yu S W, Lee J I, et al. Use of the p-floating shielding layer for improving electric field concentration of the recessed gate. ICICDT, 2008: 13

[6] Medici User's Manual. Avant! Corporation, 2004

[7] Yuan X, Udrea F, Trajkovic T, et al. Enhanced on-state performance trench IGBT with a self-aligned p base. Thirty-Sixth IAS Annual Meeting, 2001: 1033

[8] Nakamura K, Oya D, Saito S, et al. Impact of an LPT(II) concept with thin wafer process technology for IGBT's vertical structure. ISPSD, 2009: 295

[9] Nakamura K, Hisamoto Y, Matsumura T, et al. The second stage of a thin wafer IGBT low loss 1200 V LPT-CSTBT^{TM} with a backside doping optimization process. ISPSD, 2006: 1