A flexible logic circuit based on a MOS-NDR transistor in standard CMOS technology*

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Abstract: A MOS-NDR (negative differential resistance) transistor which is composed of four n-channel metal–oxide–semiconductor field effect transistors (nMOSFETs) is fabricated in standard 0.35 μm CMOS technology. This device exhibits NDR similar to conventional NDR devices such as the compound material based RTD (resonant tunneling diode) in current–voltage characteristics. At the same time it can realize a modulation effect by the third terminal. Based on the MOS-NDR transistor, a flexible logic circuit is realized in this work, which can transfer from the NAND gate to the NOR gate by suitably changing the threshold voltage of the MOS-NDR transistor. It turns out that MOS-NDR based circuits have the advantages of improved circuit compaction and reduced process complexity due to using the standard IC design and fabrication procedure.

Key words: MOS-NDR; CMOS; resonant tunneling diode; monostable-bistable transition logic element ; flexible logic gate

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1. Introduction

With silicon VLSI technology approaching the limits of scaling and miniaturization, new device technologies and systems are under investigation for improved speed and circuit compaction. Among the most promising are functional devices and circuits based on negative differential resistance (NDR). The NDR characteristics are ideally suited for the design of highly compact, self-latching logic circuits[1]. Applications based on the NDR device-resonant tunneling diode (RTD) such as oscillators[2], D flip-flops[3], adders[4] and majority gates[5] have attracted considerable attention in recent years. However, the high-cost, complicated process and inconsistent device performance due to the use of III–V compound semiconductor materials form the main obstacle to the further application of NDR devices. To solve these problems, a novel device-MOS-NDR transistor which is composed of metal–oxide–semiconductor field effect transistor (MOSFET) devices is proposed[6] to emulate the I–V characteristics of the conventional NDR device. Based on such a device, a flexible logic gate utilizing a monostable-bistable transition logic element (MOBILE) mechanism is realized in this paper. The flexible logic gate incorporates NAND and NOR functions into the same circuit configuration and considerably reduces the complexity of the circuit. Most importantly, the use of sophisticated EDA tools to design and simulate the desired device characteristics in advance, and mature standard CMOS technology to fabricate the device guarantee the good performance and uniformity of the device, thus it is more suitable for monolithic integration and mass-production.

2. Design of the MOS-NDR transistor

The MOS-NDR transistor, which is derived from an N-type negative resistance topology described in Ref. [6], is composed of four nMOSFETs. Its configuration and corresponding device symbol are shown in Figs. 1(a) and 1(b), respectively. C and E are the two terminals of the NDR device, and B as the third terminal can be connected either to a fixed voltage or tunable voltage. This MOS-NDR device can exhibit various NDR I–V characteristics by suitably changing the MOSFETs' parameters. The width to length ratios (W (μm) / L (μm)) of MN1, MN2, MN3 and MN4 used here are 15/0.5, 10/0.5,

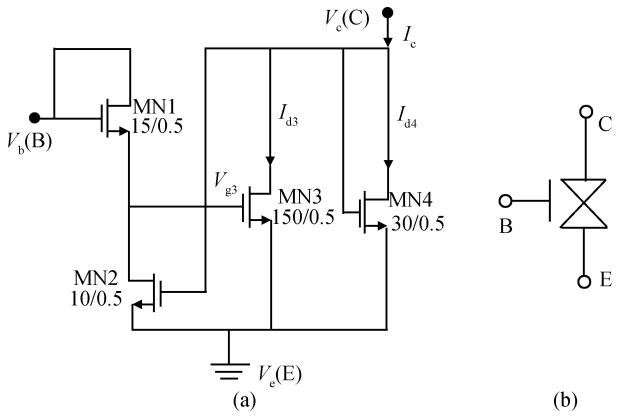

Fig. 1. MOS-NDR transistor. (a) Circuit configuration. (b) Symbol.

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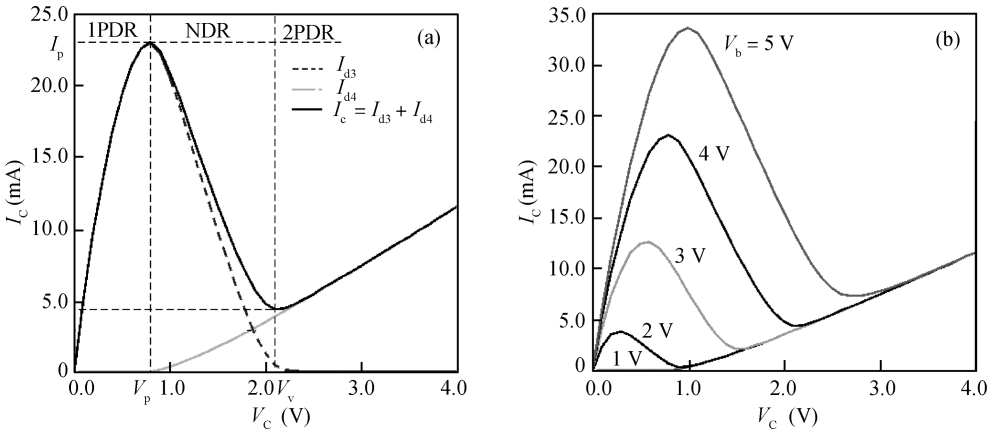

Fig. 2. Simulated I–V characteristics of the MOS-NDR transistor. (a) I–V characteristics with fixed V_b. V_p: peak voltage, I_p: peak current, V_v: valley voltage, I_v: valley current. (b) Modulated I–V characteristics by the third terminal.

150/0.5 and 30/0.5 respectively, and the turn-on voltage V_T of each nMOSFET is about 0.7 V. The performance of the device is simulated by using Cadence IC simulation tools. Figure 2(a) shows the simulated DC I_C–V_C characteristic when the V_b is fixed. The current of its collector (C) I_C is composed of two current components, i.e. the drain current of MN3 I_{d3} and drain current of MN4 I_{d4}:

$$I_C = I_{d3} + I_{d4}. \tag{1}$$

I_{d3} exhibits λ-type negative resistance, and I_{d4} has exponential characteristics. If the V_b voltage is fixed at some value (more than $2V_T \approx 1.4$ V), the operation of this MOS-NDR device can be divided into three regions in sequence by gradually increasing the bias V_C, namely the first positive differential resistance segment (1PDR), negative differential resistance segment (NDR) and the second PDR segment (2PDR). More details on its working mechanism are described in our previous work[7]. Such a negative resistance feature of the MOS-NDR device is quite similar to the RTD's I–V characteristics which can also be divided into two current components, i.e. resonant tunneling current I_{RT} and extra current I_{EX} (including hot carrier scattering and so on)[8]:

$$I_{RTD} = I_{RT} + I_{EX}. \tag{2}$$

We use I_{d3} to emulate the RTD's I_{RT}, and I_{d4} to emulate the RTD's I_{EX}.

When V_b is varied, modulation of the peak current can be realized. This obviates the necessity for the extra nMOSFET connected with the MOS-NDR device in parallel to modulate the peak current. If V_b is not large enough to make the gate voltage of MN3 V_{g3} more than V_T (≈ 0.7 V), there will be no NDR effect in the I_C–V_C curve with the increase of V_C. If V_b is large enough (say more than $2V_T$), then the modulation effect appears. The V_b's modulation characteristics are shown in Fig. 2(b), from which we can see that when V_b increases from 0 to 5 V, the I_C–V_C curve can take on different characteristics. According to our simulation, the change of I_p's magnitude is almost linearly proportional to that of V_b.

The MOS-NDR transistor is fabricated in a standard 0.35 μm 3.3/5 V CMOS process provided by Chartered technology. The characteristics of the fabricated MOS-NDR transistor are tested by using a digital device characterization system, Keithley 4200, as illustrated in Fig. 3, in which the x axis represents voltage V_C, the y axis is current I_C, and the I_C–V_C characteristics can take on different forms due to the variation of the tunable voltage V_b. A maximum PVCR (peak to valley current ratio) of 10 : 1 can be achieved, which is favorable for the application as a switch. The turn-on voltage of this device approximates 0 and the peak voltage is kept within 0.7 V. From the above analysis we can see this device shows good negative differential resistance characteristics. The overall feature of the tested I–V characteristics is in good agreement with the simulated results, except that there are plateau-characteristics at the NDR region in the tested device, the reason for which is not clearly known, and more research work needs to be done to explain it.

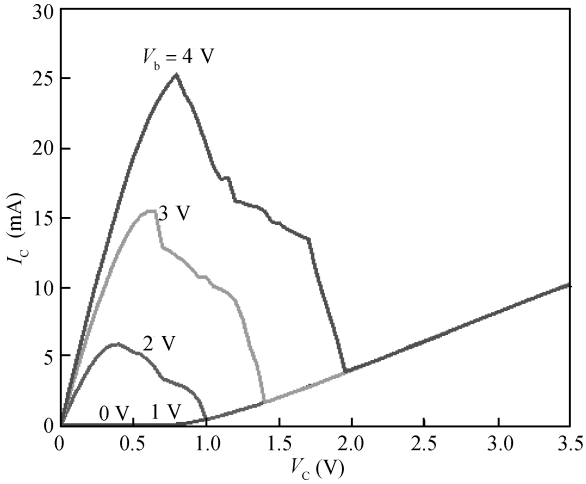

Fig. 3. Tested I–V characteristics of the MOS-NDR transistor.

3. Flexible logic based on the MOS-NDR transistor

NDR devices have wide applications in the analog and digital domains, and they take a different avenue from conventional CMOS circuits. The fundamental mechanism behind most of these applications is monostable-bistable transition logic ele-

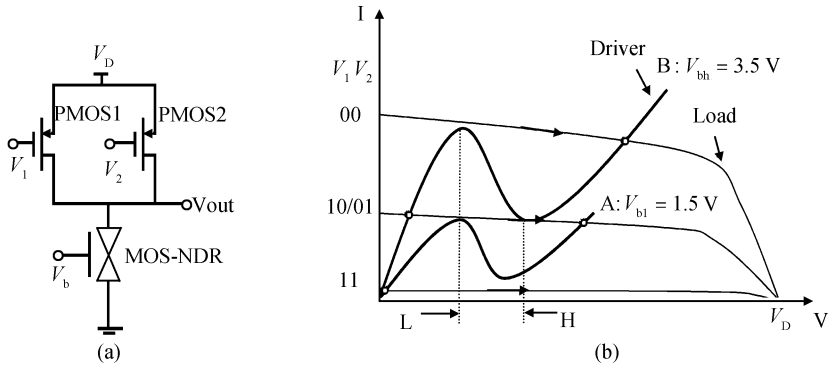

Fig. 4. Flexible logic. (a) Circuit configuration. (b) Working mechanism.

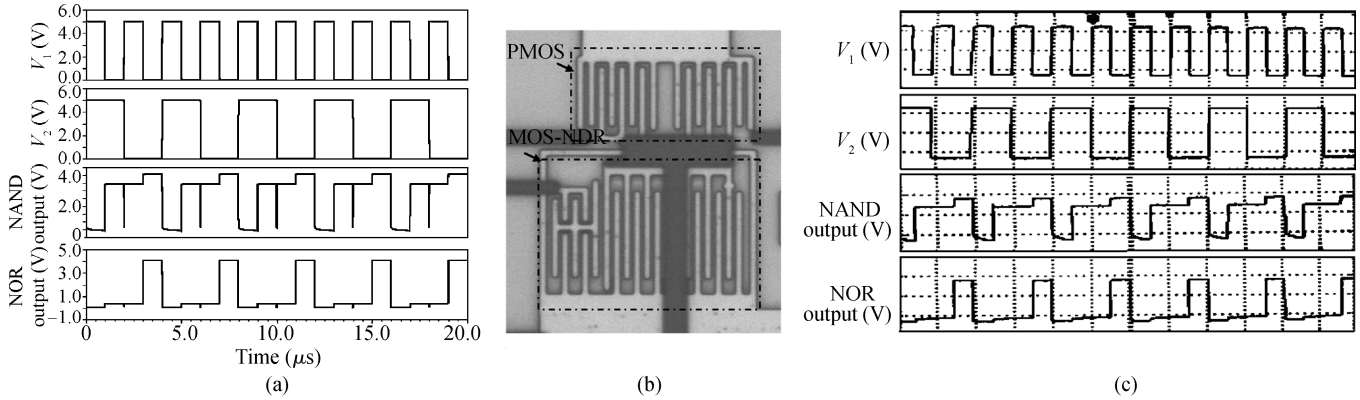

Fig. 5. Flexible logic circuit. (a) Simulated result of the circuit (NAND and NOR gates). (b) Microphotograph of the circuit. (c) Tested result of the circuit (NAND and NOR gate) (x: 500 μs/div; y: 2 V/div).

ment (MOBILE) theory derived from negative differential resistance[9]. Based on this mechanism we use a MOS-NDR transistor and two pMOSFET devices to constitute a flexible logic gate, which is capable of NAND and NOR functions by suitably changing the threshold voltage V_b. The circuit configuration and its working mechanism is shown in Fig. 4.

Figure 4(a) shows the circuit structure: the MOS-NDR device is used as the driver instead of the load to eliminate floating bias (because if the MOS-NDR works as the load , the voltage between B and E of MOS-NDR changes with V_{out}) , and two pMOSFETs (each with W/L = 50 μm/0.5 μm) work as the load. Compared with structure in Ref. [10], the complexity of this circuit is even reduced. When V_D (say 5 V) is larger than V_v of the MOS-NDR transistor, there are two possible operating points (so called bistable) corresponding to low and high states positioned at the 1PDR and 2PDR regions, respectively. The stable operating point can be determined by the intersection point of two I–V characteristics with the load line analysis method, as shown in Fig. 4(b). The driver's I–V characteristics with different V_b are in the forward direction of the X axis, typically A and B curves, and the load's I–V curve is in the reverse direction. When the load's current I_{load} rises from 0 mA, the operating point is at the 1PDR region in the first place and the output is in the low state. Then when the load's current continues to increase to a point higher than the MOS-NDR's (driver) peak current I_p, the operating point jumps from the 1PDR to the 2PDR, and V_{out} changes from low state to high state. This can be described as:

$$\text{If } I_{load} > I_p \text{ , then } V_{out} = L \rightarrow H. \tag{3}$$

An inverter can be easily realized in this way. In our case:

$$I_{load} = I_{D1}(V_1) + I_{D2}(V_2),\ V_1V_2 = 00/10/01/11. \tag{4}$$

Here $I_{D1}(V_1)$ and$I_{D2}(V_2)$ are the current through PMOS1 and PMOS2, respectively, and the input value of V_1V_2 is 0 for low level (0 V), 1 for high level (V_D). The output voltage level is a little different from the input, so "H" and "L" represent high level and low level respectively. If we suitably choose the driver's peak current I_p by modulating the MOS-NDR's third terminal V_b, then the logic function can be changed, as described as follows:

$$\begin{cases} \text{NAND: only if } V_1V_2 = 11, \\ \quad I_{D1}(V_1) + I_{D2}(V_2) < I_p(V_{bl}) \text{ and } V_{out} = L; \\ \text{NOR: only if } V_1V_2 = 00, \\ \quad I_{D1}(V_1) + I_{D2}(V_2) > I_p(V_{bh}) \text{ and } V_{out} = H. \end{cases} \tag{5}$$

When $V_b = V_{bl}$ (e.g. 1.5 V for this circuit), NAND logic is realized, and when $V_b = V_{bh}$ (e.g. 3.5 V for this circuit), NOR logic is realized. The design process is also aided by the Cadence IC design tools, and the simulated NAND and NOR logic functions are shown in Fig. 5(a). A microphotograph of the fabricated circuit is shown in Fig. 5(b) and the total area of this circuit is about 30×44 μm^2. The tested transient response of the circuit is shown in Fig. 5(c). It turns out that the test

results have good agreement with our simulation. This circuit incorporates NAND and NOR functions into one circuit structure, thus considerably diversifying the function of the conventional logic circuit and at the same time reducing the circuit complexity.

4. Conclusions

The implementation of a MOS-NDR transistor in standard CMOS technology is demonstrated in this paper. Based on such a device, a flexible logic gate which incorporates NAND and NOR gates into the same circuit configuration is realized. Although device area and circuit power dissipation are not best optimized and there is much room left for improvement, from this demonstration we can see that MOS-NDR based circuits enable use of sophisticated EDA tools and mature planar silicon CMOS technology, thus the performance of the circuit is predictable and guaranteed. Compared with all III–V compound material based RTD, the MOS-NDR transistor is more suitable for large-scale monolithic integration with a CMOS circuit and is promising for more complex and compact systems on a chip (such as cellular neural networks[11]). Thus it can considerably extend the scope of CMOS circuits into new areas.

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