Novel multi-bit non-uniform channel charge trapping memory device with virtual-source NAND flash array*

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Abstract: In order to overcome the bit-to-bit interference of the traditional multi-level NAND type device, this paper firstly proposes a novel multi-bit non-uniform channel charge trapping memory (NUC-CTM) device with virtual-source NAND-type array architecture, which can effectively restrain the second-bit effect (SBE) and provide 3-bit per cell capability. Owing to the n^- buffer region, the SBE induced threshold voltage window shift can be reduced to less than 400 mV and the minimum threshold voltage window between neighboring levels is larger than 750 mV for reliable 3-bit operation. A silicon-rich SiON is also investigated as a trapping layer to improve the retention reliability of the NUC-CTM.

Key words: multi-bit storage; non-uniform channel; charge trapping memory; NAND array; SiON layer
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1. Introduction

Recently, with the continuous increase in mass data storage applications, NAND-type flash memory has been paid much more attention owing to its merits in high density and fast programming throughput[1]. Multi-level cell (MLC) technology[2], which makes a single cell store n-bit information by controlling the amount of stored charge divided into 2^n levels, has been introduced to increase the storage density in conventional floating-gate NAND-type flash memories. However, with the storage bit number increasing and cell size shrinking, the threshold voltage (V_t) window between neighboring levels and the stored charges will decrease dramatically, resulting in serious reliability challenges for 3-bit or 4-bit storage real application[3, 4].

Owing to its immunity to the inter-cell coupling effect, nitride-based charge trapping memory (CTM) shows better scalability and promises two-bit-per-cell storage capability, such as NROM or Mirror-bit in previous work[5]. Moreover, a method combining the said mirror-bit and 2-bit-MLC to achieve four-bit storage, defined as a multi-bit cell (MBC) in this paper, is reported to enlarge the inter-level V_t window[6]. However, the second-bit effect (SBE), which comes from the commutative disturbance between the pair of bits during program or read operations, may cause the asymmetry of the two physical bits and further narrow the small V_t window in the MBC[7, 8], resulting in serious reliability issues. Moreover, the previous MBC technology also has great bottle-necks for cell size shrinking. Because it adopts the channel-hot-electron-injection (CHEI) mechanism to perform program operation, the high programming VDS voltage restricts the channel length scaling down, and the large programming current limit is only realized in parallel array architecture, resulting in a large cell size.

This paper firstly proposes a multi-bit non-uniform channel charge trapping memory device with virtual-source NAND-type array architecture, which can effectively restrain the second-bit effect and provide a larger V_t window. As a result, MBC technology can easily be introduced into this device so as to realize 3-bit or 4-bit per cell capability. The device uses band-to-band tunneling hot holes injection (BBHH)/channel FN to program/erase respectively. It therefore has low program current and is suitable for structures such as high density NAND arrays.

2. Structure and operation principle of NUC-CTM

Figure 1 shows the structure of the proposed CTM device with a non-uniform channel. There are two p-type channel regions near the source and drain, and one n^--type buffer region in the middle. Therefore, two storage nodes, bit-A and bit-B, can be located above the two physical channels, respectively, to intrinsically realize 2-bit storage. Some key parameters of the fabricated NUC-CTM device are listed in Table 1, with the gate length and the p-type channel length being about 0.35 μm and 60 nm, respectively. The n^--type buffer region is formed by As-implantation before the gate stack formation, and the p-type channel region is formed by tilted boron implantation subsequently. It needs to be pointed out that the physical channel length and gate length can be shrunk to below 35 nm and 100 nm, respectively, by carefully controlling the fabrication condition. Simulation results show that the gate length of NUC-CTM can scale down to 60 nm by adjusting the p-channel and n^--type buffer region width and doping, as shown in Fig. 2.

The proposed NUC-CTM uses BBHH and channel FN to perform program and erase operations, respectively. In order to illuminate the operation principle, 2D device simulation is used to simulate the surface potential in the program and read oper-

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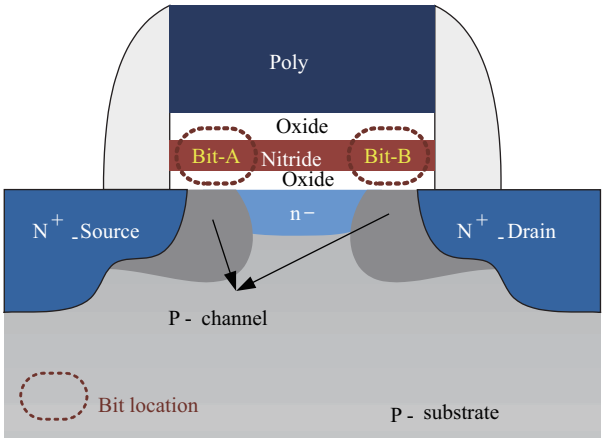

Fig. 1. Structure of a single NUC-CTM cell.

Table 1. Key parameters of the fabricated NUC-CTM device.

Parameter	Value
Gate length (μm)	0.35
Channel width (μm)	0.6
Channel length (nm)	$\sim$ 60
Bottom oxide thickness (nm)	4.5
Si-rich SiON thickness (nm)	8
Block oxide thickness (nm)	6
P-channel doping (cm^{-3})	$\sim 2\times10^{18}$
n^- -buffer region doping (cm^{-3})	$\sim 6\times10^{17}$
Gate material	N^+-poly gate

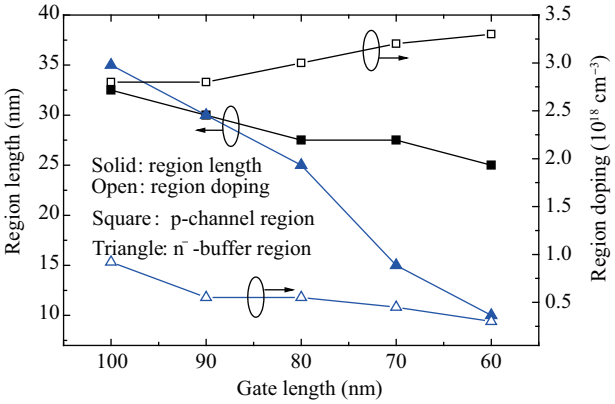

Fig. 2. Simulation results of scalability of NUC-CTM. The gate length can scale down below 60 nm by carefully controlling the length and doping of the p-channel region and the n^--type buffer region.

ations. Figure 3(a) shows the program operation with source side holes injection. The source side was applied on a positive voltage V_{source} while the gate was applied on a negative voltage V_{gate}. The hot holes were generated near the overlap of the source and gate since the high electric field. Owing to the high negative voltage V_{gate}, some of these holes were locally injected into the SiON layer at the source side to lower the surface potential, and then cause a source side negative local V_t shift (ΔV_s). Figure 3(b) shows the read operation, wherein a reverse read voltage (V_{read}) is applied on the drain side to lower the surface potential of the drain side p-type region, so that the ΔV_s can be sensed. During the channel FN erase operation, the

Table 2. Operation condition of the MC-1 cell in the VS-NAND array.

	Erase	Program		Read	
		Bit-A	Bit-B	Bit-A	Bit-B
BL0	0	0	7	3	0
BL1	0	7	0	0	3
BL2	0	0	0	0	Floating
$BSeL_0$	0	10	0	6	6
WL_0	16	10	0	6	6
WL_1	16	–10	–10	V read	V read
⋮					
WL_{15}	16	0	10	6	6
$GSeL_0$	0	0	10	6	6
$GSeL_1$	0	0	0	0	0
WL_{16}	16	0	0	0	0
⋮					
WL_{30}	16	0	0	0	0
WL_{31}	16	0	0	0	0
$BSeL_1$	0	0	0	0	0

gate was applied on a high positive voltage, so FN tunneling happened and some electrons would inject into the SiON layer to neutralize the electrons to performance erase operation. The drain side bit-B could be programmed and read by exchanging the bit-line voltage, and then realize 2-bit storage operation.

The n^- -type buffer region plays an important role in the operations for the NUC-CTM device: (1) the n^--type region lowers the surface potential in the middle of the channel, so the local V_t shift caused by holes injected at the source/drain side can be easily read out completely, providing a larger V_t window; (2) the depletion channel formed by the n^--type buffer region can isolate the interaction of the two physical bits, providing a smaller second bit effect and better reliability.

Like other MBC structures, the reverse read scheme[5] is inevitable to enlarge the V_t window for the proposed NUC-CTM device. Therefore a novel virtual-source NAND array architecture (VS-NAND), in which the source-line is merged with the neighboring bit-line, is also proposed in this paper. As shown in Fig. 4(a), the VS-NAND array forms a symmetrical architecture for the source and drain operations, making the two bits operation feasible in the array level. Figure 4(b) shows the top-view layout of the VS-NAND structure. The operation conditions of the VS-NAND array are given in Table 2. When selects bit-A in the selected cell MC-1 to perform a program operation, for example, a 7 V programming voltage on the BL1 is transferred to the drain of MC-1 through the 10 V biased selection transistor BSeL0 and WL0, and –10 V gate voltage is biased on the selected WL1, injecting holes into the nitride at the region of bit-A through the BBHH mechanism[9]. In read operation, a 3 V read voltage VBL0 is transferred to the source of MC-1 through the 6 V biased selection transistor GSeL0 and WL2–15 to lower the barrier and screen the blocking effect of bit-B. The n^- buffer region can help to turn on the region uncontrolled by the barrier lowering effect from the source side, and screen the disturbance of the two pair-bits.

3. Experimental results and discussion

3.1. Restrain on second-bit effect

The program/erase characteristic of the NUC-CTM is shown in Fig. 5. The V_t was defined as the word-line voltage

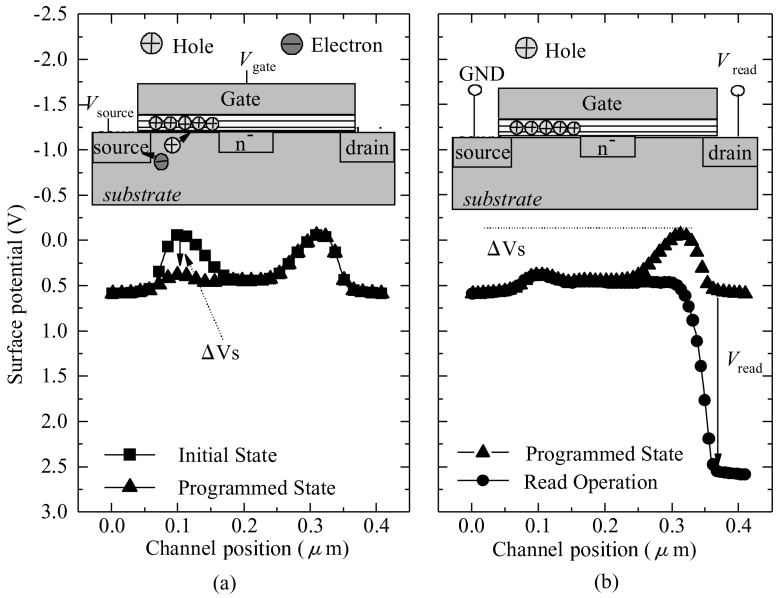

Fig. 3. (a) Source-side program and (b) source-side read operation principle of the NUC-CTM cell.

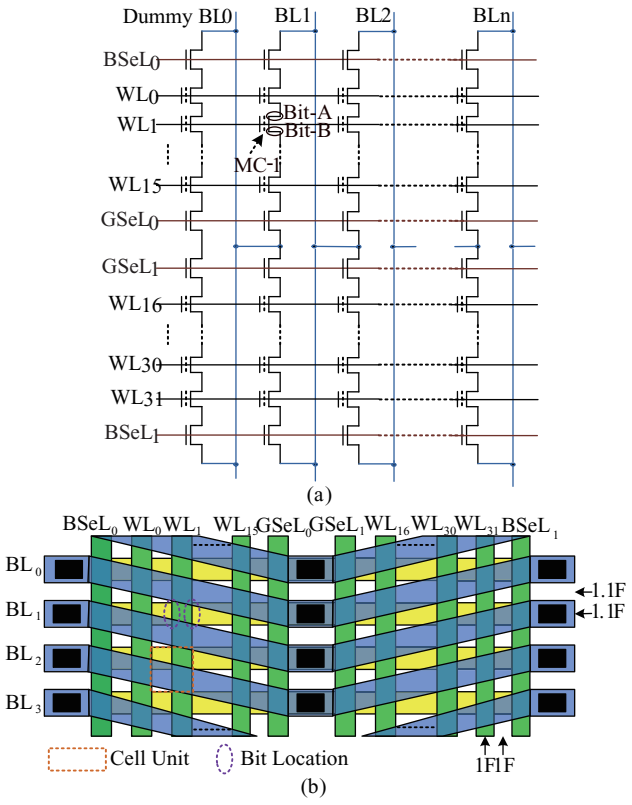

Fig. 4. (a) Schematic diagram of the proposed virtual-source NAND type array structure. (b) Top view layout of the proposed VS-NAND structure.

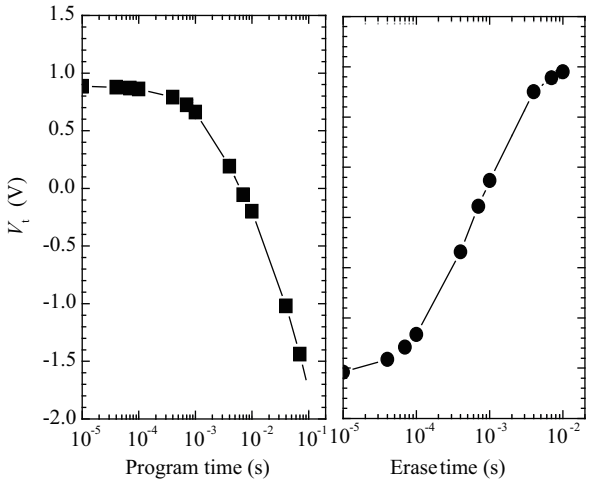

Fig. 5. Program/erase characteristic of the NUC-CTM cell.

when I_{drain} = 1 A. The bit-to-bit interference during program operation is a critical issue in the mirror-bit storage device[5]. The programmed bit would have an impact on the program operation of the other bit. In the NUC-CTM, owing to the BBHH program method, this interference could be well restrained, as shown in Fig. 6. Firstly, bit-A is programmed to a low V_t state and obtains an approximate 2 V V_t window within 30 ms, while bit-B stands stably. Subsequently, bit-B is also programmed to a low V_t state within 30 ms. The matching V_t value after the same program time of bit-A and bit-B indicates the symmetry of program operation in the NUC-CTM. Figure 7 shows the I–V curve of the NUC-CTM with different states of bit-A and bit-B. As described above, in MBC the SBE induced V_t shift plays the most critical limitation to the reliability performance. According to the programming/un-programming state of the pair-bit (bit-A and bit-B in Fig. 1), the SBE between the two pair-bit can be classified into two different cases: SBE on un-programmed bit (SBE-UNP) and SBE on a programmed bit (SBE-PGM). These two kinds of SBE may shrink the V_t window simultaneously[9]. In order to overcome this problem, an n^- buffer region is located at the middle of the uniform channel device to form the NUC-CTM. The potential of the n^- buffer region in the channel is lower than that of two p-halo regions, and can effectively reduce the interference between the two-side bits. Figure 8 clearly shows the SBE-UNP and SBE-PGM

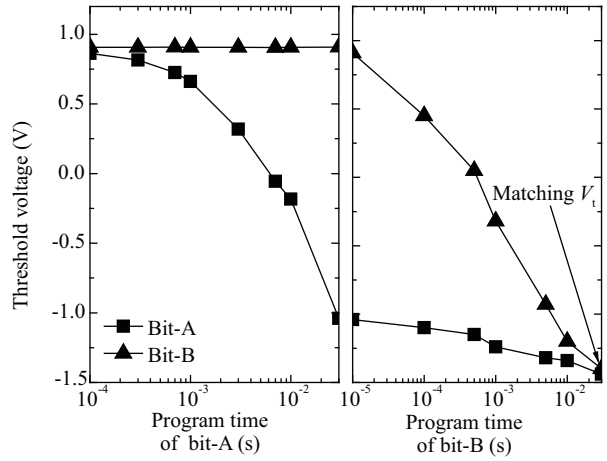

Fig. 6. Restrain on the interference between bit-A and bit-B during program operation.

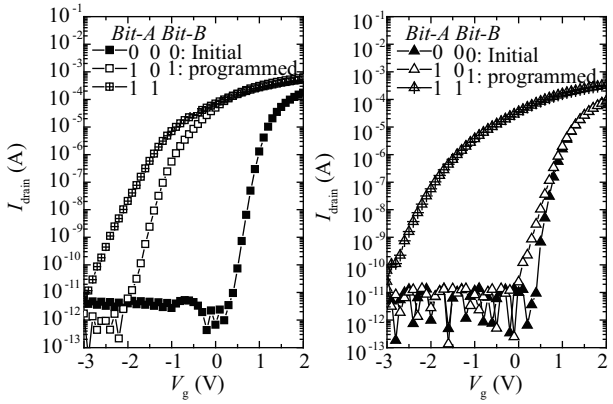

Fig. 7. I_{drain}/I_{source}–V_g curve of the NUC-CTM with different states of bit-A and bit-B.

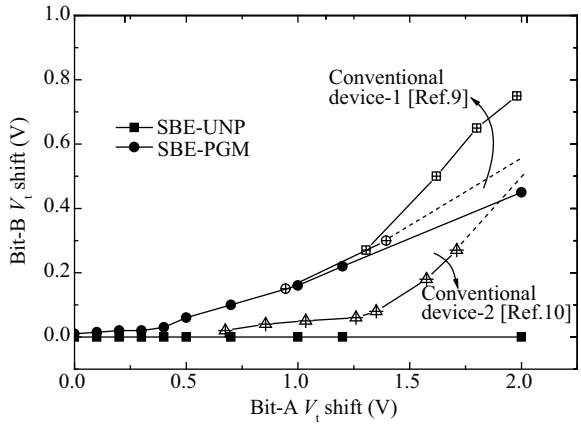

Fig. 8. SBE-UNP and SBE-PGM induced V_t shifts in the NUC-CTM and other mirror-bit storage devices[9, 10].

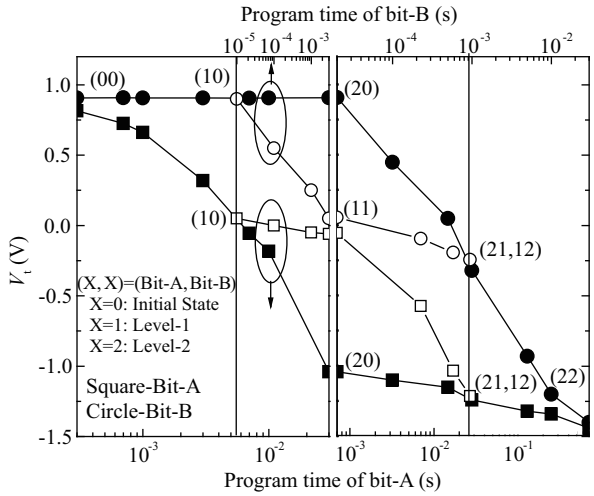

Fig. 9. 3-bit/cell storage characteristic of NUC-CTM and the program speed of each bit.

induced V_t shifts of the NUC-CTM and makes a comparison with the previously reported ones[9, 10]. It is obvious that the SBE-PGM induced V_t shift is higher than the one induced by the SBE-UNP. Owing to the BBHH operation and the isolation effect of the n^- buffer region in the NUC-CTM, the V_t shifts of the un-programmed and programmed bit-B are about 0 mV and 440 mV, respectively, when the bit-A is programmed to a 2 V V_t window. Compared with conventional devices, it can be seen that both the obtained V_t window and the effective V_t window, which is the former one deducting the whole SBE induced V_t shifts, are greatly improved in our device, promising a better chance to realize the multi-level storage for each bit. Figure 9 shows the 3-bit/cell storage characteristic of the NUC-CTM. By carefully controlling the program time, each bit can be separated into 3 states ("0", "1", and "2"). Due to the well restrain on SBE, the minimum V_t window can be larger than 0.75 V.

3.2. Reliability

One of the critical problems in localized storage devices is the mismatch of injected electrons and holes during program and erase[11]. In the NUC-CTM, since the channel FN erase is along the whole channel, electrons can totally neutralize the injected holes. The high potential of the n^- buffer region can not only reduce the amount of injected electrons in the middle of the channel, but also screen these injected electrons, providing 2.75 V V_t window after 10^4 cycles, as shown in Fig. 10(a). It has been reported that, in a Si_3N_4 trapping layer device, charge losses occur through intra-nitride transport, such as holes lateral movement, because holes have a shallow trap energy in the Si_3N_4 layer[12]. To obtain a better retention characteristic in the NUC-CTM, we developed silicon-rich SiON as the trapping layer as the deeper trap in SiON. The SiON layer was deposited by LPCVD (Si : N : O = 1 : 0.9 : 0.3). Figure 10(b) shows the retention characteristic of the NUC-CTM. A 2.5 V V_t window was expected after 10 years baking at 140 ℃.

4. Conclusion

In this paper, a novel non-uniform channel charge trapping memory device (NUC-CTM) is studied. BBHH and channel FN are respectively used to perform program and erase operations, providing low power consumption. Owing to the n^--region in the middle of the channel, the device can effectively restrain the SBE, thus provides a large enough V_t win-

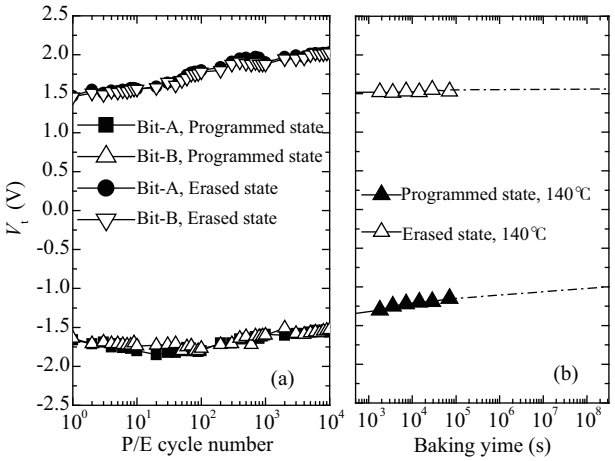

Fig. 10. (a) Endurance and (b) retention characteristic of the NUC-CTM.

dow (about 2 V) for each bit to perform three or four levels (0.75 V for three levels), making the NUC-CTM three-bit or four-bit storage capability. The NUC-CTM also replaced the conventional Si_3N_4 trapping layer with silicon-rich SiON to improve retention reliability. The 2.5 V V_t window remained after 10 years baking at 140 ℃. The low power consumption, large V_t window and excellent reliability makes the NUC-CTM a promising candidate for a sub-100 nm memory device.

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