A curvature calibrated bandgap reference with base–emitter current compensating in a 0.13 μm CMOS process*

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Abstract: In bandgap references, the effect caused by the input offset of the operational amplifier can be effectively reduced by the utilization of cascade bipolar junction transistors (BJTs). But in modern CMOS logic processes, due to the small value of β, the base–emitter path of BJTs has a significant streaming effect on the collector current, which leads to a large temperature drift for the reference voltage. To solve this problem, a base–emitter current compensating technique is proposed in a cascade BJT bandgap reference structure to calibrate the curvature of the output voltage to temperature. Experimental results based on the 0.13 μm logic CMOS process show that the reference voltage is 1.238 V and the temperature coefficient is 6.2 ppm/℃ within the range of −40 to 125 ℃.

Key words: bandgap reference; CMOS; BJT; base current compensating
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1. Introduction

In most modern analog and mixed signal integrated circuits (IC), a voltage/current reference is an indispensable and basic element. Although there are various structures of references, most of them are based on compensating between different elements that have either a positive or a negative response to temperature[1−6]. Among them, the most popular architecture is the bandgap reference (BGR), which is compatible with major CMOS processes.

Different components or circuits have different responses to temperature. The basic structure of a BGR is illustrated in Fig. 1(a). The electromotive force of the PN junction, $V_{\rm BE}$, is inversely proportional to the temperature (Eq. (1)). The voltage difference, $\Delta V_{\rm BE}$, of base–emitter junctions for different bipolar junction transistors (BJTs) is directly proportional to the temperature, on the condition that the collector current densities are different (Eq. (2)). Therefore, an effective way to generate a constant voltage is to merge $V_{\rm BE}$ and $\Delta V_{\rm BE}$, with the temperature T to be counteracted (Eq. (3)). In the following equations, parameter m is the grading coefficient (GC) of the PN junction, n is the ratio of the emitter area in those two BJTs, q is unit electricity, $V_{\rm T}$ is thermal voltage, $E_{\rm g}$ is the bandgap energy of silicon, $I_{\rm S}$ is the saturation current, R_0 and R_1 are the compensated resistors, and α_1 and α_2 are coefficients for compensating. Because the voltage $V_{\rm REF}$ equals the bandgap voltage of silicon when the temperature is absolute zero, this structure is also called a BGR.

$$\frac{\partial V_{\rm BE}}{\partial T} = \frac{V_{\rm BE} - (3+m)V_{\rm T} - E_{\rm g}/q}{T}, \tag{1}$$

$$\begin{aligned}\Delta V_{\rm BE} &= V_{\rm BE0} - V_{\rm BE1} = V_{\rm T}\ln\frac{I_{\rm C0}}{I_{\rm S}} - V_{\rm T}\ln\frac{I_{\rm C1}}{I_{\rm S}} \\ &= V_{\rm T}\ln n = \frac{kT}{q}\ln n,\end{aligned} \tag{2}$$

$$V_{\rm REF} = \alpha_1 V_{\rm BE2} + \alpha_2 \Delta V_{\rm BE(0-1)} = V_{\rm BE2} + \frac{R_1}{R_0}V_{\rm T}\ln n. \tag{3}$$

As is well known, the reference plays an essential role in the whole circuit, and any variation in the reference greatly influences the circuit's stability. Unfortunately, numerous factors can affect the stability of the reference, including the offset of the transistor, the offset of the operational amplifier (OPA), the mismatch of current sources and the noise of the power supply. Many studies have focused on depressing the temperature coefficient (TC) of the BGR. A buck voltage transfer cell was utilized in Chen's work to provide high order compensating, and the power supply rejection ratio (PSRR) was improved with cascode current sources[3]. Hoon[4] provided a subtractor circuit to improve the PSRR, by merging the noise of power supply with the feedback loop. Xing[6] provided a current mode structure to improve the TC with high order compensating.

Numerous factors can increase the TC of the BGR, two of which are most noteworthy. One factor is the input voltage offset of the OPA, $V_{\rm OS}$. This offset, which makes Eq. (3) untenable, cannot be completely avoided. The other is the base–emitter current in the BJTs. For most CMOS processes, the amplificatory multiple β of the substrate BJT is not big enough to make the difference between collector current and emitter current ignorable, thus making Eq. (2) untenable.

This paper focuses on solving these two problems discussed above. The structure of a BGR with cascade BJTs, which can reduce the OPA offset effect on temperature stability of the output voltage, is described; the relation between base–emitter current and TC is discussed; and an adaptive current compensated technique is proposed to solve those two problems of the OPA offset and the base–emitter current effect.

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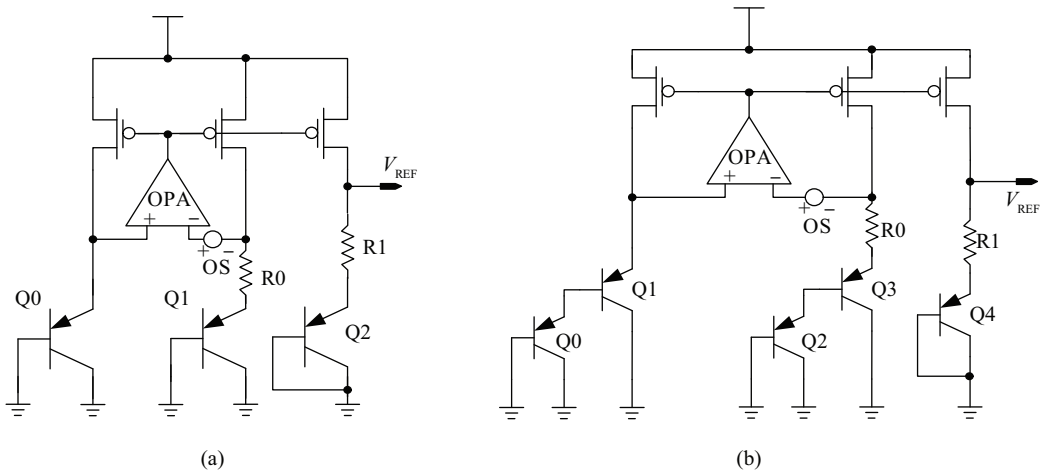

Fig. 1. (a) Typical structure of a bandgap voltage reference and (b) its transformation.

2. BGR structure with cascade BJT

Despite any disturbance caused by other elements, the input offset of the OPA is a key matter in the instability of BGRs. The "imaginary short" property of each input pin of the OPA is essential to Eq. (3). In other words, any input offset will destroy the precondition of Eq. (3). However, the input offset of the OPA cannot be completely avoided, especially when the temperature changes. The offset makes the output of the OPA unpredictable, as does the response of the reference voltage to the temperature. In Jiang's study[7], a relationship between the input offset V_{OS} and the output V_{REF} was analyzed in detail. In Fig. 1 (a), the reference, V_{REF} , is expressed as Eq. (4), in which the input offset V_{OS} of the OPA is considered. The relation between V_{OS} and the temperature depends on the architecture of the OPA and the process. Obviously, there exists some unpredictability in V_{REF}, due to the uncertainty of $\partial V_{OS}/\partial T$.

$$V_{REF} = V_{BE2} + \frac{R_1}{R_0}(\Delta V_{BE} - V_{OS}). \tag{4}$$

According to Eq. (4), there are two ways to enhance the stability of the BGR and reduce the impact caused by V_{OS}. One method is to redesign the OPA and to calibrate it so as to reduce the absolute value of the input offset V_{OS}. The other way is to increase the absolute value of ΔV_{BE}, so as to reduce the ratio of V_{OS} to $\Delta V_{BE} - V_{OS}$, which means the impact caused by V_{OS} will also be reduced. In this work, the second technique is adopted although both methods are widely used.

Based on the above analysis, Equation (4) is transformed into Eq. (5), where λ is the series of cascade PN junctions. The response curvature of V_{REF} to temperature is calibrated, because the ratio of V_{OS} to $\lambda\Delta V_{BE} - V_{OS}$ is depressed. V_{REF} in Eq. (5) is less sensitive to V_{OS} than V_{REF} in Eq. (4).

$$V_{REF} = V_{BE2} + \frac{R_1}{R_0}(\lambda\Delta V_{BE} - V_{OS}). \tag{5}$$

A detailed structure is shown in Fig. 1(b), where λ is equal to 2. The output voltage V_{REF} is given in Eq. (6).

$$V_{REF} = V_{BE2} + \frac{R_1}{R_0}(2\Delta V_{BE} - V_{OS}). \tag{6}$$

Observing Eqs. (5) and (6), a conclusion can be drawn that the more BJTs to be stacked, the lower is the ratio of V_{OS}. This means that the parameter λ is difficult to select. Because of the limitation caused by complexity, power consumption or stack efficiency, the structure of a two layer stack is widely used, which is the case in this paper.

3. Effect on output accuracy caused by base–emitter current

It is a fundamental precondition that the collector current in the two BJTs must be equal[1], which is the necessary condition for Eq. (2). However, because there is a current path from the emitter to the base, which occupies much of the collector current, Q0, Q1, Q2 and Q3 may not have the same collector current at all in Fig.1 (b).

A general scheme is proposed in Fig. 2(a). Two additional current mirrors are employed to ensure that the currents in each down spur track are the same. These current mirrors are shown in the shadow of Fig. 2(a). Nevertheless, since the base–emitter paths separate the collector current, they make the collector current in each BJT no longer equal to each other.

In the logic CMOS process, there is a big difference between the collector current I_c and the emitter current I_e in the substrate BJT, because of the small β value. In Fig. 2(b) we assume two preconditions: the first one is that the emitter area of Q0 is equal to that of Q1, and the same as those of Q2 and Q3; the second precondition is that the emitter area in Q2 and Q3 is M times those of Q0 and Q1. Then a new expression in Eq. (7) can be transformed from Eq. (2),

$$\begin{aligned} 2\Delta V_{BE} &= V_T \ln\frac{I_{c1}}{I_S} - V_T \ln\frac{I_{c3}}{MI_S} + V_T \ln\frac{I_{c0}}{I_S} - V_T \ln\frac{I_{c2}}{MI_S} \\ &= V_T\left(\ln\frac{MI_{c1}}{I_{c3}} + \ln\frac{MI_{c0}}{I_{c2}}\right). \end{aligned} \tag{7}$$

Obviously, since Q1 and Q3 in Fig. 2(b) are working in the linear region, I_{c1} and I_{c3} are β times to I_{eb1} and I_{eb3}. Then the procedure of analysis is shown as follows,

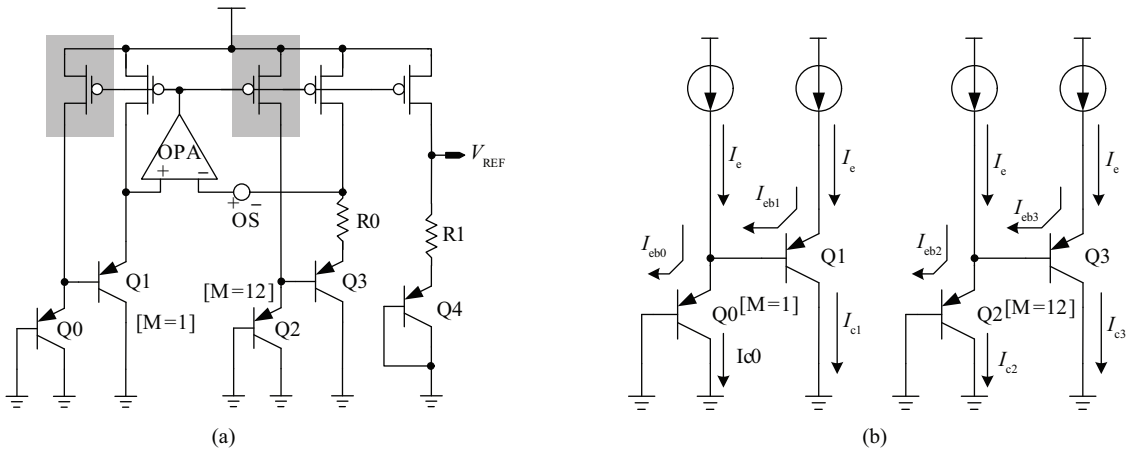

Fig. 2. Error caused by base – emitter current.

$$I_e = I_{c0} + I_{eb0} - I_{eb1} = I_{c1} + I_{eb1} = (\beta + 1)I_{eb1}, \quad (8)$$

$$I_e = I_{c2} + I_{eb2} - I_{eb3} = I_{c3} + I_{eb3} = (\beta + 1)I_{eb3}, \quad (9)$$

$$\begin{aligned} 2\Delta V_{BE} &= V_T \left(\ln M \frac{I_{c1}}{I_{c3}} + \ln M \frac{I_e + I_{eb1} - I_{eb0}}{I_e + I_{eb3} - I_{eb2}} \right) \\ &= V_T \left(\ln \frac{M I_{c1}}{I_{c3}} + \ln M \frac{(\beta+1)I_{eb1} + I_{eb1} - I_{eb0}}{(\beta+1)I_{eb3} + I_{eb3} - I_{eb2}} \right) \\ &= V_T \left(\ln M \frac{I_{c1}}{I_{c3}} + \ln M \frac{I_{c1} - \beta I_{eb0}/(\beta+2)}{I_{c3} - \beta I_{eb2}/(\beta+2)} \right) \\ &= V_T \left(2\ln M + \ln \frac{I_{c1}}{I_{c3}} + \ln \frac{\beta I_e/(\beta+1) - \beta I_{eb0}/(\beta+2)}{\beta I_e/(\beta+1) - \beta I_{eb2}/(\beta+2)} \right) \\ &= V_T \left(2\ln M + \ln \frac{I_{c1}}{I_{c3}} + \ln \frac{(\beta+2)I_e - (\beta+1)I_{eb0}}{(\beta+2)I_e - (\beta+1)I_{eb2}} \right). \end{aligned} \quad (10)$$

Due to the tiny differences between the collector currents of each BJT, the expression in Eq. (2) is no longer precise, and the accurate expression is in Eq. (10). Moreover, the current I_{c1} approximates I_{c3}, so $\ln(I_{c1}/I_{c3}) \to 0$. In this case, a transformation of Eq. (10) is shown in Eq. (11),

$$2\Delta V_{BE} = V_T \left(2\ln M + \ln \frac{(\beta+2)\, I_e - (\beta+1)\, I_{eb0}}{(\beta+2)\, I_e - (\beta+1)\, I_{eb2}} \right). \quad (11)$$

As can be seen, the base–emitter current in the BJTs destroys the necessary condition of Eq. (2), and a new term is introduced into Eq. (3). Thus, V_{REF} will be more accurately expressed by Eq. (12). Comparing Eq. (4) and Eq. (12), a conclusion can be drawn that the impact caused by V_{OS} for the same OPA is reduced remarkably. At the same time, another complex term is imported, which makes the response of V_{REF} to temperature difficult to analyze.

$$\begin{aligned} V_{REF} &= \alpha_1 V_{BE} + \alpha_2 \Delta V_{BE} = V_{BE} \\ &+ \frac{R_1}{R_0} \left\{ V_T \left[2\ln M + \ln \frac{(\beta+2)\, I_e - (\beta+1)\, I_{eb0}}{(\beta+2)\, I_e - (\beta+1)\, I_{eb2}} \right] - V_{OS} \right\}. \end{aligned} \quad (12)$$

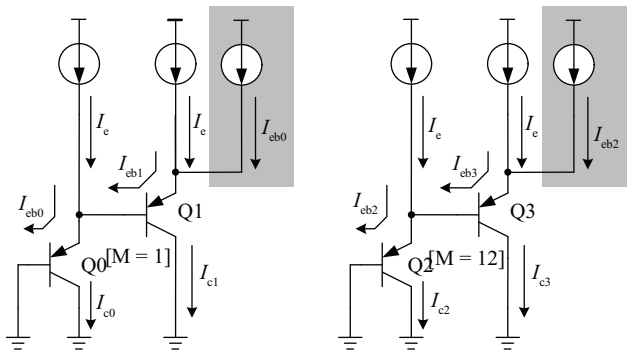

Fig. 3. Base–emitter current compensated.

4. Proposed circuit with base–emitter current compensated

The disturbance on V_{REF} caused by the input offset of the OPA is remarkably reduced with the utilization of cascade BJTs. However, a new unexpected term is imported, which is shown in Eq. (12). Considering the OPA input offset, the ideal expression of the BGR output voltage will be found in Eq. (5). Therefore, a perfect method to remove that unexpected term in Eq. (12) is to have the base–emitter current compensated.

An effective method of compensating is illustrated in Fig. 3, in which the circuits are shadowed. By applying Kirchhoff's current law to each BJT tube, Equations (8) and (9) will be replaced by Eqs. (13) and (14).

$$I_e = I_{c0} + I_{eb0} - I_{eb1} = I_{c1} + I_{eb1} - I_{eb0}, \quad (13)$$

$$I_e = I_{c2} + I_{eb2} - I_{eb3} = I_{c3} + I_{eb3} - I_{eb2}. \quad (14)$$

Based on the simultaneous equations Eqs. (7), (13) and (14), a new expression of $2\Delta V_{BE}$ is given in Eq. (15),

$$\begin{aligned} 2\Delta V_{BE} &= V_T \left(\ln M \frac{I_{c1}}{I_{c3}} + \ln M \frac{I_e + I_{eb1} - I_{eb0}}{I_e + I_{eb3} - I_{eb2}} \right) \\ &= V_T \left(2\ln M + \ln \frac{I_{c1}}{I_{c3}} + \ln \frac{2I_e - I_{c1}}{2I_e - I_{c3}} \right). \end{aligned} \quad (15)$$

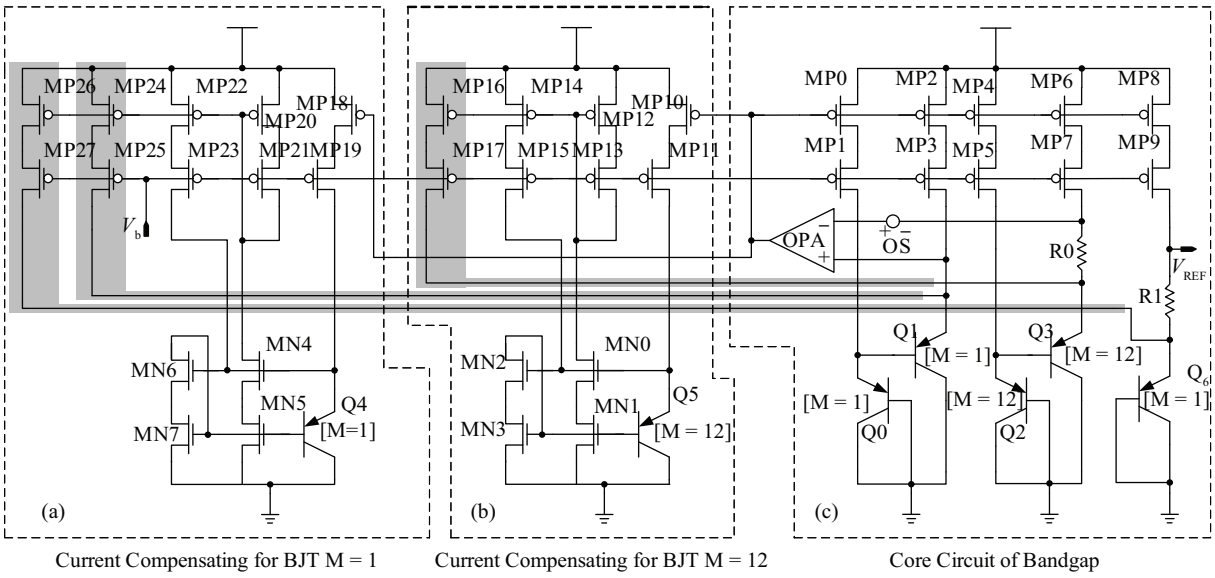

Fig. 4. High precision BGR with base current compensating.

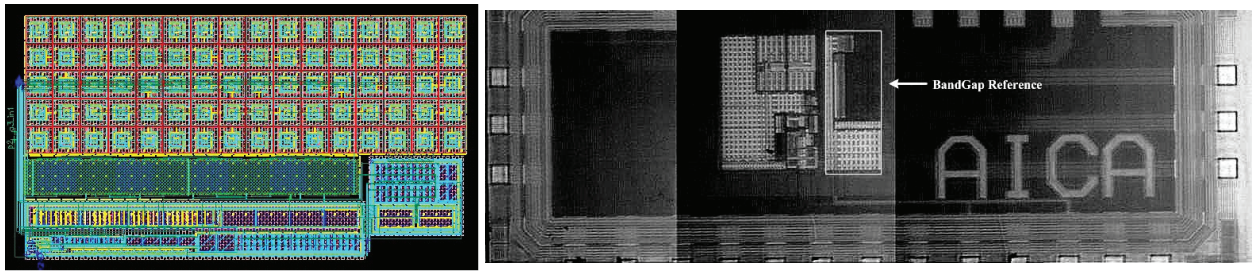

Fig. 5. (a) Layout and (b) chip photo of this work.

The calibrated expression of $V_{\rm REF}$ is illustrated in Eq. (16), which has the unexpected term removed, on the condition that $I_{\rm c1}$ approximates $I_{\rm c3}$. As can be seen, the precise expression of $V_{\rm REF}$ has the same format as the one represented in Eq. (5).

$$V_{\rm REF} = \alpha_1 V_{\rm BE} + \alpha_2 \Delta V_{\rm BE} = V_{\rm BE} + \frac{R_1}{R_0}\left[V_{\rm T}\left(2\ln M\right) - V_{\rm OS}\right]. \tag{16}$$

The novel architecture of the BGR proposed in this paper is shown in Fig. 4, with the startup circuit excluded. The core circuit of the BGR is denoted in Fig. 4(c), which is very similar to the one represented in Fig. 2(a). Cascode PMOS current mirrors are utilized to improve the PSRR, and the impact of $V_{\rm OS}$ on $V_{\rm REF}$ is greatly weakened by the utilization of cascade BJTs.

Only the core circuit in Fig. 4(c) cannot achieve the design goal of Eq. (16). Two additional circuits are appended to adaptively and separately compensate the base–emitter current. These two portions are shown in Figs. 4(a) and 4(b), and the compensating path is shadowed.

Take the circuit in Fig. 4(a) as an example. MN4, MN5, MN6 and MN7 have the base–emitter current $I_{\rm eb4}$ of Q4 mirrored. MP18, MP19, MP22, MP23 and the OPA guarantee identical work states of Q4 and Q0. Based on all the analysis above, the adaptive drain currents of MP25 and MP27 may compensate the current drop of Q1 and Q6. The same is true for MP17 and Q3 in Fig. 4(b). Let M equal 12. Then the output of the whole circuit can be expressed in Eq. (17), with the adaptive compensated technique embedded,

$$V_{\rm REF} = V_{\rm BE6} + \frac{R_1}{R_0}(4.9698 V_{\rm T} - V_{\rm OS}). \tag{17}$$

5. Results of simulation and testing

The test chip was established in a 0.13 μm 1P8M logic CMOS process. A snapshot of the layout (Metal 3 and below) is illustrated in Fig. 5(a). The micrograph of the whole test chip is shown in Fig. 5(b) with the BGR in the white rectangle frame. The area of the BGR circuit is 150×260 μm^2.

The simulation result for the BGR with base–emitter current compensation is illustrated in Fig. 6(a), and that without compensation is presented in Fig. 6(b). Obviously, within the temperature range from –40 to 125 ℃, the BGR compensated by the technique proposed in this article generates a reference voltage of 1.2381 V, its peak to peak value is 1.27 mV, the TC is 6.2 ppm/℃ and the power consumption increases to 370.37 μW @ 50 ℃. In contrast, BGR without compensation generates a reference voltage of 1.2243 V, its peak to peak value is 3.1 mV, the TC is 15.4 ppm/℃ and the power consumption is 220.66 μW @ 50 ℃. In conclusion, the TC of the

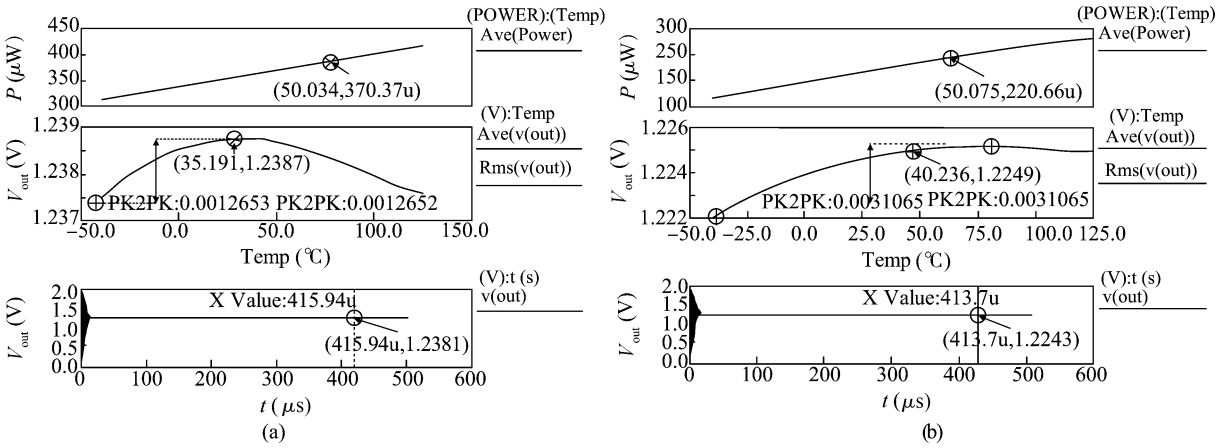

Fig. 6. Curves for voltage versus temperature of the BGR (a) with or (b) without base – emitter current compensation.

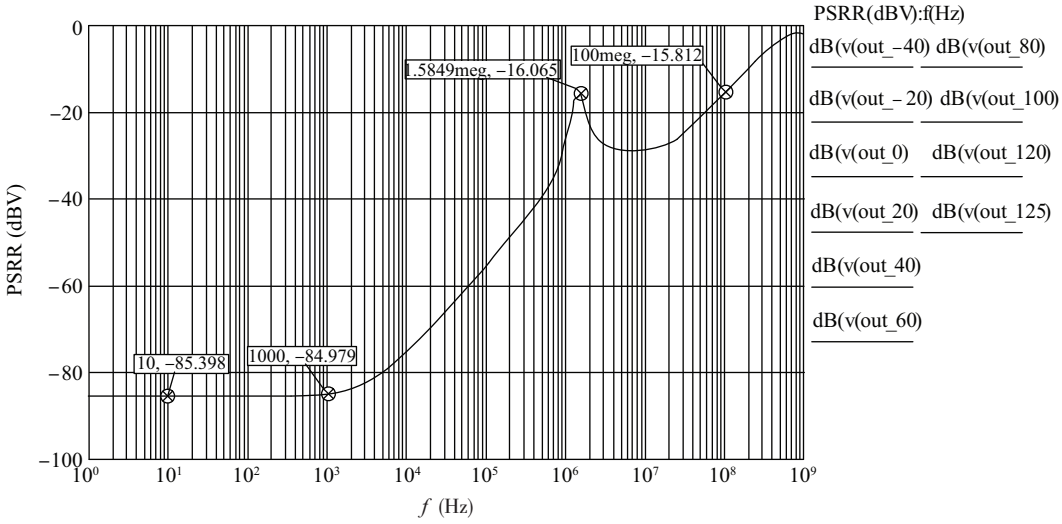

Fig. 7. PSRR curves with different temperatures of the proposed BGR.

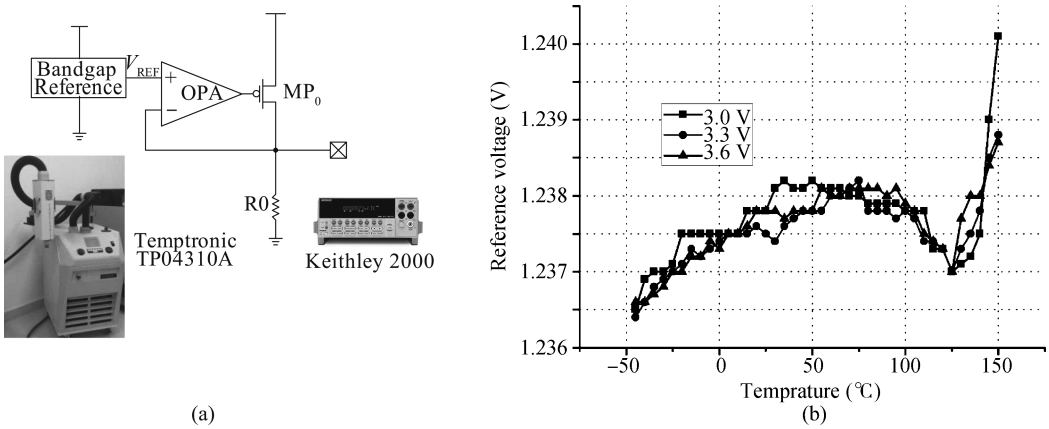

Fig. 8. (a) Test environment and (b) testing result.

BGR is diminished effectively by using the base–emitter current compensated technique proposed in this work, while the reference voltage barely changes. This is called curvature calibration.

The default power supply of this BGR is 3.3 V, but any value from 3 to 5 V is applied. With the utilization of cascode PMOS current mirrors, the power supply rejection (PSR) of the proposed BGR is –85.4 dB in the DC band, and –15.8 dB in the high frequency AC band. The PSRR curves are shown in Fig. 7. From –40 to 125 ℃, the PSRR curves are almost the same.

The reference voltage output does not have the ability to

Table 1. compares results from previous studies with those generated by this work.

Parameter	Ref. [2]	Ref. [3]	Ref. [4]	Ref. [6]	This work*
Process	1.2 μm CMOS	0.5 μm CMOS, Mixed	0.8 μm BiCMOS	0.18 μm CMOS, Mixed	0.13 μm CMOS, Logic
Temperature range (℃)	0–100	–20 to 100	–40 to 125	0–150	–40 to 125
Accuracy	±3%	5.6 ppm/℃	14 ppm/℃	10 ppm/℃	6.2 ppm/℃
Power consumption (μW)	600	Not available	Not available	47	370
Output voltage (V)	1.2	1.196	1.207	0.657	1.238

*Testing conditions: 3.3 V power supply, 55 ℃, ideal workload. And 6.2 ppm/℃ for simulation, 6.8 ppm/℃ for testing, 370 μW for the whole circuit.

load on the drive, nor does the circuit in Fig. 4. In order to test the actual performance of the circuit, a testing structure is built, as shown in Fig. 8(a), by using a high gain OPA, a PMOS transistor, an off-chip resistor, the Temptronic®TP04310A, and a high precision digital multimeter KEITHLEY®2000.

The testing results are described in Fig. 8(b). The power supply is 3.0 V, 3.3 V and 3.6 V. Within the temperature range from –40 to 125 ℃, the output voltage of the test chip migrates in the range 1.2365–1.2382 V, and the value of the TC approximates 6.8 ppm/℃. Compared with the simulation results, the actual measured TC is a little higher, which may be attributed to the influence caused by the test circuit, including the OPA, the PMOS transistor and the resistor. So, the actual TC of the BGR that is proposed in this article should be no greater than 6.8 ppm/℃.

6. Conclusion

A BGR is an essential element for most analog and mixed signal ICs. In this paper, a base–emitter current compensating technique in a BGR with cascade BJTs is proposed. With this technique, the collector current of each BJT in the BGR is greatly stabilized, and the disturbance caused by the input offset of the OPA is also depressed. Furthermore, the TC of the BGR is remarkably decreased, and the curvature of output voltage to temperature is calibrated. A test chip was established in a 0.13 μm 1P8M logic CMOS process. The testing results have shown the reference voltage to be 1.238 V, and the TC is not greater than 6.8 ppm/℃ within the temperature range of –40 to 125 ℃.

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