RF CMOS modeling: a scalable model of RF-MOSFET with different numbers of fingers*

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Abstract: A novel scalable model for multi-finger RF MOSFETs modeling is presented. All the parasitic components, including gate resistance, substrate resistance and wiring capacitance, are directly determined from the layout. This model is further verified using a standard 0.13 μm RF CMOS process with nMOSFETs of different numbers of gate fingers, with the per gate width fixed at 2.5 μm and the gate length at 0.13 μm. Excellent agreement between measured and simulated S-parameters from 100 MHz to 20 GHz demonstrate the validity of this model.

Key words: RF-MOSFETs; scalable model; parasitic components; layout-based
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1. Introduction

The continuous downscaling of complementary metal oxide semiconductor (CMOS) technology has greatly improved the radio-frequency (RF) performance of transistors. These improvements to the CMOS manufacturing process have made it an excellent choice for RF integrated circuit (RFIC) design. The success of RFIC design strongly relies on accurate device models. However, general device models provided by semiconductor foundries are not guaranteed within a certain bias and frequency range, and they also offer poor correlation between the device layouts and the RF characteristics. Transistor layout and its wiring effect are considered as one of the crucial issues for gigahertz circuit design, since they directly affect the RF transceiver performance[1, 2].

Previous approaches to RF-MOSFET modeling involve adding lump elements to a compact model for digital and analog circuit designs, such as BSIM3, BSIM4, and MM9, and they focus on how to build a reasonable sub-circuit and how to extract their values according to equivalent circuits[3−5]. These methods consist of analysis and optimization. Few attempts have been made to build a scalable RF-MOSFET model, including the layout-based extrinsic elements. For RF-MOSFET modeling, lots of issues need to be considered[6, 7], especially the three most important parasitic components: gate resistance R_g, which influences the input impedance and noise performance of RF-MOSFETs[8, 9]. The substrate network has a great impact on output impedance S_{22} when operated at RF, owing to the signal coupling to source and body terminal through the source junction and substrate resistance[6]. The capacitance components describe the capacitive parasitic between the gate and source, and the drain and body terminal.

In this paper, a layout-based scalable model for the parasitic components of RF-MOSFET modeling is developed. The gate resistances, substrate resistances and wiring capacitances are considered and determined from the layout directly.

2. RF-MOSFET model

Figure 1 shows the topology of the proposed RF model for high frequency simulation. In this model, additional parasitic components add to the original PSP model, including gate resistance R_{gate}, substrate resistance R_{juns}, R_{jund} and R_{well}, extrinsic parasitic capacitance drain to source capacitance (C_{dsext}), gate to source capacitance (C_{gsext}), gate to drain capacitance (C_{gdext}), gate extension to drain capacitance (C_{pegd}), and gate extension to drain capacitance (C_{pegs}) to drain capacitance source to bulk diode (D_{jsb}) and drain to bulk diode (D_{jdb}). In order to ensure the DC characteristics, parameters extracted for DC measurements are not perturbed by the possible different R_d and R_s extracted from the measured S-parameters,

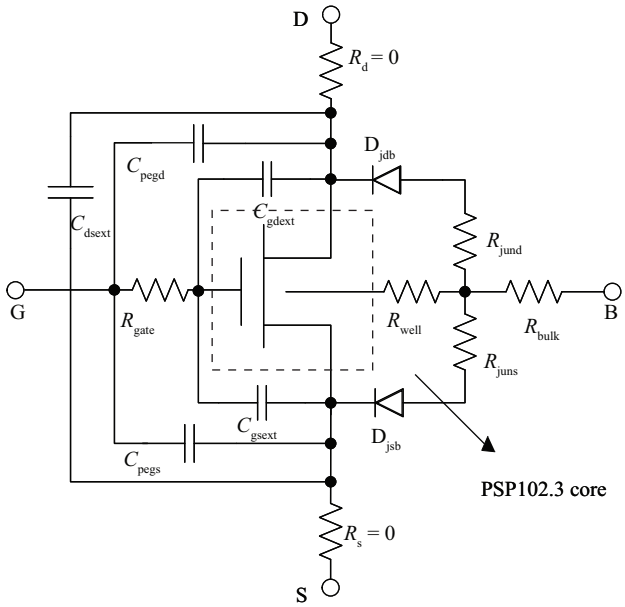

Fig. 1. Equivalent circuit of RF-MOSFET model based on PSP102.3 with parasitic components used for RF simulation.

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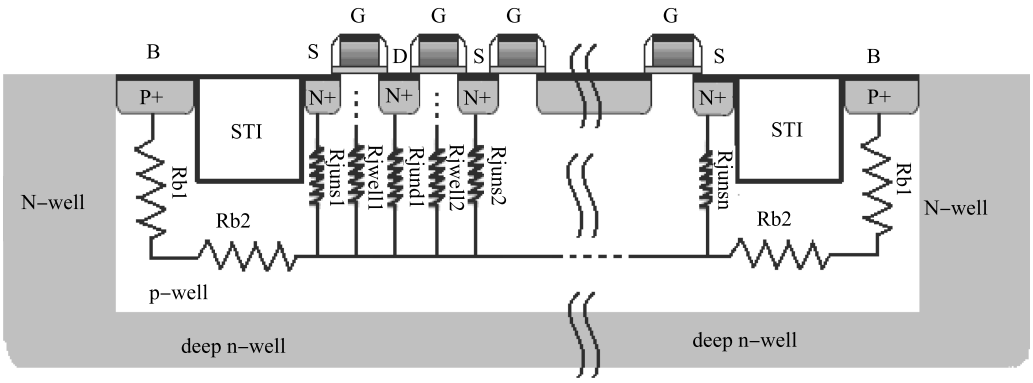

Fig. 3. Equivalent circuit of substrate resistance.

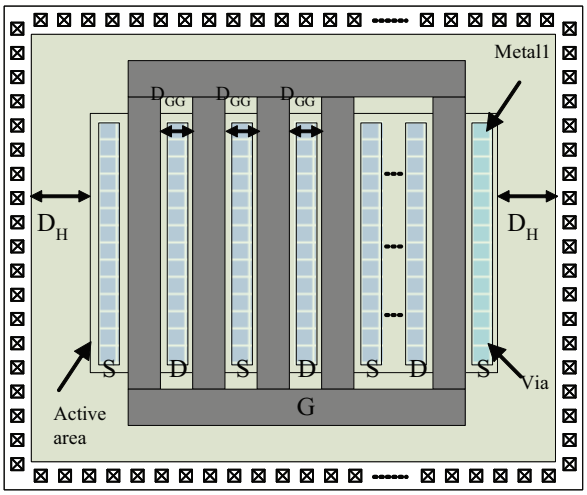

Fig. 2. Typical layout of a RF-MOSFET.

and the values of terminal resistance R_d and R_s are zeroed[6].

For RF circuit design, multi-finger devices are usually employed to improve the parasitic effects. Figure 2 shows the typical layout of a RF-MOSFET: all the source (gate or drain) terminals of different fingers are connected together, and the source and body terminals are grounded together. Detailed calculation methods are described in the following sections.

2.1. Gate resistance model

The proposed gate resistance model mainly consists of three parts: gate poly resistance R_{Gploy}, gate strap resistance R_{Gs} and contact resistance R_{Gc}. Their method of calculation is described in the following sections.

The gate poly resistance R_{Gploy} is expressed as[8]

$$R_{G,\,poly} = \frac{R_{shg}}{N_f L}\left(\frac{W_f}{3N_{gcon}N_{gcon}} + W_{ext}\right), \tag{1}$$

where R_{shg} is the gate sheet resistance of poly-silicon, W_{ext} is the extension of the poly-silicon gate over the active region, L is the channel length, N_f is the number of gate fingers, W_f is the channel width per finger and N_{gcon} is typically 1 or 2, depending on whether the gate fingers are connected to one side or to both sides to account for the gate distributed effect.

The strap resistance R_{Gs} is expressed as

$$R_{G,\,s} = R_{shg}\frac{L_s}{N_{gcon}N_f W_s}, \tag{2}$$

where L_s and W_s are the length and width of the gate strap poly, respectively. They can also be determined for layout. The contact resistance R_{Gc} is expressed as

$$R_{G,\,c} = \frac{R_{con}}{N_{ca}N_{gcon}}, \tag{3}$$

where N_{ca} is the number of contacts between the poly and the metal, depending on the physical layout. R_{con} is the number resistance per contact via. The total gate resistance can be expressed as the sum of Eqs.(1)–(3),

$$R_G = \frac{R_{shg}}{N_f L}\left(\frac{W_f}{3N_{gcon}N_{gcon}} + W_{ext}\right) + \frac{R_{con}}{N_{ca}N_{gcon}} + R_{shg}\frac{L_s}{N_{gcon}N_f W_s}. \tag{4}$$

2.2. Substrate resistance model

As illustrated in Fig. 3, four resistors R_{juns}, R_{jund}, R_{well} and R_{bulk} are proposed. R_{juns} and R_{jund} are used to model the resistance under the source and drain, R_{well} represents the resistance under the gate, and the resistance of bulk is modeled by R_{bulk}.

The basic calculation methodology[10, 11] of resistance is expressed as

$$R = \rho\frac{\text{length}}{\text{area}}. \tag{5}$$

R_{juns1}, R_{jund1} and R_{well1} are, respectively, the source to body resistance, the drain to body resistance and the resistance under the gate, corresponding to each single source, drain and gate region. The value of resistance R_{juns1} can be derived as follows

$$l = X_{well} - X_{js}, \tag{6}$$

$$S = W_f D_{GG}, \tag{7}$$

$$\rho = R_{shb}X_{well} \tag{8}$$

$$R_{juns,1} = R_{shb}X_{well}\frac{X_{well} - X_{js}}{W_f D_{GG}}. \tag{9}$$

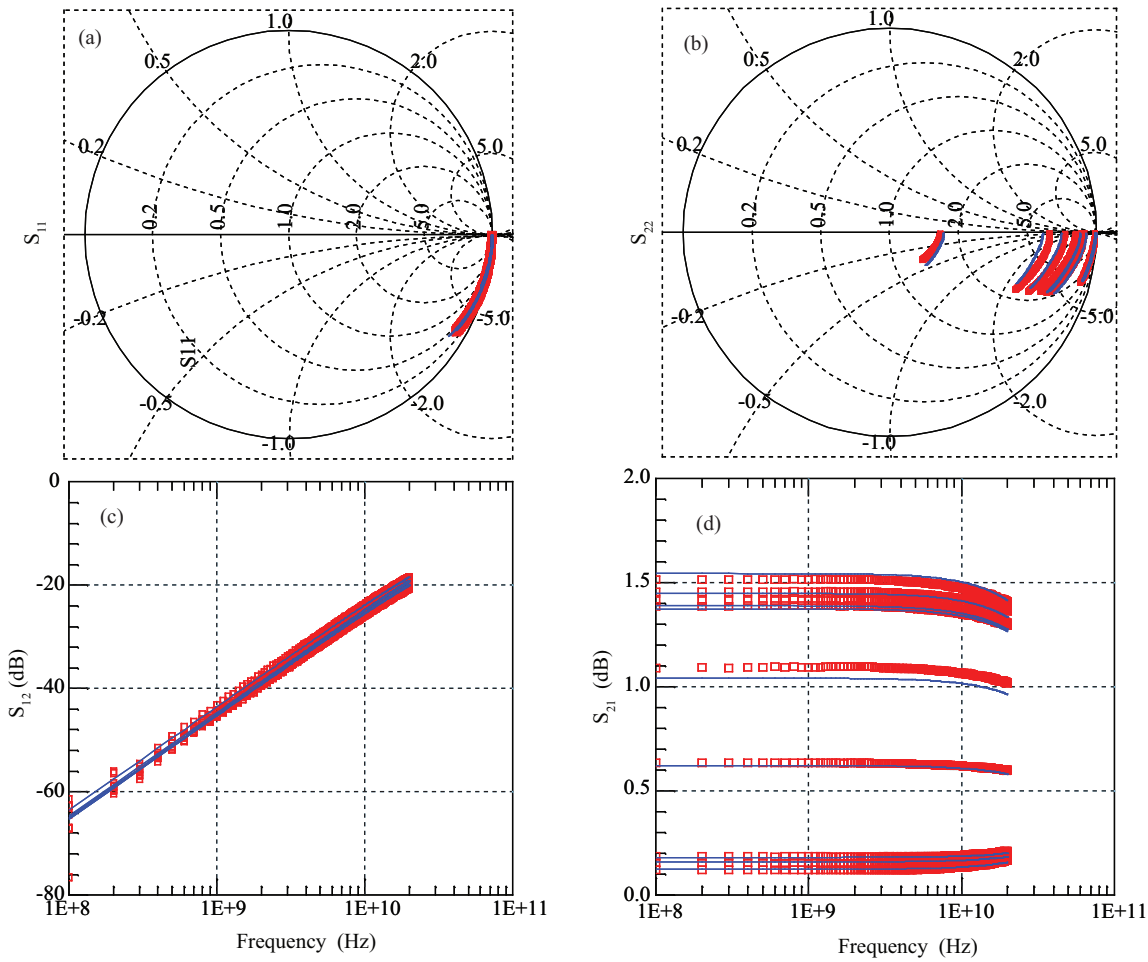

Fig. 4. Measured and simulated S-parameters of an 8-finger nMOSFET (W_f = 2.5 μm and L = 0.13 μm for each finger), with V_{GS} = 0.4, 0.8, 1.2 V and V_{DS} = 0.3, 0.75, and 1.2 V (Square: Measured; Line: Simulated).

Due to resistance in a parallel configuration, the total resistance can be derived as follows,

$$R_{juns} = \left[\sum_{k=1}^{N_s} \frac{1}{R_{juns,k}}\right]^{-1}, \tag{10}$$

$$R_{juns} = R_{shb} X_{well} \frac{X_{well} - X_{js}}{W_f D_{GG} N_s}, \tag{11}$$

$$N_s = \text{int}\left[(N_f + 2)/2\right], \tag{12}$$

where X_{well} and X_j are the depth of the p-well and the junction, respectively. R_{shb} is the sheet resistance of the P-well. N_s is the number of source diffusion, expressed in Eq. (12). The calculation methodology of resistance under the drain and gate is similar to R_{juns}, given by

$$R_{jund} = R_{shb} X_{well} \frac{X_{well} - X_{jd}}{W_f D_{GG} N_d}, \tag{13}$$

$$R_{well} = R_{shb} X_{well} \frac{L}{W_f D_{GG} N_f}, \tag{14}$$

where N_d is the number of drain diffusions, which is expressed as

$$N_d = \text{int}\left[(N_f + 1)/2\right]. \tag{15}$$

The difference between Eqs. (12) and (15) is that only even gate numbers are supported in this model.

R_{bulk} consists of two components: the vertical resistance of the contact area ($R_{b,1}$) and the horizontal resistance between the active area and substrate contact ($R_{b,2}$),

$$R_{b,1} = R_{shb} X_{well} \frac{X_{well} - X_{jd}}{X_1 X_2}, \tag{16}$$

$$R_{b,2} = R_{shb} X_{well} \frac{D_H}{(X_{well} - X_{sti})^2}. \tag{17}$$

The total resistance of bulk can be expressed as the sum of Eqs. (16) and (17),

$$R_{bulk} = \frac{R_{shb} X_{well}}{2} \left[\frac{D_H}{(X_{well} - X_{sti})^2} + \frac{X_{well} - X_{jd}}{X_1 X_2}\right], \tag{18}$$

where X_{sti} and D_H are the depth and the length of shallow trench isolation (STI), respectively. X_1 and X_2 are the width and length of body contact in the vertical direction, respectively.

2.3. Wiring capacitance model

The total wiring capacitance includes (1) C_{gsext}/C_{gdext} includes the contact-ploy and poly-metal-l coupling capacitance

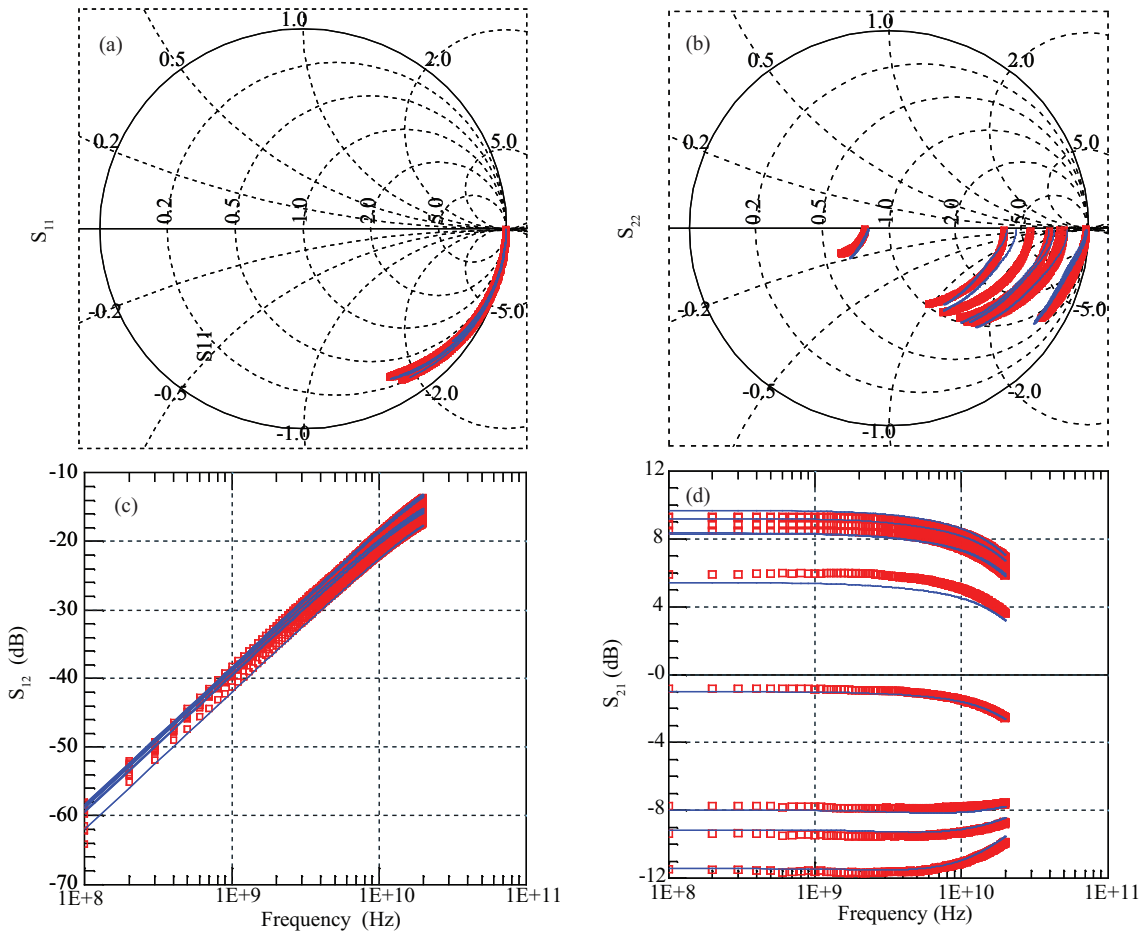

Fig. 5. Measured and simulated S-parameters of a 16-finger nMOSFET (W_f = 2.5 μm and L = 0.13 μm for each finger), with V_{GS} = 0.4, 0.8, 1.2 V and V_{DS} = 0.3, 0.75, and 1.2 V (Square: Measured; Line: Simulated).

between the gate poly and the drain/source, C_{pcgs}; (2) C_{dsext} consists of metal-metal, contact-metal and contact-contact coupling capacitances between the source and the drain; (3) C_{pegd}, C_{pegs} represent the gate strap and gate extension to the source, and the drain, respectively. They are calculated as follows,

$$C_{pcgd} = C_{p1} N_{ct} N_f, \tag{19}$$

$$C_{pcgs} = C_{p1} N_{ct} N_f, \tag{20}$$

$$C_{pmgs} = C_{p2} N_f, \tag{21}$$

$$C_{pmgd} = C_{p2} N_f, \tag{22}$$

$$C_{pegd} = C_{p3} N_d N_{gcon}, \tag{23}$$

$$C_{pegs} = C_{p3} N_s N_{gcon}, \tag{24}$$

$$C_{gsext} = C_{p1} N_{ct} N_f + C_{p2} N_f, \tag{25}$$

$$C_{gdext} = C_{p1} N_{ct} N_f + C_{p2} N_f, \tag{26}$$

$$C_{dsext} = C_{wds} N_f, \tag{27}$$

where N_{ct} is the number of vias between the metal-l and the active region, which can be determined from the layout directly. C_{p1} is the coupling capacitance per via between the gate poly and the contact via. C_{p2} is the coupling capacitance between the gate poly and the metal in the source or the drain. C_{p3} is the coupling capacitance between the gate strap and the gate extension to the source or the drain. C_{wds} is the coupling capacitance between the drain and the source.

3. Model verification and validation

For verification, a set of n-MOSFETs with different numbers of fingers (N_f of each device is 8, 12, 16, 24, 32, 48 and 64, with L = 0.13 μm and W_f = 2.5 μm) were fabricated using the SMIC 0.13 μm 1P8M RF-CMOS process. Two-port S-parameters were measured and de-embedded (Open + Short) for parasitics introduced by GSG PAD using an Agilent E8363B network analyzer and a CASCADE Summit probe station.

Firstly, the DC, AC and junction capacitor model parameters were extracted by the extraction routine installed in Accelion's MBP[12]. These values were kept fixed during ac parameter extraction and optimization. To verify the validity of the proposed scalable model and the RF model parameter extraction method, the macro-model shown in Fig. 1, consisting of a PSP102.3 model core with the proposed new RF parasitic

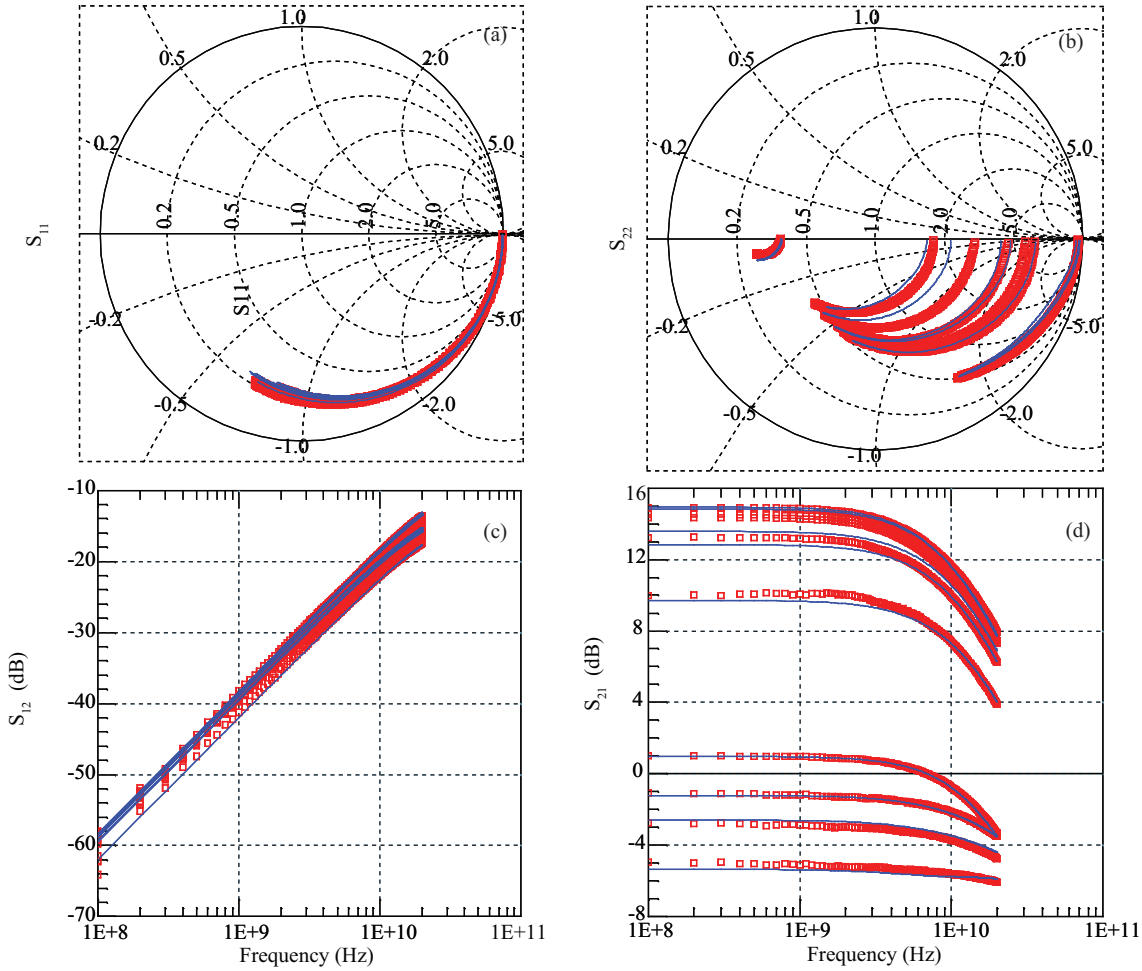

Fig. 6. Measured and simulated S-parameters of a 32-finger nMOSFET (W_f = 2.5 μm and L = 0.13 μm for each finger), with V_{GS} = 0.4, 0.8, 1.2 V and V_{DS} = 0.3, 0.75, and 1.2 V (Square: Measured; Line: Simulated).

network, is simulated based on the extracted parameters in the Agilent advanced design system (ADS) directly.

Figures 4 to 6 depict excellent agreement between the measured and simulated S-parameters of three multi-finger RF-MOSFETs in different operating regions, which validated the accuracy of the proposed scalable model.

4. Conclusions

A layout-based scalable model for multi-finger RF-MOSFET modeling has been presented. A simple but accurate method is proposed to directly determine all the parasitic components of MOSFETs for high frequency applications. This model was further verified and validated through the excellent agreement observed up to 20 GHz between the simulated and measured S-parameters of a set of nMOSFETs with different numbers of fingers, connected in common-source and operated in different bias conditions.

References

[1] Cao C, Kenneth K O. A 90-GHz voltage-controlled oscillator with a 2.2-GHz tuning range in a 130-nm CMOS technology. Proc Symp VLSI Circuits Dig Tech Papers, 2005: 242

[2] Chan C Y, Chen S C, Tsai M H, et al. Wiring effect optimization in 65-nm low-power NMOS. IEEE Electron Device Lett, 2008, 29(11): 1245

[3] Jen S H M, Enz C C, Pehlke D R, et al. Accurate modeling and parameter extraction for MOS transistors valid up to 10 GHz. IEEE Trans Electron Devices, 1999, 46(11): 2217

[4] Lee S, Yu H K. A semianalytical parameter extraction of a SPICE BSIM3v3 for RF MOSFET's using S-parameters. IEEE Trans Microw Theory Technol, 2000, 48(3): 412

[5] Gao J, Werthof A. Scalable small-signal and noise modeling for deep-submicrometer MOSFETs. IEEE Trans Microw Theory Technol, 2009, 57(4): 737

[6] Cheng Y, Deen J, Chen C H. MOSFET modeling for RF IC design. IEEE Trans Electron Devices, 2005, 52(7): 1286

[7] Pehlke D R, Schroter M, Burstein A, et al. High-frequency application of MOS compact models and their development for scalable RF model libraries. IEEE CICC, 1998

[8] Cheng Y, Matloubian M. High frequency characterization of gate resistance in RF MOSFETs. IEEE Electron Device Lett, 2001, 22(2): 98

[9] Jin X, Ou J J, Chen C H. An effective gate resistance model for CMOS RF and noise modeling. IEDM Tech Dig, 1998: 961

[10] Kang I M, Jung S J, Choi T H, et al. Scalable model of substrate resistance components in RF MOSFETs with bar-type body contact considered layout dimensions. IEEE Electron Device Lett, 2009, 30(4): 404

[11] Itoh N, Ohguro T, Katoh K, et al. Scalable parasitic components model of CMOS for RF circuit design. IECICE Trans Fundamentals, 2003, E86-A(2): 288

[12] Accelicon MBP User Guide Accelicon Technologies, Inc., 2009