A novel TFS-IGBT with a super junction floating layer*

Ye Jun(叶俊)†, Fu Daping(傅达平), Luo Bo(罗波), Zhao Yuanyuan(赵远远), Qiao Ming(乔明), and Zhang Bo(张波)

(State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China)

Abstract: A novel trench field stop (TFS) IGBT with a super junction (SJ) floating layer (SJ TFS-IGBT) is proposed. This IGBT presents a high blocking voltage (> 1200 V), low on-state voltage drop and fast turn-off capability. A SJ floating layer with a high doping concentration introduces a new electric field peak at the anode side and optimizes carrier distribution, which will improve the breakdown voltage in the off-state and decrease the energy loss in the on-state/switching state for the SJ TFS-IGBT. A low on-state voltage (V_F) and a high breakdown voltage (BV) can be achieved by increasing the thickness of the SJ floating layer under the condition of exact charge balance. A low turn-off loss can be achieved by decreasing the concentration of the P-anode. Simulation results show that the BV is enhanced by 100 V, V_F is decreased by 0.33 V (at 100 A/cm^2) and the turn-off time is shortened by 60%, compared with conventional TFS-IGBTs.

Key words: IGBT; super junction; on-state voltage; breakdown voltage; energy loss; charge balance
DOI: 10.1088/1674-4926/31/11/114008 **EEACC:** 2560

1. Introduction

In the field of power semiconductor devices, the most important factors are reducing the switching/on-state loss, increasing the power density and improving the maximum operating temperature. Insulated gate bipolar transistors (IGBTs) combine the high input impedance of an MOSFET with the current carrying capability of an bipolar transistor. In recent years, the IGBT has established itself as the device of choice for low-medium power electronic applications, such as AC motors, frequency converters, switching mode power suppliers (SMPSs), LED drivers and traction engines due to its switching loss/on-state voltage drop trade off, high current carrying capability, wide safe operating area, ease of gate control, ruggedness and ease of manufacture[1−3]. The IGBT has developed from punch through (PT) to non-punch through (NPT), field stop (FS), and to lightly punch through (LPT) with respect to fabrication technology, and from planar to trench with respect to gate structure[4−7]. PT and NPT technology has limitations to some extent, thus giving birth to FS technology, which is a compromise between PT and NPT. Planar gate structure is difficult for high-density integration because of the intrinsic JFET effect, and thus it promotes the development of the trench gate.

In order to improve the trade-off between turn-off loss and on-state voltage drop so as to improve the performance of the IGBT, researchers have undertaken much work and proposed many structures: a low-doped P-buffer and transparent P-emitter structure was proposed by Matsudai *et al.*[8] to eliminate the oscillation of turn-off waveforms so as to reduce turn-off loss; a 3D n-region-controlled anode structure was proposed by Chen *et al.*[9] to cut the turn-off time; the IEGT was proposed by Kitagawa *et al.*[10] to boost the plasma density in the vicinity of the cathode cell; a moderately doped n region under the p base structure was proposed by Mori *et al.*[11] to enhance the carrier density in the vicinity of the cathode; and an accumulation channel trench gate insulated gate bipolar transistor (ACT-IGBT) was proposed by Qiang *et al.*[12] to lower the on-state voltage drop.

In this paper, an SJ TFS-IGBT is proposed. This maintains a high static/dynamic avalanche breakdown and further improves the trade-off between turn-off loss and on-state voltage drop. The main aim of the paper is to identify the optimal SJ TFS-IGBT structure from a static characteristic, on-state/switching loss point of view.

2. Device structure and operation mechanism

The FS offers the thinnest drift region and employs the most powerful concept to design the optimal plasma in the drift region. The trench brings with it a more natural 1D current distribution, eliminates the parasitic JFET effect, enhances the PIN diode effect (electron injection into the top side of the drift region), minimizes the MOS channel resistance and increases the immunity against latch-up. Figure 1(b) shows a schematic cross-section of the proposed SJ TFS-IGBT. The SJ floating layer with a narrow p-pillar (with correspondingly more doping) and a wide n-pillar (with relatively less doping) is inserted between the N-buffer and the N-drift region in this new structure. It brings the following two advantages. First, the p-pillar of the SJ floating layer forms a new p-pillar/n junction. As a result, a new electric field peak comes into being which will modulate the original electric field distribution and improve the breakdown voltage. Second, for the conventional TFS-IGBT, the hole density near the cathode and the electron density near the anode are small. In contrast, the new structure optimizes

* Project supported by the National Natural Science Foundation of China (No. 60906038) and the Science-Technology Foundation for Young Scientist of University of Electronic Science and Technology of China (No. L08010301JX0830).
† Corresponding author. Email: andyye1009@126.com
Received 20 May 2010

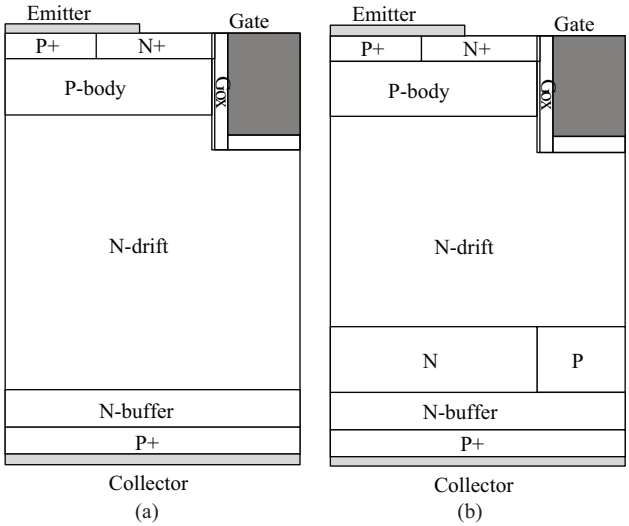

Fig. 1. Schematic cross-section of (a) conventional TFS-IGBT and (b) proposed SJ TFS-IGBT.

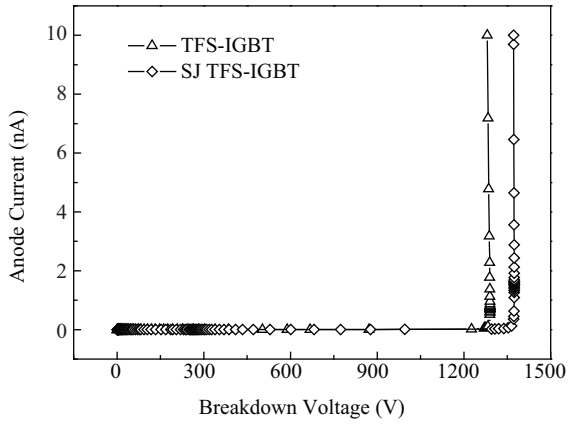

Fig. 2. Breakdown characteristics of conventional TFS-IGBT and proposed SJ TFS-IGBT.

carrier distribution. It enhances the hole density near the cathode region and electron density in the vicinity of the anode. High plasma density in the device results in a lower on-state voltage, plenty of electrons close to the anode and holes close to the cathode, which can be quickly extracted in the off-state, which leads to lower turn-off loss.

3. Results and discussion

2D simulation was carried out utilizing Medici to determine the device electrical characteristics. The key parameters are as follows. The width of the half cell pitch is 6 μm, the channel length is 3.5 μm, the gate oxide thickness is 100 nm, the 6-μm-thick N-buffer layer has a concentration of 1×10^{17} cm^{-3}, the 41-μm-thick N-drift layer has a concentration of 5×10^{13} cm^{-3}, and the 45-μm-thick SJ layer has a concentration of 5×10^{15} cm^{-3} for the p-pillar and 2.5×10^{15} cm^{-3} for the n-pillar.

3.1. Forward blocking characteristics

The breakdown characteristics of the conventional TFS-IGBT and proposed SJ TFS-IGBT are shown in Fig. 2. The SJ TFS-IGBT demonstrates a breakdown voltage (BV) of 1372 V, compared with the conventional TFS-IGBT, where the BV is increased by 100 V. This is due to the introduction of the SJ floating layer, which forms a new PN junction and yields a new electric field peak at the anode side. Figure 3 shows a comparison of the vertical electric field distribution of the conventional TFS-IGBT and the proposed SJ TFS-IGBT. As can be seen, the conventional TFS-IGBT has only one electric field peak at the cathode side and decreases linearly from the cathode to the anode side. By contrast, the proposed SJ TFS-IGBT has an electric field peak both at the cathode and at the anode side. A higher electric field peak appears at the anode side because of the high doping concentration of the SJ floating layer. The electric field peak of the anode is strongly dependent on the concentration of the SJ floating layer, according to Eqs. (1)–(3). In other words, the concentration of the SJ floating layer can adjust and control the electric field of the anode.

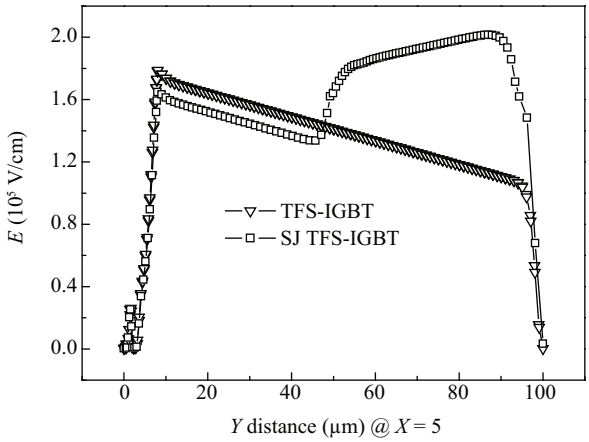

Fig. 3. Vertical electric field distribution of conventional TFS-IGBT and proposed SJ TFS-IGBT.

$$V_{\rm bi} = \frac{kT}{q} \ln \frac{N_{\rm A} N_{\rm D}}{n_{\rm i}^2}, \tag{1}$$

$$N_0 = \frac{1}{\dfrac{1}{N_{\rm A}} + \dfrac{1}{N_{\rm D}}}, \tag{2}$$

$$E_{\max} = \left(\frac{2qN_0}{\varepsilon_{\rm s}} V_{\rm bi} \right)^{\frac{1}{2}}, \tag{3}$$

where $\frac{kT}{q}$ is the thermal voltage, $N_{\rm A}$ is the acceptor doping concentration, $N_{\rm D}$ is the donor doping concentration, $n_{\rm i}$ is the intrinsic carrier concentration, $V_{\rm bi}$ is the built-in potential and $\varepsilon_{\rm s}$ is the permittivity of the semiconductor.

3.2. Forward conduction characteristics

The on-state voltage drop versus the anode current of the two structures, and I–V characteristics of the proposed SJ TFS-IGBT at temperatures of 300 and 400 K, are shown in Fig. 4. As can be seen, the on-state voltage drop at 100 A/cm^2 is decreased by 0.33 V, from 2.53 V for the conventional TFS-IGBT to 2.2 V for the proposed SJ TFS-IGBT, which means a lower on-state loss. For the proposed structure, as the temperature rises, the energy barrier of the junction P-anode/N-buffer decreases, which will lead to a lower on-state voltage

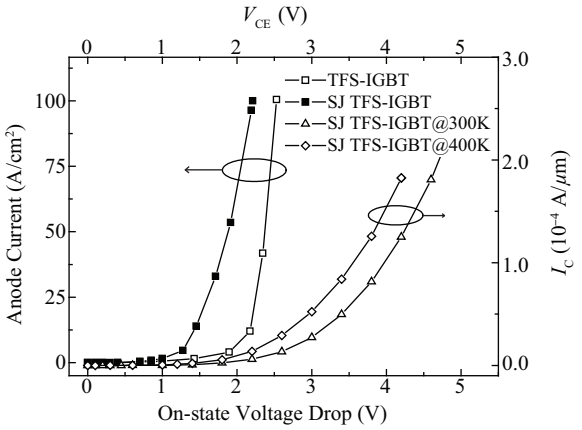

Fig. 4. On-state voltage drop versus anode current of the two structures, and I–V characteristics of the proposed SJ TFS-IGBT at temperatures of 300 and 400 K.

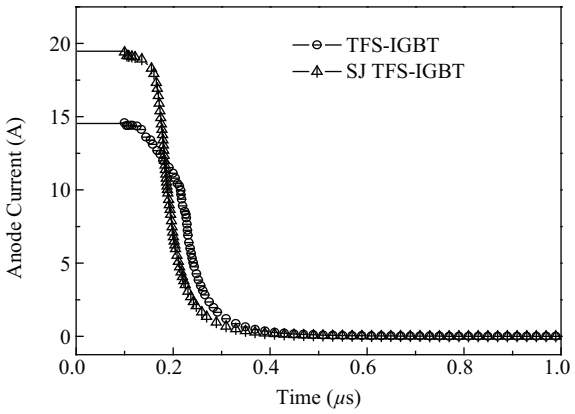

Fig. 5. Turn-off characteristics of the conventional TFS-IGBT and proposed SJ TFS-IGBT (gate resistance R_G = 22 Ω, load inductance L_0 = 480 μH, stray inductance L_S = 200 nH, pulse gate voltage V_{GS} = 15 V, minority carrier lifetime $\tau_{n0} = \tau_{p0} = 1$ μs and DC bus voltage V_{dc} = 1200 V).

drop. However, channel resistance as well as the N-drift resistance increase with rising temperature. Due to these characteristics, changes in the voltage of the junction P-anode/N-buffer are larger than those in the channel resistance and the N-drift region resistance at low collector current level, so the on-state voltage drop has a small negative temperature coefficient, as illustrated in Fig. 4. A large positive temperature coefficient of the on-state voltage drop will degrade the current handling capability of the IGBT significantly, but a small positive temperature coefficient at a higher current level is beneficial to homogeneous current distribution within chips and good current sharing when paralleling devices. A large negative temperature coefficient of the on-state voltage drop will be prone to thermal runaway, so care should be taken when it used. Conversely, a small negative temperature coefficient is helpful for carrying current capability. In conclusion, a small temperature coefficient closing to zero is a good choice for an IGBT.

3.3. Turn-off characteristics

The turn-off waveforms in the inductive condition of the conventional TFS-IGBT and proposed SJ TFS-IGBT are shown in Fig. 5. It can be seen that the proposed SJ TFS-IGBT with a capability of turning off 20 A or so anode current, compared with 15 A for conventional TFS-IGBT, has a 25% stronger turning-off capability.

As can be seen from Fig. 5, the turn-off time (T_{off}) is shortened by 60%, from 250 ns for the conventional TFS-IGBT to 100 ns for the proposed SJ TFS-IGBT, so its turn-off loss is much lower. A lower turn-off loss is attributed to an optimized carrier distribution, as illustrated in Figs. 6 and 7. Holes distribute more near the cathode and less near the anode, while electrons distribute more in the whole region compared with the conventional TFS-IGBT, which is called anode and cathode engineering in Refs. [13–15]. As reported in the literature, this structure betterments turn-off characteristic sharply while not degenerating the on-state voltage drop.

In order to understand the SJ TFS-IGBT's turn-off behavior in depth, different concentrations of the P-anode were simulated while keeping the other parameters unchanged. The results are plotted in Fig. 8. From this we draw the conclusion that

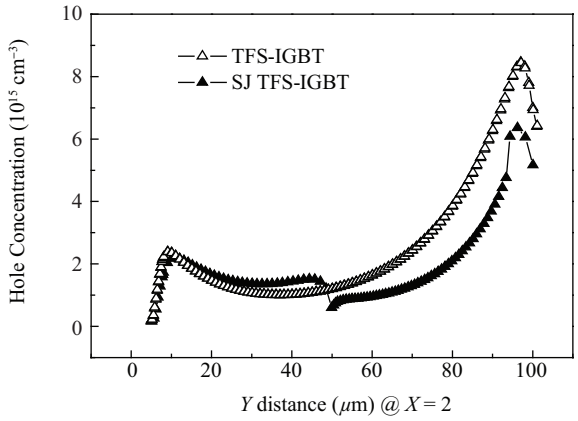

Fig. 6. Hole distribution of the conventional TFS-IGBT and the proposed SJ TFS-IGBT.

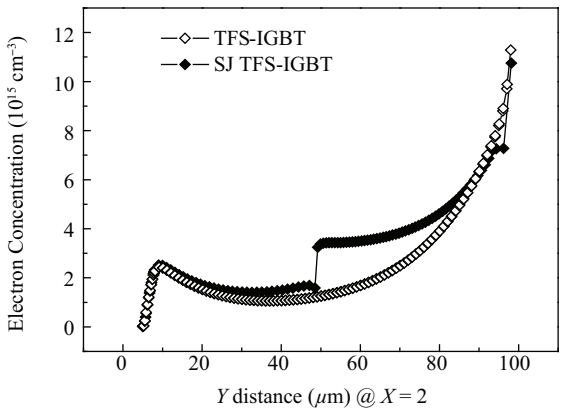

Fig. 7. Electron distribution of the conventional TFS-IGBT and the proposed SJ TFS-IGBT.

the turn-off time is dependent on the P-anode's concentration: the higher the P-anode's concentration, the longer the turn-off time. The concentration of the P-anode should be strictly controlled, otherwise an unintended result will appear.

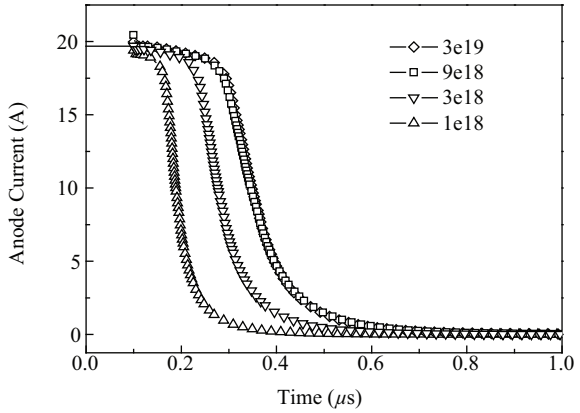

Fig. 8. Influences of the P-anode's concentration on the turn-off time of the proposed SJ TFS-IGBT (gate resistance $R_G = 22\ \Omega$, load inductance $L_0 = 480\ \mu$H, stray inductance $L_S = 200$ nH, pulse gate voltage $V_{GS} = 15$ V, minority carrier lifetime $\tau_{n0} = \tau_{p0} = 1\ \mu$s and DC bus voltage $V_{dc} = 1200$ V).

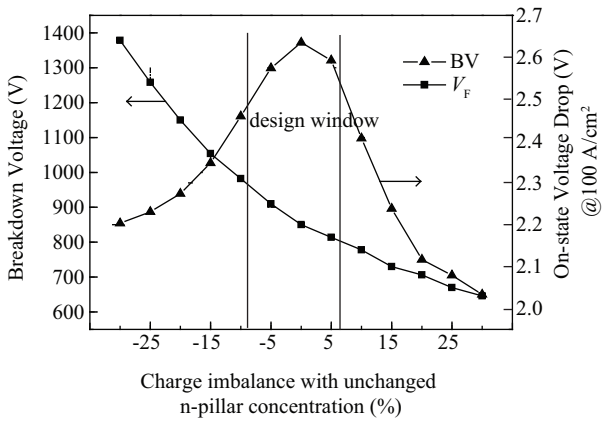

Fig. 9. Sensitivity of the BV and V_F versus the charge imbalance for the proposed SJ TFS-IGBT.

3.4. Charge imbalance and design windows

For the SJ, the charge imbalance is an unavoidable and serious problem that has to be mentioned, although the process technology has been greatly improved. Figure 9 shows the sensitivity of the BV and V_F versus the charge imbalance of the proposed SJ TFS-IGBT. Figure 10 shows the sensitivity of the BV and $R_{on,SP}$ versus the charge imbalance of the proposed SJ TFS-IGBT. Ideally, the highest BV can be obtained when the charge is balanced. However, when the charge balance was broken, the breakdown voltage began to decline parabolically from the balanced peak value and the on-state voltage drop decreased monotonically. A charge imbalance changing from negative to positive means that the carrier density has increased, so $R_{on,SP}$ decreases, as Figure 10 shows. The design windows meeting at least 1200 V BV are illustrated in Figs. 9 and 10. In these design windows, V_F ranges from 2.15 to 2.3 V, $R_{on,SP}$ ranges from 0.5 to 0.54 $\Omega\cdot$mm^2 and –8% to 8% for charge imbalance, which is in the control of the process technology.

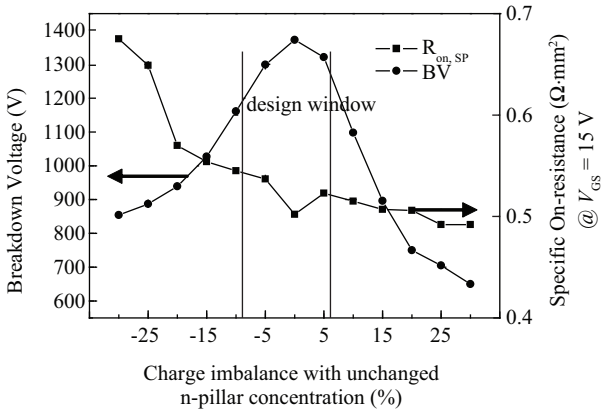

Fig. 10. Sensitivity of the BV and $R_{on,SP}$ versus the charge imbalance for the proposed SJ TFS-IGBT.

4. Conclusion

A novel TFS-IGBT with a SJ floating layer between the N-buffer and N-drift is demonstrated to improve the trade-off between V_F and E_{off}. An optimized carrier distribution is achieved by the introduction of the SJ floating layer, so a lower E_{off} is obtained in the off-state while not deteriorating V_F in the on-state. The thickness and concentration of the SJ floating layer have great influence over the overall performance of the SJ TFS-IGBT; an optimal SJ TFS-IGBT is achieved by changing these parameters. Simulation results show that the SJ TFS-IGBT exhibits a BV of 1372 V, V_F of 2.2 V and T_{off} of 100 ns, compared with the conventional TFS-IGBT BV, which is enhanced by 100 V, and where V_F is decreased by 0.33 V and T_{off} is shortened by 60%. The excellent device performances make the proposed SJ TFS-IGBT a promising candidate for power electronic applications.

References

[1] Bryant A T, Wan Y, Finney S J, et al. Numerical optimization of an active voltage controller for high-power IGBT converters. IEEE Trans Power Electron, 2007, 22(2): 374

[2] Combrink F W, Mouton H T, Enslin J H R, et al. Design optimization of an active resonant snubber for high power IGBT converters. IEEE Trans Power Electron, 2006, 21(1): 114

[3] Sheng K, Williams B W, Finney S J. A review of IGBT models. IEEE Trans Power Electron, 2000, 15(6): 1250

[4] Laska T, Münzer M, Pfirsch F, et al. The field stop IGBT (FS IGBT)—a new power device concept with a great improvement potential. Proc ISPSD, 2000: 355

[5] Rahimo M, Schlapbach U, Kopta A, et al. SPT+, the next generation of low-loss HV-IGBTs. Proc PCIM, 2005: 361

[6] Nakamura K, Kusunoki S, Nakamura H, et al. Advanced wide cell pitch CSTBTs having light punch-through (LPT) structure. Proc ISPSD, 2002: 277

[7] Nakamura K, Hisamoto Y, Matsumura T, et al. The second stage of a thin wafer IGBT low loss 1200 V LPT-CSTBTTM with a backside doping optimization process. Proc ISPSD, 2006: 133

[8] Matsudai T, Tsukuda M, Umekawa S, et al. New anode design concept of 600 V thin wafer PT-IGBT with very low dose P-buffer and transparent P-emitter. IEE Proceedings of Circuits Devices, 2004: 151

[9] Chen W, Zhang B, Li Z. Area-efficient fast-speed lateral IGBT

with a 3D n-region-controlled anode. IEEE Electron Device Lett, 2010, 31(5): 468

[10] Kitagawa M, Omura I, Hasegawa S, et al. A 4500 V injection enhanced insulated gate bipolar transistor (IEGT) in a mode similar to a thyristor. Tech Dig IEDM, 1993: 679

[11] Mori M, Oyama K, Kohno Y, et al. A trench-gate high-conductivity IGBT (HiGT) with short-circuit capability. IEEE Trans Electron Devices, 2007, 54(8): 2011

[12] Qian Mengliang, Li Zehong, Zhang Bo, et al. Insulated gate bipolar transistor with trench gate structure of accumulation channel. Journal of Semiconductors, 2010, 31(3): 034002

[13] Nakamura K, Oya D, Saito S, et al. Impact of an LPT (II) concept with thin wafer process technology for IGBT's vertical structure. Proc ISPSD, Barcelona-Spain, 2009: 295

[14] Mori M, Uchino Y, Sakano J, et al. A novel high conductivity IGBT (HiGT) with a short circuit capability. Proc ISPSD, 1998: 429

[15] Green D, Vershinin K, Sweet M, et al. Anode engineering for the insulated gate bipolar transistor—a comparative review. IEEE Trans Power Electron, 2007, 22(5): 1857