A 100-MHz bandpass sigma–delta modulator with a 75-dB dynamic range for IF receivers*

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Abstract: A fourth-order switched-capacitor bandpass ΣΔ modulator is presented for digital intermediate-frequency (IF) receivers. The circuit operates at a sampling frequency of 100 MHz. The transfer function of the resonator considering nonidealities of the operational amplifier is proposed so as to optimize the performance of resonators. The modulator is implemented in a 0.13-μm standard CMOS process. The measurement shows that the signal-to-noise-and-distortion ratio and dynamic range achieve 68 dB and 75 dB, respectively, over a bandwidth of 200 kHz centered at 25 MHz, and the power dissipation is 8.2 mW at a 1.2 V supply.

Key words: analog-to-digital converter; bandpass sigma-delta modulator; resonator; IF receiver

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1. Introduction

With the development of modern wireless communication systems, one of the recent trends in radio receiver research has been to digitize the signals from the intermediate-frequency (IF)[1, 2], because digital signal processing is more flexible and insensitive to nonidealities. By converting analog to digital at the IF location, lower-frequency signals can be processed in the digital domain, so that the imperfections of analog circuitry, such as flicker noise and DC offset, can be efficiently avoided[1].

A digital IF receiver[2] is shown in Fig. 1. The bandpass (BP) ΣΔ modulator is a popular architecture as the core of analog-to-digital converters (ADC) in this system, due to its high resolution for narrow bandwidth signals as well as greater immunity to analog nonidealities than Nyquist ADC counterparts.

This paper presents a 4th-order bandpass ΣΔ modulator for digital IF receivers. In order to simplify I and Q demodulation[1], the sampling frequency (f_s) is set to 100 MHz, and the signal band is centered at 25 MHz with a bandwidth of 200 kHz for GSM. In Section 2, the details of the architectural issues are discussed. Section 3 is dedicated to the circuit implementation guided by a proposed transfer function of the resonator considering analog nonidealities. Section 4 shows the measurement results and is followed by the conclusion.

2. Architectural design

2.1. Modulator topology

The modulator architecture is designed by building a behavior model in MATLAB.

The design of the bandpass ΣΔ modulator is guided by the theoretical signal-to-quantization-noise ratio (SQNR), which is expressed as

$$\mathrm{SQNR} = 10\lg\left[\frac{3}{2\pi^L}(1+L)\cdot \mathrm{OSR}^{L+1}\left(2^N-1\right)^2\right], \quad (1)$$

where L is the order of the loop filter, OSR is the oversampling ratio and N is the internal resolution. Equation (1) indicates that, in order to achieve the specified performance, the design parameters of ΣΔ modulators are the oversampling ratio, the order of the loop filter, and the internal resolution.

A design tradeoff can be made according to Eq. (1). From the OSR point of view, SQNR increases sharply along with OSR, which, however, is fixed to 250 in this design since the sampling frequency is 100 MHz for GSM, i.e., 200 kHz signal bandwidth. From the loop filter point of view, the in-band noise decreases as L increases. Single-loop and cascaded architectures are possible options. The former with sixth or greater order may suffer from instability[2], which has to be carefully considered in the design phase. The latter enables high-order noise shaping without stability problems, but suffers from quantization noise leakage due to the mismatch of the analog and digital paths, leading to serious deterioration of the noise performance of the modulator. From the internal res-

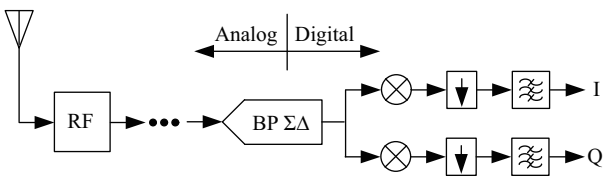

Fig. 1. Digital IF receiver.

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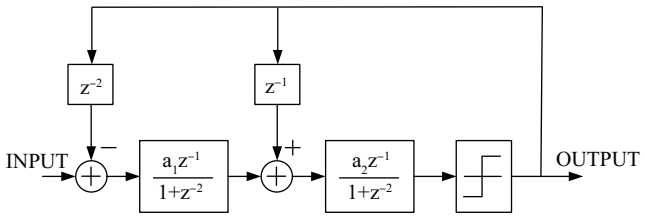

Fig. 2. Bandpass ΣΔ modulator architecture.

olution point of view, the quantization noise decreases by 6 dB for each bit added to the quantizer, resulting in high SQNR, theoretically. However, any distortion in the required multi-bit feedback DAC is not shaped in the loop and directly subtracted from the input signal. Hence, the linearity of a multi-bit ΣΔ modulator is ultimately limited by that of the DAC. In order to relieve such effects, a dynamic element matching technique has been widely used, which, however, introduces extra power consumption as a penalty. In summary, with a view to power efficiency, single-loop single-bit architecture is adopted in this paper.

At the sampling rate of 100 MHz, the OSR for GSM is 250. According to MATLAB-based behavioral simulations, a 1-bit 4th-order bandpass .ΣΔ modulator is sufficient for the GSM requirements.

Figure 2 shows the topology of the designed 1-bit 4$^{\text{th}}$-order bandpass modulator, consisting of two resonators, a 1-bit quantizer and feedback delay blocks. The resonators with the loop coefficients a_1 and a_2, which are implemented by double-delay (DD)[2] topology, have only one feedforward delay. The noise transfer function (NTF) of the targeted modulator can be calculated as

$$\mathrm{NTF}(z) = \frac{\left(1+z^{-2}\right)^2}{1+(2-a_2)\,z^{-2}+[1-a_2\,(1-a_1)]\,z^{-4}}, \quad (2)$$

where the coefficients a_1 and a_2 are determined in order to obtain the designed signal-to-noise ratio (SNR), as shown in Fig. 3, and set to 1/3 and 3/4, respectively. Although, a bigger a_1 improves SNR a litter further, it requires a larger output swing of the operational amplifier (OTA), which is not suitable for an operating voltage as low as 1.2 V in this design.

2.2. Stability model

In order to analyze the stability of ΣΔ modulators, a quantizer gain λ, whose value varies from zero to infinity for a 1-bit ΣΔ modulator, is introduced to model the nonlinearity[3]. Then, Equation (2) can be rewritten as

$$\mathrm{NTF}(z) = \frac{\left(1+z^{-2}\right)^2}{1+(2-\lambda a_2)\,z^{-2}+[1-\lambda a_2\,(1-a_1)]\,z^{-4}}. \quad (3)$$

The stability depends on the poles of the NTF, and the root locus for a 4th-order bandpass ΣΔ modulator is shown in Fig. 4 with $a_1 = 1/3$ and $a_2 = 3/4$. When the value of λ goes high, a pole pair moves outside the unit circle. Then the signal swings begin to increase, and the gain λ decreases, leading to the pole pair moving back inside the unit circle. Therefore, the modulator is stable with the determined coefficients a_1 and a_2.

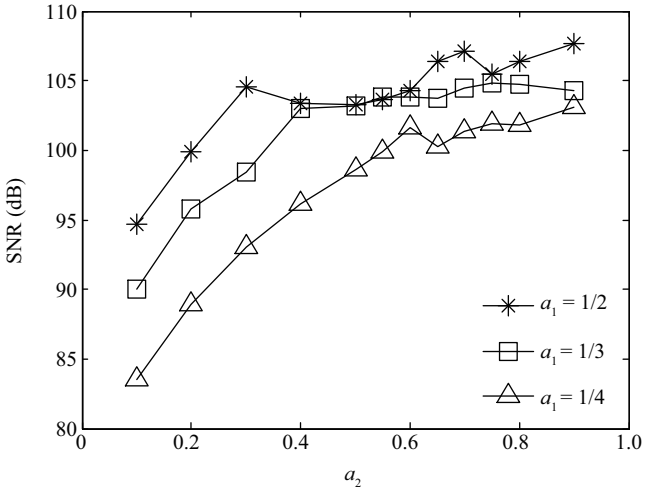

Fig. 3. Simulated SNR for bandpass modulator.

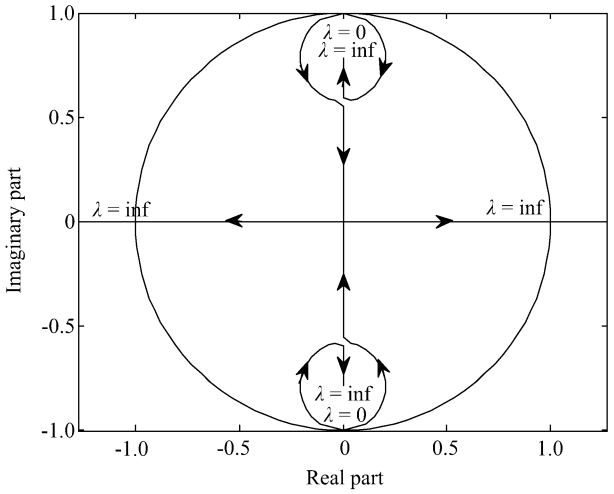

Fig. 4. Root locus of the poles for a 4th-order bandpass ΣΔ modulator.

3. Circuit implementation

The modulator is implemented as a fully-differential switched-capacitor circuit, as shown in Fig. 5. The circuit schematic is equivalent to the block diagram in Fig. 2, and the outputs of two delay blocks control the inputs of the resonators as feedback signals. The analog blocks are explained in detail as follows.

3.1. Resonator

As mentioned above, the resonators are implemented by DD topology in this paper. Actually, a discrete-time (DT) resonator can be implemented with different structures, such as Forward Euler (FE), lossless discrete integrator (LDI), or double-delay (DD), among which the DD structure is the only one where it is possible to use one amplifier to implement a resonator. Additionally, the DD structure is found to be the most insensitive to circuit nonidealities, such as capacitor mismatching[4]. The drawbacks of this structure include more switches, and complex clocking signals. In addition, its center frequency is fixed at $f_s/4$. Nevertheless, the DD structure is regarded as

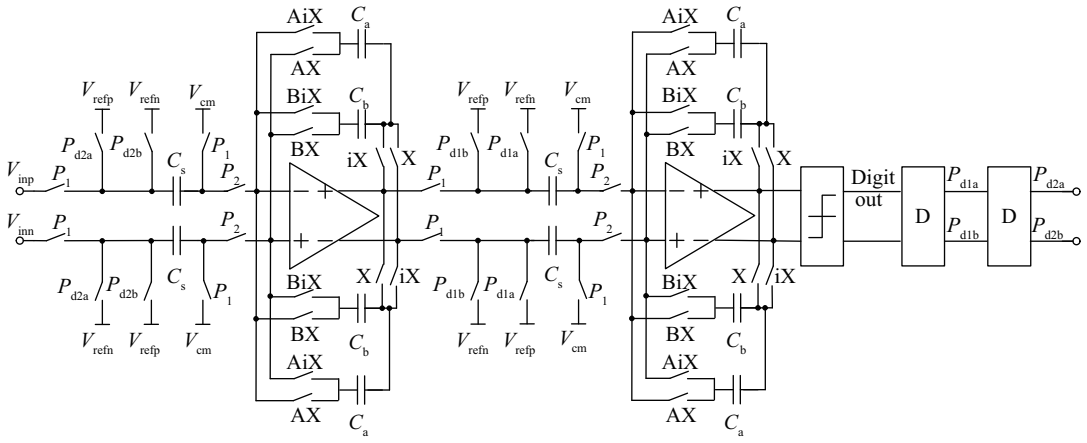

Fig. 5. Circuit schematic of the bandpass ΣΔ modulator.

the best candidate for high performance bandpass ΣΔ modulators. Since the center frequency of $f_s/4$ is suitable for our design, the DD structure is used.

The operation of the DD resonator[2] can be seen in Fig. 6. The signal P_{da} and P_{db} are controlled by the feedback circuit, and others are generated by a clock generator, as shown in Fig. 6(b). In clock phase P_1, the input voltage is sampled to the capacitor C_s. In clock phase P_2, the charge in the C_s is transferred to one of the integration capacitors C_a or C_b. Both integration paths operate alternately.

Therefore, the output signal in the z-domain can be written as

$$V_o(z) = \frac{C_s}{C_{a,b}} \frac{z^{-1}}{1+z^{-2}} V_i(z), \tag{4}$$

where C_s and $C_{a,b}$ are chosen to obtain the desired a_1 and a_2 for two resonators in Fig. 2.

3.2. Sampling capacitor

In sampling circuits, the thermal noise, which is caused by the thermal motion of the charge carriers, limits the performance severely. In order to make the thermal noise neglectable under a given DR, the input sampling capacitor should satisfy

$$C_s = \frac{8kT \cdot \mathrm{DR}}{V_{FS}^2 \cdot \mathrm{OSR}}, \tag{5}$$

where k is the Boltzmann constant, T is the absolute temperature, and V_{FS} is the amplitude of a full-scale sinusoidal input.

Therefore, given DR = 85 dB for a design margin, V_{FS} = 0.4 V, and OSR = 250, the required sampling capacitance is calculated as 0.26 pF at room temperature. With the extra noise margin, the final sampling capacitance is set to 0.5 pF. Although this capacitance is applicable to both resonators, it is too stringent for the second one, whose input noise would be shaped by the loop filter. Hence, the capacitor value of the second resonator is set to 0.4 pF.

3.3. Operational amplifier

According to Eq. (4), the ideal z-domain transfer function of the resonator $H_i(z)$ can be expressed as

$$H_i(z) = \frac{C_s}{C_{a,b}} \frac{z^{-1}}{1+z^{-2}}. \tag{6}$$

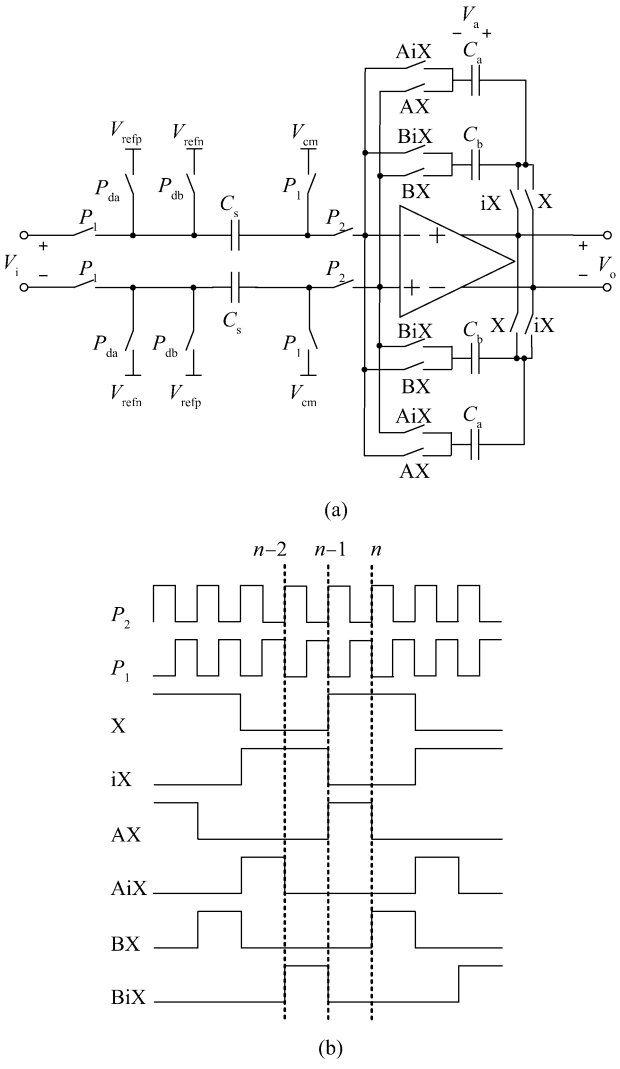

Fig. 6. Double-delay resonator. (a) Circuit diagram. (b) Timing diagram.

However, the nonidealities of the operational amplifiers make the transfer function deviate from Eq. (6). It is worth deriving the real transfer function in order to optimize the performance of resonators, and therefore, it will be deduced by

taking account of the finite gain (A_o) and unit-gain bandwidth (GBW) of the operational amplifier.

From Fig. 6, in the period $t_{n-1} < t \leqslant t_{n-1/2}$,

$$v_o(t) = \frac{1}{p} v_X \left(1 - e^{-u(t)}\right) + v_{o,n-1} e^{-u(t)}, \quad (7)$$

$$v_a(t) = \left[\frac{1+b}{p} - \left(\frac{1+b}{p} - \beta\right) e^{-u(t)}\right] v_X + (1 + b - p\beta)\, e^{-u(t)} v_{o,n-1}, \quad (8)$$

where $\beta = \dfrac{C_{a,b}}{C_s + C_{a,b}}$, $p = 1 + \dfrac{1}{\beta A_o}$, $b = \dfrac{1}{A_o}$, $v_X = -v_{a,n-2} - \dfrac{C_s}{C_{a,b}} v_{i,n-1}$, $u(t) = p\beta \cdot \mathrm{GBW} \cdot (t - t_{n-1})$. According to $a_1 = 1/3$ and $a_2 = 3/4$, the feedback factors (β) are 3/4 and 4/7 for the first and second resonators, respectively.

In addition, in the period $t_{n-1/2} < t \leqslant t_n$,

$$v_a(t) = v_{a,n-1/2}, \quad (9)$$

$$v_o(t) = \frac{1}{b+1}\left(1 - e^{-y(t)}\right) v_{a,n-1/2} + e^{-y(t)} v_{o,n-1/2}, \quad (10)$$

where $y(t) = (b+1) \cdot \mathrm{GBW} \cdot \left(t - t_{n-1/2}\right)$.

Therefore, replacing $t - t_{n-1/2}$ by $T_s/2$ and taking the z-transform of Eqs. (7)–(10), the real response of the resonator $H_r(z)$ can be described as

$$H_r(z) = \frac{C_s}{C_{a,b}} \left[\frac{1}{p} - \left(\frac{1}{p} - \frac{\beta}{1+b}\right) e^{-\alpha} - \frac{\beta}{1+b} e^{-(\alpha+\gamma)}\right] z^{-1} \times \left\{1 - \left[\left(1 - \frac{p}{1+b}\beta\right) e^{-\alpha} + \frac{p}{1+b}\beta e^{-(\alpha+\gamma)}\right] z^{-1} + \left[\frac{1+b}{p} - \left(\frac{1+b}{p} - \beta\right) e^{-\alpha}\right] z^{-2} - \beta e^{-(\alpha+\gamma)} z^{-3}\right\}^{-1}, \quad (11)$$

where $\alpha = p\beta \cdot \mathrm{GBW} \cdot T_s/2$, $\gamma = (b+1) \cdot \mathrm{GBW} \cdot T_s/2$, and T_s is the sampling period. If $A_o \to \infty$ and GBW $\to \infty$, Equation (11) becomes the ideal case in Eq. (6).

Figure 7 shows the SNR dependence on A_o and GBW simulated by the behavioral model in Fig. 2 with the transfer function (6) replaced by Eq. (11). The figure shows that A_o has little influence on the SNR, and the SNR degrades significantly when GBW decreases. In order to reserve sufficient design margin, A_o and GBW of the first and second resonator are set to 70 dB/850 MHz and 70 dB/1100 MHz, respectively. Due to smaller sampling capacitance and smaller β in the second resonator as addressed above, the equivalent capacitive load of the second resonator is less than that of the first one. As a result, the design of the OTA in the second resonator is more relaxed. In order to achieve high gain, high bandwidth as well as large output swing, the operational amplifiers in resonators are implemented using a two-stage topology, which is shown in Fig. 8.

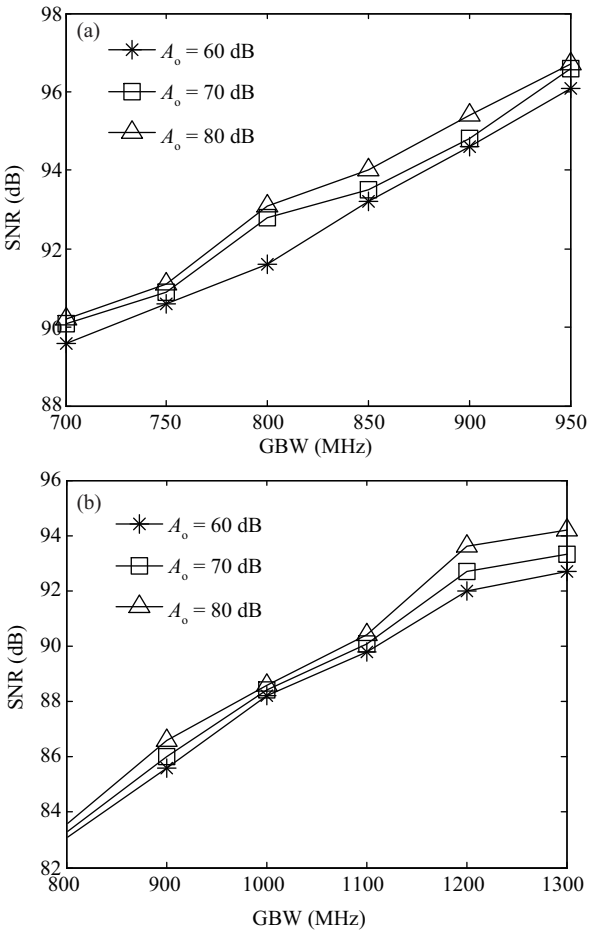

Fig. 7. SNR versus A_o and GBW. (a) OTA in the first resonator. (b) OTA in the second resonator.

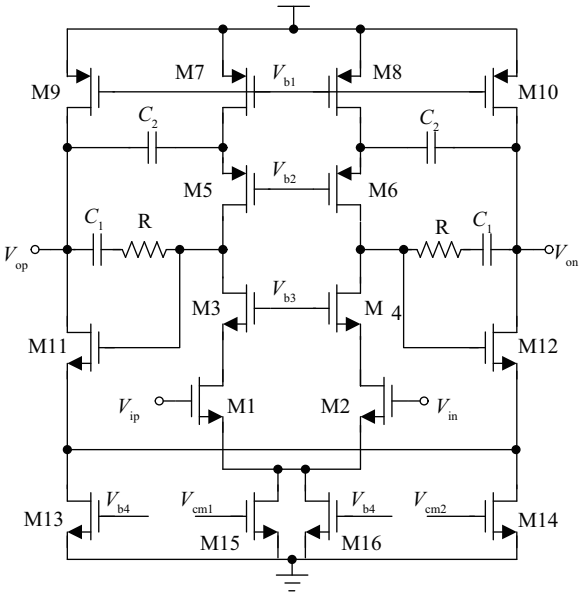

Fig. 8. Two-stage OTA used in resonator.

3.4. One-bit quantizer

Since the nonidealities of the comparator experience noise-shaping the same as the quantization noise, the design requirement of a 1-bit quantizer can be relaxed in the ΣΔ modulator. A fully differential dynamic comparator[5] with switched current sources loaded with a CMOS latch is used, as shown in Fig. 9. In this DT ΣΔ modulator, SNDR does not degrade even with a half period delay, while in a CT ΣΔ modulator, the signal-dependent delay can significantly degrade SNDR as

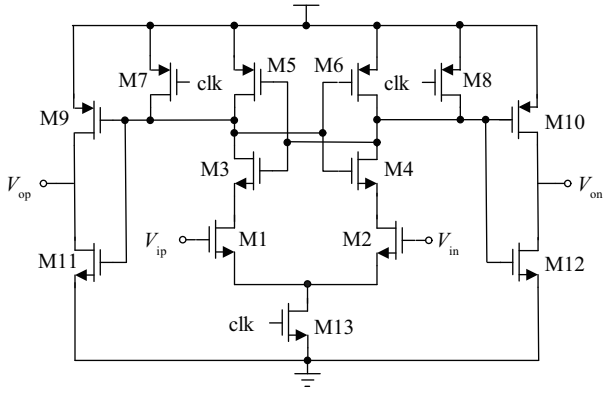

Fig. 9. Schematic of the comparator.

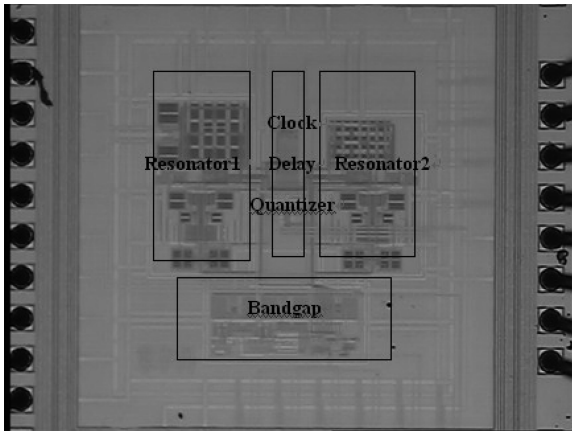

Fig. 10. Chip microphotograph.

Table 1. Performance summary.

Parameter	Value
Sampling frequency	100 MHz
Bandwidth	200 kHz
OSR	250
SNDR	68 dB
Dynamic range	75 dB
Power consumption	8.2 mW

a similar effect of clock jitter[6].

4. Experiment and measurement results

The designed bandpass ΣΔ modulator is implemented in a 0.13-μm standard CMOS process. The die photograph is shown in Fig. 10, and the modulator occupies an area of 0.47 mm^2. Figure 11 shows a typical output spectrum with a 25.08-MHz input signal, which is calculated by a 131072–point fast Fourier transform (FFT) from measurement data. Figure 12 shows the measured SNDR curve over a 200 kHz (GSM) signal bandwidth. The SNDR is calculated without f_s/4-clock feedthrough and image [2].The measured peak SNDR and DR are 68 dB and 75 dB, respectively. The performance is summarized in Table 1.

The figure of merit (FoM) is defined as[6]

$$\mathrm{FoM} = \frac{P}{2\mathrm{BW} \cdot 2^{(\mathrm{DR}-1.76)/6.02}}, \qquad (12)$$

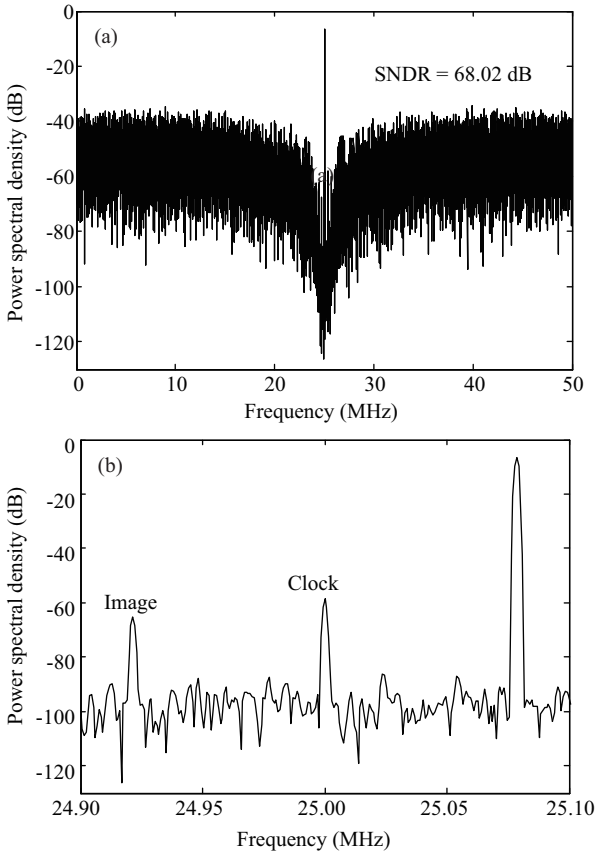

Fig. 11. Output spectrum with 25.08-MHz input signal.

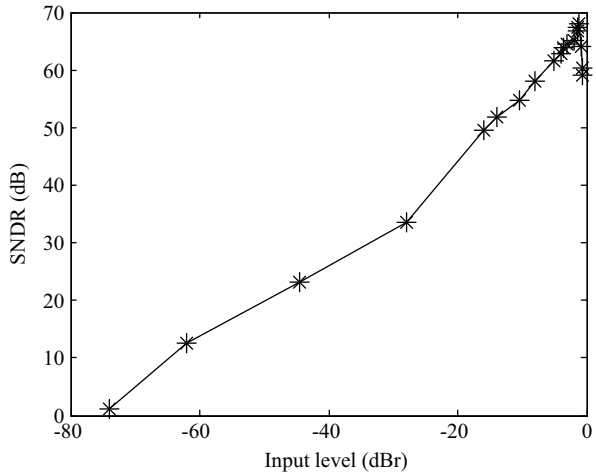

Fig. 12. Measured SNDR curve over a 200-kHz signal bandwidth.

where P is the power dissipation. Table 2 shows a comparison of performance with recently published bandpass ΣΔ modulators. The designed modulator achieves an FoM of 4.46 pJ/level, which is the lowest among these bandpass ΣΔ modulators.

5. Conclusion

This paper presents the design of a 100-MHz bandpass ΣΔ modulator in a 0.13-μm standard CMOS process. A 4th-order switched-capacitor loop filter is implemented to perform noise shaping. The nonidealities of the operational amplifier are analyzed to optimize the performance of resonators. The mea-

Table 2. Performance comparison.

Reference	Technology	BW (kHz)	SNDR (dB)/DR (dB)	Power (mW)	FoM (pJ/level)
Ref. [2], 2002	0.35 μm/3.0 V	270	72/84	56	8.01
Ref. [7], 2005	0.35 μm/3.3 V	200	66/69	45	48.84
Ref. [8], 2008	0.15 μm/3.3 V	200	79/94	208	12.69
This work	0.13 μm/1.2 V	200	68/75	8.2	4.46

surement results show that this modulator achieves an SNDR of 68 dB, the dynamic range of 75 dB, and dissipates 8.2 mW at a 1.2 V supply. The performance comparison demonstrates that this modulator has optimized performance. It is suitable for digital IF receivers implemented in deep-submicron CMOS technology.

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