Novel SEU hardened PD SOI SRAM cell

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Abstract: A novel SEU hardened 10T PD SOI SRAM cell is proposed. By dividing each pull-up and pull-down transistor in the cross-coupled inverters into two cascaded transistors, this cell suppresses the parasitic BJT and source-drain penetration charge collection effect in PD SOI transistor which causes the SEU in PD SOI SRAM. Mixed-mode simulation shows that this novel cell completely solves the SEU, where the ion affects the single transistor. Through analysis of the upset mechanism of this novel cell, SEU performance is roughly equal to the multiple-cell upset performance of a normal 6T SOI SRAM and it is thought that the SEU performance is 17 times greater than traditional 6T SRAM in 45nm PD SOI technology node based on the tested data of the references. To achieve this, the new cell adds four transistors and has a 43.4% area overhead and performance penalty.

Key words: SEU; PD SOI SRAM; parasitic BJT; mixed-mode simulation
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1. Introduction

Since its first observation in 1975[1], single-event upset (SEU) has become a major problem for the micro-electronic devices in orbit systems. When the particle is incident in the IC, the very high density of electron-hole pairs (EHP) created along the ion track and the electric field is distorted, there is a funneling effect[2] and a large amount of charge may be collected along several microns of the ion track in bulk devices. The collected charge forms current and makes the SRAM cell flip. To minimize this reliability problem, silicon on insulator (SOI) technology is widely used in aerospace and radiation environments. SOI technology is the full dielectric isolation between individual transistors, which replaces the classical reversed biased junctions of bulk technologies. This structure has three advantages over bulk technology in radiation environments[3]. (1) It avoids any possibility of latch-up by suppressing the parasitic thyristor structure (npnp layers). (2) By reducing the silicon volume in which radiation generates carriers, it reduces the sensitivity to transient irradiations. (3) No funneling effect can occur, the sensitive regions of the transistors are insulated by a dielectric film that prevents carrier flow from the substrate. However, for partly depleted (PD) SOI, whether a floated or body-tied transistor, its parasitic bipolar junction transistor (PBJT) effect[4] is more serious than in bulk when the ion injects into the sensitive region. Moreover, as technology is scaled down, source-drain penetration charge collection[5] and the PBJT effect will become increasingly serious in PD SOI transistors.

To address the above single-event effect (SEE) weakness, this paper proposes a novel body-separated 10T PD SOI SRAM cell. It can suppress PBJT and the source–drain penetration charge collection effect and so SEU performance will be improved.

2. SEU in PD SOI SRAM

A typical 6T PD SOI SRAM cell is shown in Fig. 1(a). Two cross-coupled inverters constitute a bi-stable structure and T5 and T6 control the read/write access. Assume Q = 1 and QB = 0, T1 and T4 are cutoff; T2 and T3 are turned on. In this case, the body of T1 and T4 is the SEU sensitive region. For write enable and read stability[6], the drive ability of the pull-down transistor usually is four times grater than the pull-up transistor, so the body of the T1 is the most SEU sensitive region for the weaker restore ability of pull-up transistor. When the ion strikes the body, high density EHP is generated in the channel and introduces a low resistance state between source and drain[7]. This effect can be observed in Fig. 1(b) that gives the cross section of T1 and will generate a current from source to drain for the high potential of the drain. Figure 1(b) gives the PD SOI NMOS that is separated by the buried oxide (BOX) from the substrate and has an isolated neutral body region, the PMOS has the same structure. This isolated body region will form the base of the PBJT and is usually connected to the fixed level by a high resistance body-tie or floated. The electrons of high density EHP in the body region disappear by recombination and are collected by source and drain quickly. However, the holes can only be removed by slow recombination or removed by a high resistance body-tie. This will enhance the potential of the body, i.e. base electrode, and trigger horizontal PBJT in an SOI transistor. The current of the low resistance and the PBJT will degrade the SEU performance of the SOI SRAM. As technology is scaled down, the channel length will become smaller and smaller, i.e. the base electrode of the PBJT is shortened, so the PBJT effect becomes more and more serious[5]. This PBJT current is shown in Fig.1 (a) as I_Q and the restore transistor T3 will compensate this current. However, its drive ability is limited and the current flow through T3 will reduce the Q voltage level. If this low voltage passes through the

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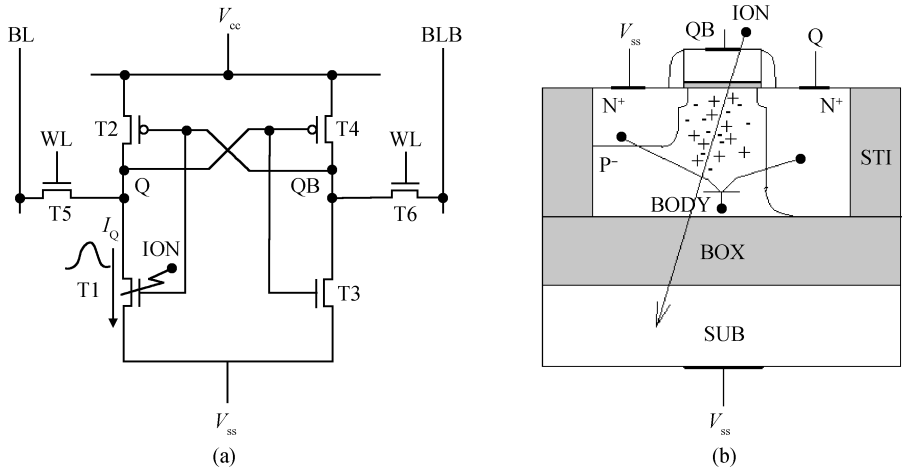

Fig. 1. (a) Typical PD SOI 6T SRAM cell. (b) Cross-section of the struck device, PD SOI NMOS.

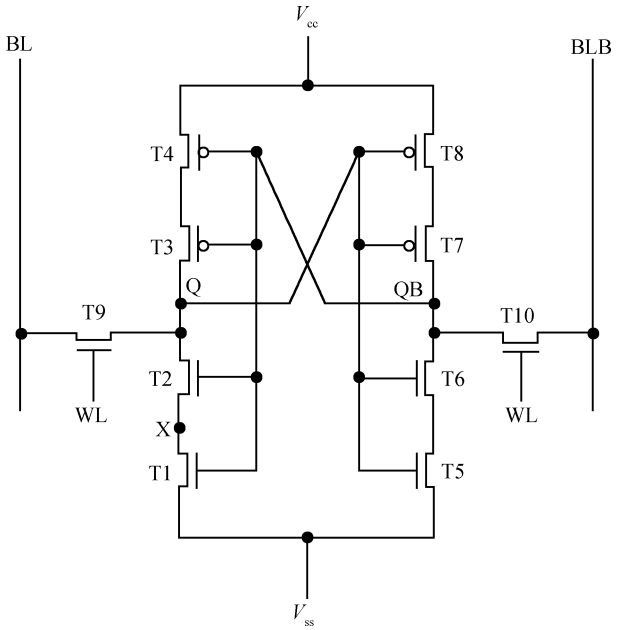

Fig. 2. Novel 10T SEU hardened PD SOI SRAM cell.

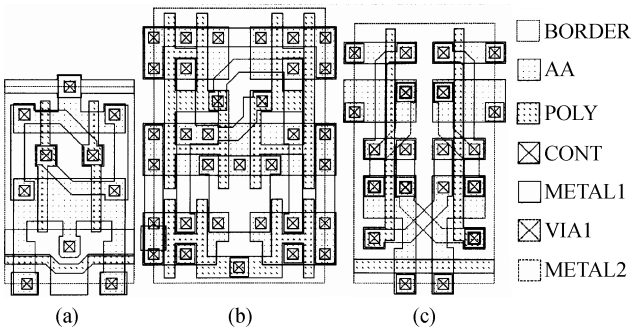

Fig. 3. (a) Floated 6T cell. (b) Body-tied H gate cell. (c) Novel floated 10T cell.

inverter consisted by T2 and T4 and is fed back to the gate of T1 and T3, the cell will flip. Otherwise this cell will restore the original storage state[8].

3. 10T PD SOI SRAM cell

Based on previous analysis, the SEU performance will worsen and worsen as the technology is scaled down for PD SOI SRAM. For this reliability problem, this paper proposes a novel 10T PD SOI SRAM cell. It greatly reduces the amount of collection charge induced by the ion and completely avoids the SEU for the particle-affect one-transistor situation.

Figure 2 gives the schematic of this novel cell. It divides the pull-up and pull-down transistors into two cascaded transistors and has the same read/write access as the conventional 6T cell.

The SEU hardened mechanism for this novel cell is analyzed below. Assume $Q = 1$ and $Q_B = 0$ in Fig. 2, so the cut-off cascaded T1, T2 and T7, T8 are the sensitive transistor for the cell. When the ion strikes the body region of the T1, it will affect the level of the intermediate node X and discharge X to low level, but this will not affect the node Q. When the ion strikes the T2, node Q will discharge to X but not ground. So the level variation of the node Q depends on the capacitance of the node Q and X. Assuming the worst case, node X is low and ignoring the recovery of T3 and T4 current, the particle impact is long enough to make the X and Q in the same voltage level. According to capacitance equation (1), the voltage of the node can be determined.

$$V_Q = \frac{C_Q V_{dd}}{C_Q + C_X}, \tag{1}$$

where V_Q is the voltage level of the node Q and C_Q and C_X are the capacitance of node Q and X, respectively. Figure 2 shows that the node X only contains two drain PN junction capacitances but the node Q contains four gate capacitances and two drain PN junction capacitances. For PD SOI technology, the PN junction is smaller than gate capacitance. According to 0.35 μm PD SOI technology and the transistor's dimension shown in Fig. 3, the capacitance of C_Q is six times greater than C_X. So, based on Eq. (1), V_Q only degrades to $\frac{6}{7} V_{dd}$, far smaller than the flipping voltage. When $Q = 0$ and $Q_B = 1$, similar analysis can be made.

According to the above analysis, this novel cell divides one SEU sensitive body region into two body regions. These two

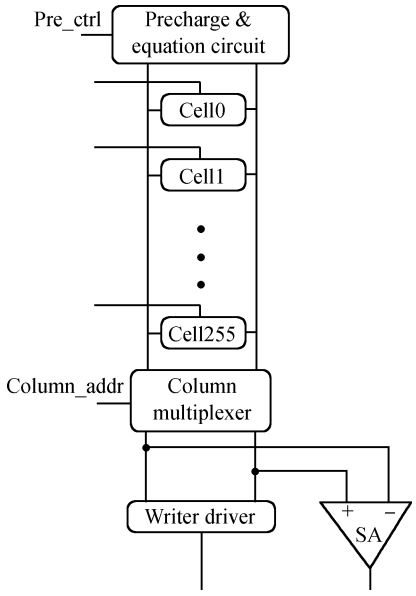

Fig. 4. Simulation schematic of the read/write.

body regions decouple the storage node to the power rail. Regardless of where the particle strikes the body area, the cell will not flip.

4. Simulation results

Figure 3 gives the layout of the three SRAM cells. Figure 3(a) is a conventional floated 6T cell layout and the pull-up, pull-down and access transistor's dimensions are $4.6\lambda/2\lambda$, $9.2\lambda/2\lambda$, $4.6\lambda/2\lambda$, respectively, λ is the half of the minimum channel length. Figure 3(b) is H gate body-tied 6T cell layout and the transistor's dimensions are the same as Fig. 3(a). Figure 3(c) is the novel 10T floated cell and the transistor's dimensions are $4.6\lambda/2\lambda$, $9.2\lambda/2\lambda$, $4\lambda/3\lambda$, respectively. The area of these three layouts from (a) to (c) is $24.4\lambda \times 36.8\lambda = 898\lambda^2$, $32.4\lambda \times 51.6\lambda = 1672\lambda^2$ and $25.1\lambda \times 51.3\lambda = 1288\lambda^2$, respectively. This cell saves 23.0% area compared with the H gate cell, but has 43.4% area overhead compared with a floated 6T cell. In Fig. 3(c), the cascaded pull-down and pull-up transistors are physically separated, this can effectively reduce the possibility that the cascaded transistors are affected by one high energy or a grazing ion. Based on 0.35 μm PD SOI technology, the RC post net-lists are extracted for the layout of Fig. 3 and we perform simulations to compare these three cells.

4.1. Read/write performance and static noise margin simulation

The read/write performance is simulated by H-spice and the transistor model is BSIM3SOI. The simulated circuit is a memory bank formed by 256 row × 256 column cells. One of the columns is illustrated in Fig. 4.

Read static noise margin (SNM) is the metric used in this paper to characterize that the stability of the SRAM cells for read access has the minimum SNM. The SNM is defined as the minimum noise voltage necessary to flip the state of a SRAM cell. So the read SNM is the side length of the maximum nested square between the voltage transfer characteristics of the two data storage nodes[9]. The simulation results are shown in Table 1.

Table 1. Read/write performance and read SNM.

Cell type	Floated 6T cell	H gate 6T cell	Floated 10T cell
Write time (ns)	0.25	0.27	0.35
Read time (ns)	0.30	0.35	0.40
Read SNM (V)	0.54	0.53	0.54

The simulation results show that the read time is slower than the write time, so the read time decides the access cycle. The floated 10T cell's read time is greater than the floated 6T cell by 33%, so this novel cell has a 33% performance penalty. This is because the drive ability of the access transistor is weaker than the floated 6T cell for the area tradeoff. If the width of the floated 10T cell is properly increased, this cell could also reach a high performance. In terms of read SNM, the three cells have little difference, as shown in Table 1.

4.2. SEU performance simulation

Based on the technology parameter provided by 0.35 μm process line, the 2D model of the NMOS is made by Sentarus Structure Editor. The basic technology parameter is shown in Table 2.

The heavy ion vertically strikes the chip surface and the photo-generation model uses a Gaussian radial distribution of charges with a fixed characteristic radius of 0.1 μm[10]. Incidence position locates at the middle of the channel.

To float the 6T cell, a 100 MΩ resistor concatenates between the body and the ground to simulate the floated situation. Figure 5(a) shows the current density initial set up and 40 ps after the ion strike in drain. The current density in Fig. 5(a) shows that the diameter of influence by the ion is close to the channel length and will induce a source drain penetration effect. 40 ps after the ion strike in drain, the electrons have disappeared but the holes still elevate the body potential and the PBJT sustains the source-to-drain current. Simulations obtain that the threshold of linear energy transfer (LET) is 0.056 pC/μm and the critical charge is 24 fC.

In the body-tied H gate cell, a 4 kΩ resistor concatenates between the body and the ground to simulate the body-tied situation. Simulations obtain that the threshold of LET is 0.094 pC/μm, the critical charge is 74 fC. At the location in which the ion strikes is the furthest from the body-tie, the body-tie effect is not obvious and the high LET threshold is caused by a larger storage node capacitance than in the floated 6T cell. Figure 5(b) gives the SEU current and the storage node voltage curve.

In the floated 10T cell, T1 and T2 are replaced by 2D NMOS physical device model. When the ion strikes the body of the T1, the voltage of the Q does not alter sweeping the LET from 0.05 to 0.8 pC/μm. When the ion strikes the body of the T2, the voltage of the Q drops 0.3 V and the cell does not flip sweeping the LET from 0.05 to 0.8 pC/μm. When two ions strike the bodies of the T1 and T2, respectively, and sweep the ion energy from 0.05 to 0.8 pC/μm, the simulation results show that the upset depends on the lower energy particle. When this lower energy particle's LET is larger than 0.12 pC/μm, this 10T

Table 2. Technology parameters.

Parameter	Silicon film	Gate oxide	BOX	Channel dope concentration	Min gate length	V_{dd}	Transistor structure
Value	200 nm	7 nm	375 nm	4.3×10^{17} cm^{-3}	0.35 μm	3.3 V	BUSFET

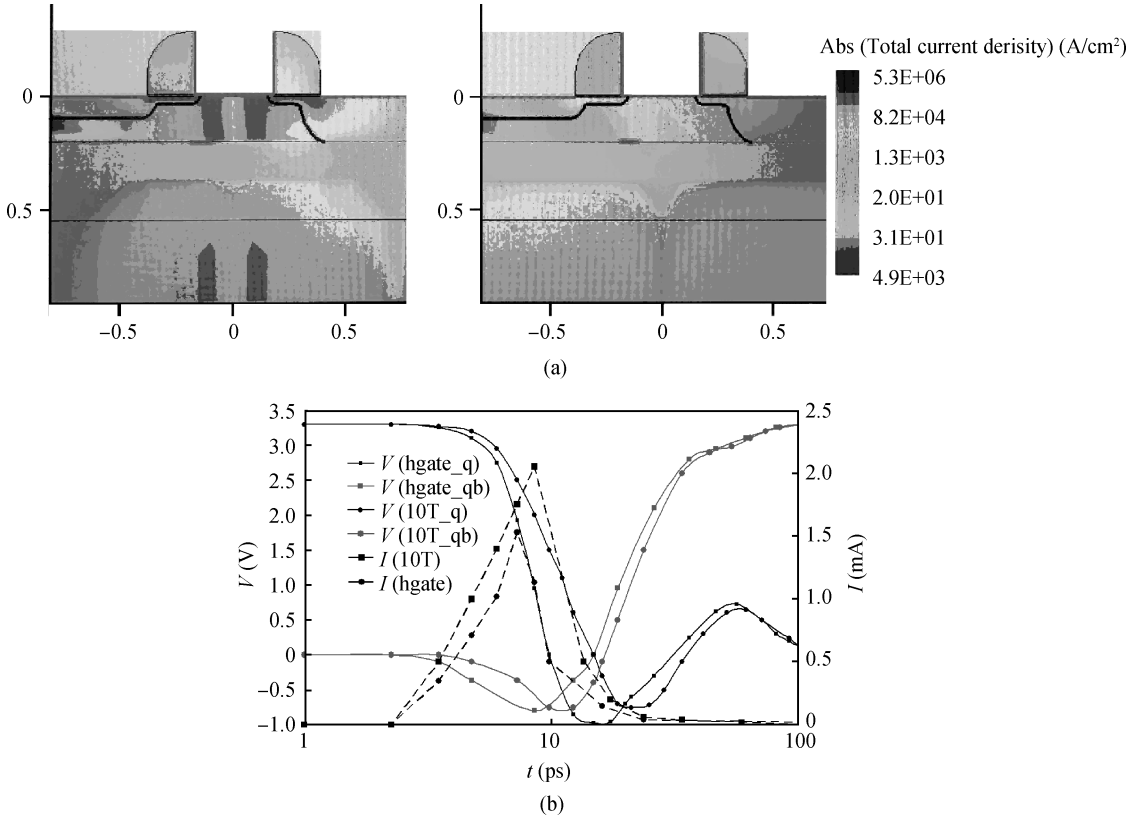

Fig. 5. (a) Current density when the ion strikes the drain and 40 ps after the strike. (b) Current and node voltage upset curve.

cell will upset, otherwise, no upsets occurs. Figure 5(b) gives the SEU current and the storage node voltage curve. Integrating the current curve obtains that the critical charge of the 10T cell is 114 fC.

4.3. SEU performance compared with normal 6T floated SOI SRAM cell

Normal 6T floated SOI SRAM is most prevalent in PD SOI technology and can also cause multiple-cell upsets (MCU) such as in bulk technology. Two mechanisms usually cause the MCU in SOI SRAM. One is that the particle strikes the chip surface with a large angle. The other is that the particle generates the second particle and it affects the other cell. These two cases are illustrated in Fig. 6. M1 represents the SEU sensitive transistor of the cell A, M2 is the sensitive transistor of the cell B. Ion1 represents the large angle particle which affects the cell A and cell B simultaneously and so causes the MCU in SRAM array. Ion2 strikes the cell A's sensitive transistor and generates the second ion, which affects the sensitive transistor of cell B and so Ion2 can introduce the MCU too. T is the space of the two sensitive transistors and the larger the T, the smaller the probability of an MCU.

The MCU for a normal 6T cell and the single cell upset (SCU) for the novel 10T cell have the same characteristics in that one particle affects the two sensitivity transistor simultaneously. The last mechanism which will induce the SCU of this novel cell is where two particles simultaneously strike the two sensitive transistors in the same cell. Compared with the first two mechanisms, this last mechanism can be ignored due to its very low probability[11]. In addition to the mechanism being similar, these two upsets (MBU for 6T and SCU for novel 10T) have the familiar layout as illustrated in Fig. 7.

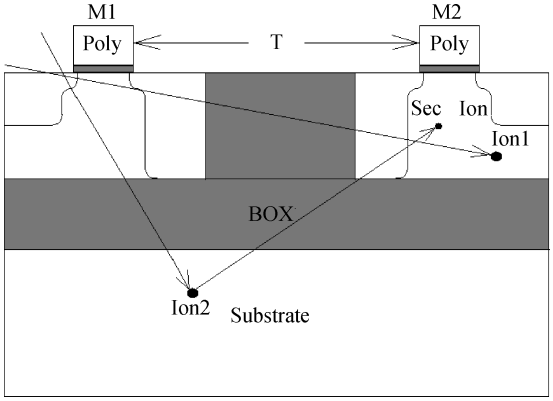

Fig. 6. Two mechanisms that can cause MCU in normal 6T floated SOI SRAM.

Figure 7(a) shows the 65 nm 6T cell array and the black

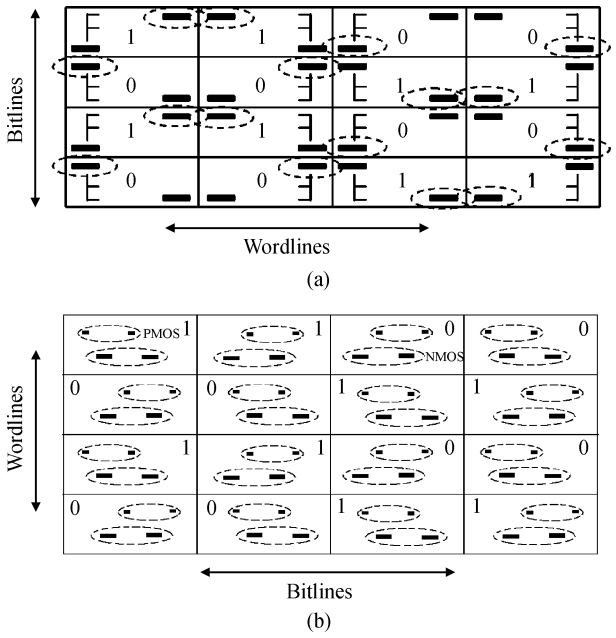

Fig. 7. (a) Layout of normal 6T SOI SRAM array. (b) Layout of novel 10T SOI SRAM array.

region is the sensitive transistor[11]. In each cell, the sensitive transistors of the pull-down device are circled. In Fig. 7(a), the adjacent black regions are likely affected by one particle and generate MCU. Figure 7(b) shows the 65 nm novel 10T cell array and the black region is the sensitive transistor. This novel 10T cell is radiation hardened by design and process independent, and through careful cell design, it can adapt to any technology. In Fig. 7(b), each cell has the two sensitive transistors of a pull-down device and the two sensitive transistors of the pull-up device are circled. Only if the two transistors in the circle are affected simultaneously, will the cell upset.

According above analysis, the novel 10T SOI SRAM cell's SCU is very similar to the MCU of the normal 6T SOI SRAM cell and so the SCU of the novel cell is roughly equal to the MCU of a 6T cell. In 0.35 μm PD SOI technology, the sensitivity transistors are too far away to cause MCU for 6T cell, so the SCU probability of this novel cell is very small. However, due to aggressive developments in technology, the space of the two SEU sensitivity transistors is becoming smaller and smaller and occurrences of MCU in normal 6T floated SOI SRAM cells is more and more prevalent, so the SCU probability in this novel cell will become larger too.

In two recent publications, the ratio of MCU-to-SCU was measured to be approximately 1% in 65 nm[11] and approximately 6% in 45 nm SOI SRAM[12] under exposure to high energy protons. Based on Ref. [11], the SEU sensitivity regions are adjacent, as illustrated in Fig. 7(a), so the normal 6T SOI SRAM cell has a high probability of MCU. However, in this novel 10T floated SOI SRAM cell, as illustrated in Fig. 7(b), the SEU sensitivity regions in one cell are separated by the non-sensitivity transistor, as illustrated in Fig. 3(c). Based on above analysis, a conservative estimation is that the SCU performance for this novel 10T cell is 100 times greater than a 6T floated cell in 65 nm SOI technology and 17 times greater in 45 nm technology.

5. Summary

This paper proposed a novel 10T SEU-hardened SRAM cell suited for PD SOI technology. By separating the pull-up and pull-down transistor in the cross-coupled inverters into two cascaded transistors, this novel cell separates the storage node from the power rail and so suppresses the PBJT and the source-drain penetration charge collection effect in a PD SOI transistor. This cell has 37% area overhead and a read/write performance penalty of 33% compared to conventional 6T floated cell but sensitivity to SEU down to 6% of the 45 nm SOI technology node. Only when the serious cut-off transistors are affected simultaneously, will this cell flip. So by spacing out the serious cut-off transistors in the layout, this cell can reduce sensitivity further. Based on the above analysis, this SEU-hardened novel PD SOI 10T cell is well suited for operation under transient irradiation, in military or space applications.

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