A 150% enhancement of PMOSFET mobility using hybrid orientation*

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Abstract: A high-performance PMOSFET based on silicon material of hybrid orientation is obtained. Hybrid orientation wafers, integrated by (100) and (110) crystal orientation, are fabricated using silicon–silicon bonding, chemical mechanical polishing, etching silicon and non-selective expitaxy. A PMOSFET with $W/L = 50\ \mu$m/8 μm is also processed, and the measured results show that the drain–source current and peak mobility of the PMOSFET are enhanced by up to 50.7% and 150% at $V_{gs} = -15$ V and $V_{ds} = -0.5$ V, respectively. The mobility values are higher than that reported in the literature.

Key words: hybrid orientation; non-selective expitaxy; carrier mobility; (110) crystal orientation; PMOSFET; chemical mechanical polishing

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1. Introduction

With the rapid development of high-speed scaled CMOS devices, the most important challenge is how to enhance electron or hole carrier mobility. Under normal conditions, NMOSFET carrier mobility is two to three times greater than PMOSFET carrier mobility, because electron mobility (μ_n) is almost three times greater than hole mobility (μ_p). Thus optimization of the materials, processes and structures to enhance the mobility of PMOSFET has become an important issue in the microelectronics domain. In Ref. [1], a strained-Si structure and PMOSFET strained-Si/SiGe on insulator substrate are used, and the μ_p of the PMOSFET is enhanced by 30%. In Ref. [2], which is based on strained-Si and the Ge content in the relaxed $Si_{1-x}Ge_x$ buffer layer, when compared to PMOSFETs with $x = 0.1$, PMOSFETs with $x = 0.22$ and 0.29 exhibit μ_p enhancement factors of 1.4 and 1.8, respectively. Obviously the strained-Si and relaxed SiGe buffer layer are attractive for the enhancement of μ_p. At the same time, μ_p in the (110) crystal orientation wafer is about two times larger than that in the (100) wafer, as reported in the literature. However, μ_n will reduce by 30%–40% and hybrid orientation is seen to hold the advantage of PMOSFET and NMOSFET.

In this paper, based on hybrid orientation technology, a high-performance PMOSFET is developed and reported. By using silicon–silicon bonding, chemical mechanical polishing (CMP), etching silicon and non-selective expitaxy, a hybrid orientation wafer integrated by (100) and (110) is fabricated. In order to validate the characteristics of the wafer, a long channel PMOSFET with $W/L = 50\ \mu$m/8 μm was processed and measured. At the end of this paper, the drain–source current (I_{ds}) and μ_p are also analyzed.

2. Hybrid orientation wafer

Using a hybrid orientation wafer integrated by (100) and (110) is key to enhancing the carrier mobility of the electron and hole. While in (110) orientation, the μ_n will reduce. Consider application in high-speed scaled CMOS devices: the (100) orientation wafer is selected to process the substrate and the (110) orientation wafer is chosen to form the top silicon layer.

Figure 1 is a sketch map of the process flow of the hybrid orientation wafer, which is integrated by (100) and (110). With

(a) Silicon–silicon bonding
Substrate wafer: (100) orientation, 7–10 Ω•cm.
Top wafer: (110) orientation, 10–20 Ω•cm.
Oxide thickness: 200–300 nm.

(b) Chemical mechanical polishing (CMP)
Top silicon: (110) orientation wafer.
Top silicon: left 3–4 μm.

(c) Etch silicon
Etch top silicon: 3–4 μm.
Etch oxide: 200–300 nm.
No etch: fabricate PMOSFET area.

(d) Non-selective expitaxy
Expitaxy thickness: 7–8 μm.

(e) Chemical mechanical polishing (CMP)
CMP thickness: 2–3 μm.

Fig. 1. Sketch map of the process flow of the hybrid orientation wafer integrated by (100) and (110).

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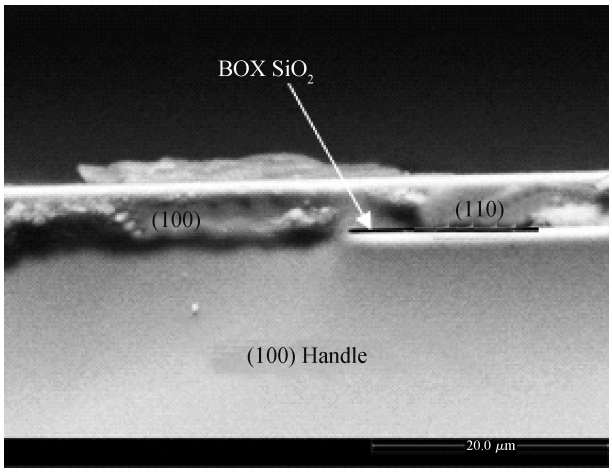

Fig. 2. SEM photo of the hybrid orientation wafer cross structure.

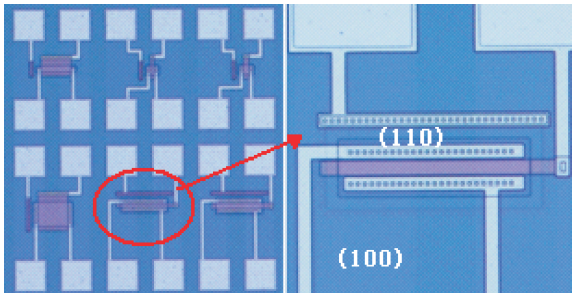

Fig. 3. Partial photograph of the hybrid orientation wafer.

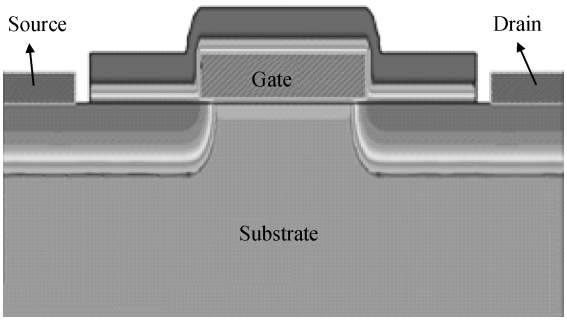

Fig. 4. The simulated cross structure of the PMOSFET.

this flow, the hybrid orientation wafer can be obtained. Figure 2 is an SEM photo of the cross structure of the hybrid orientation wafer, and Figure 3 is a partial photograph of the hybrid orientation wafer.

From Figs. 2 and 3, the substrate of the hybrid orientation wafer is the (100) orientation wafer, and the (110) orientation wafer is chosen to fabricate the top silicon layer.

3. PMOSFET design and validation

3.1. PMOSFET design

In order to validate the characteristics of the hybrid orientation wafer, the poly-silicon gate self-aligned structure of a PMOSFET is designed and processed. The simulated cross structure is shown in Fig. 4, and Table 1 lists the simulated results of a PMOSFET fabricated on a (100) and (110) wafer.

Table 1. Simulated results of a PMOSFET fabricated on a (100) and (110) wafer.

Parameter	Condition	(100)	(110)
Gate oxide (nm)	—	44.8	61.9
Source depth (μm)	—	0.71	0.71
Threshold voltage (V)	$V_{ds} = -0.5$	–1.24	–1.36

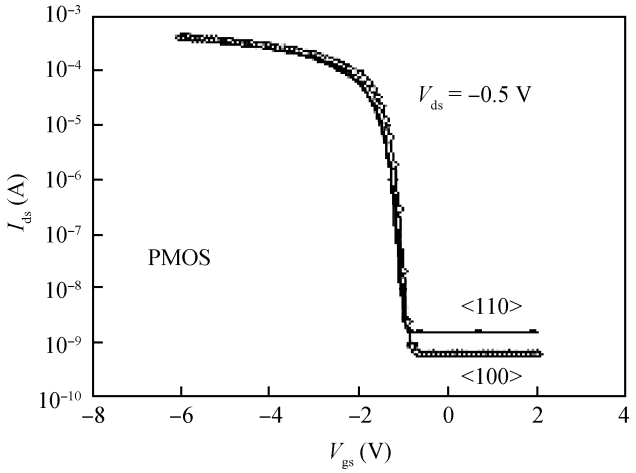

Fig. 5. The contrastive curves of the transfer characteristics of the PMOSFET fabricated on the (110) and (100) wafers (I_{ds} and V_{gs} at $V_{ds} = -0.5$ V).

The actual process flow is described as follows.

A hybrid orientation wafer integrated with (110) and (100) → field oxide → P well photo/etch → thin oxide → P well boron implant → anneal → strip oxide all → thin oxide → P+ ring lithography → P+ ring implant → N+ ring lithography → N+ ring implant → LPCVD deposit SiO_2 → anneal → active lithography/etch → NMOSFET threshold voltage adjust lithography → phosphorus implant → gate oxide LPCVD deposit poly-silicon → poly-silicon lithography/etch → poly-silicon oxide → P source/drain lithography → BF_2 implant → N source/drain lithography → phosphorus implant → LPCVD deposit SiO_2 → anneal → contact lithography/etch → metallization → testing → alloy → passivation → PAD lithography/etch → re-alloy → parameter testing.

3.2. Validation

By adopting the hybrid orientation wafer and mentioned flow, a high-performance PMOSFET is fabricated. At the end, the characteristics of the devices are measured by a Keithley 4200-SCS at 25 ℃ in air. Figure 5 shows the contrastive curves of the transfer characteristics of the PMOSFET at $V_{ds} = -0.5$ V, which are fabricated in (100) and (110) orientation, respectively. Figure 6 shows the contrastive curves of the output characteristics of the two orientations of the PMOSFET when V_{gs} changes from 0 to –15 V at the –3 V step. Figure 7 shows the ratio curves of the mobility and I_{ds} of the PMOSFET at $V_{gs} = -15$ V.

From Fig. 5 to Fig. 7, the I_{ds} values and the peak mobilities of the PMOSFET processed on the (110) wafer are almost 1.5 and 2.5 times different from the values of the PMOSFET

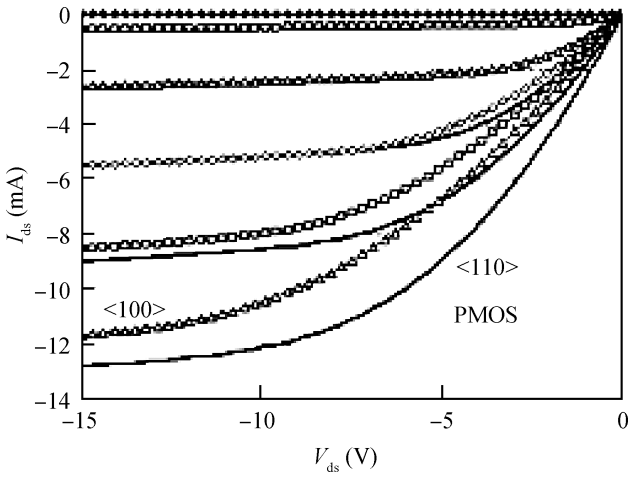

Fig. 6. The contrastive curves of the output characteristics of the PMOSFET fabricated on the (110) and (100) orientation wafers.

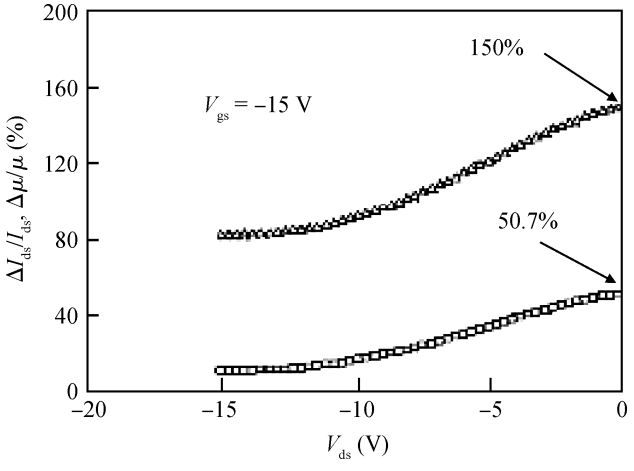

Fig. 7. The ratio curves of the mobility and drain–source current of the PMOSFET fabricated on the (110) and (100) wafers at $V_{gs} = -15$ V.

fabricated on the (100) wafer at $V_{ds} = -0.5$ V and $V_{gs} = -15$ V, respectively.

3.3. Discussion

The drain–source current density and μ_{MAX} of the proposed PMOSFET are improved by 50.7% and 150%, respectively.

By designing the territory, the channel width of the proposed PMOSFET is 8 μm, and the PMOSFETs fabricated in the (100) and (110) crystal orientations are processed with the same suite of masks. Thus the studied PMOSFET can be considered as a long-channel MOS device and the classical square-rule formula can be used, which is shown in Eq. (1).

$$I_{ds} = C_{ox}\frac{\mu W}{L}\left[\left(V_{gs} - V_t\right)V_{ds} - \frac{1}{2}V_{ds}^2\right], \tag{1}$$

where C_{ox} is the capacitance of the poly-silicon gate to the expitaxy layer, μ is the mobility of the carrier, W is the width of the channel, L is the length of the channel, and V_t is the threshold voltage of the gate–source. From Eq. (1), when V_{ds} is higher than $V_{gs} - V_t$, $V_{gs} - V_t$ can be used instead of V_{ds}. Hence, Equation (2) is logical.

$$\frac{I_{ds1}}{I_{ds2}} = \frac{C_{ox1}}{C_{ox2}}\frac{\mu_1}{\mu_2}, \tag{2}$$

where I_{ds1} , C_{ox1} and μ_1 are the drain–source current, the capacitance of the poly-silicon gate to the expitaxy layer, and the mobility of the electron in the channel of the PMOSFET fabricated (110) orientation wafer, respectively. I_{ds2}, C_{ox2} and μ_2 are the drain–source current, the capacitance of the poly-silicon gate to the expitaxy layer, and the mobility of the electron in the channel of the PMOS processed on the (100) wafer, respectively.

From Eq. (2), the C_{ox1} value is not equal to C_{ox2}, and this result from the speed of the oxide grown on the (110) wafer is 1–1.5 times greater than on the (100) wafer. The testing gate oxide thickness on the (110) wafer is 68 nm and the value on the (100) wafer is 41 nm, with both grown in the same process conditions.

$$\begin{aligned}\Delta I_{ds} &= \frac{I_{ds2} - I_{ds1}}{I_{ds1}} = \frac{I_{ds2}}{I_{ds1}} - 1 \\ &= \frac{41}{68}\frac{\mu_2}{\mu_1} - 1 = 50.7\%.\end{aligned} \tag{3}$$

When mentioning the PMOSFET, Eq. (3) to come into existence. The peak current density and the μ_{MAX} of the PMOSFET fabricated on the (110) wafer are enhanced by up to 50.7% and 150% at $V_{ds} = -0.5$ V and $V_{gs} = -15$ V, respectively. These results can also be obtained from Figs. 5 and 6.

4. Conclusion

Using silicon–silicon bonding, CMP, etching silicon and non-selective expitaxy, hybrid orientation wafers integrated with (110) and (100) are obtained successfully. Furthermore, a high-performance PMOSFET is designed and fabricated in the hybrid orientation wafer. Finally, the measured results show that the drain–source current and the peak mobility of the PMOSFET fabricated on the (110) orientation are improved by 50.7% and 150% at $V_{gs} = -15$ V and $V_{ds} = -0.5$ V. The hybrid orientation wafer process and the PMOSFET with mobility enhanced by 150% are advanced and high performance. The PMOSFET and wafer processes can be used to develop high-speed scaled CMOS devices and high-performance MEMS devices.

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