Effect of a gate buffer layer on the performance of a 4H-SiC Schottky barrier field-effect transistor*

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Abstract: A lower doped layer is inserted between the gate and channel layer and its effect on the performance of a 4H-SiC Schottky barrier field-effect transistor (MESFET) is investigated. The dependences of the drain current and small signal parameters on this inserted gate-buffer layer are obtained by solving one-dimensional (1-D) and two-dimensional (2-D) Poisson's equations. The drain current and small signal parameters of the 4H-SiC MESFET with a gate-buffer layer thickness of 0.15 μm are calculated and the breakdown characteristics are simulated. The results show that the current is increased by increasing the thickness of the gate-buffer layer; the breakdown voltage is 160 V, compared with 125 V for the conventional 4H-SiC MESFET; the cutoff frequency is 27 GHz, which is higher than 20 GHz of the conventional structure due to the lower doped gate-buffer layer.

Key words: 4H-SiC; Schottky barrier field-effect transistor; Poisson's equation
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1. Introduction

Silicon carbide (SiC) MESFETs are very attractive for high power microwave devices due to the combination of the high electron velocity, high breakdown strength, and high thermal conductivity of SiC[1]. With the recent progress in SiC epitaxial material and device processes, several improved SiC MESFET structures have been reported[2−4]. However, the improvement of the power density of the above mentioned structures is very limited because there is a potential tradeoff between the further increment of drain current and breakdown voltage: a large drain current requires a large channel doping product and thickness; nevertheless, this will reduce breakdown voltage. Similarly, to increase the operation frequency, the gate length should be reduced; however, this will also degrade the performance of the devices and circuits[5, 6].

In this paper, the performance of 4H-SiC MESFETs are improved by inserting a lower doped gate-buffer layer between the gate and the channel layer, instead of increasing the doping concentration of the channel layer and decreasing the gate length. The analytical models that describe the effect of the inserted gate-buffer layer on the performance of the device are obtained by solving one-dimensional (1-D) and two-dimensional (2-D) Poisson's equations. Based on the analytical models, the drain current and small signal parameters are calculated and analyzed for a 4H-SiC MESFET with a gate-buffer layer of 0.15 μm. Meanwhile, the breakdown characteristics for a 4H-SiC MESFET of the same size are simulated. The results show that not only power but also frequency performance are improved compared with the conventional structure due to the inserted lower doped gate-buffer layer.

2. Analytical models

In order to describe the device operation, the channel current in the channel can be expressed as

$$I_{\rm C} = qWn(x)\mu(E)E(x)[a - h(x)], \tag{1}$$

where q is the magnitude of the electronic charge, W the channel width, a the channel layer thickness, $E(x)$ the lateral electric field strength, and $n(x)$ the electron concentration, x away from the source. $n(x)$ is equal to $N_{\rm D}$, the doping concentration of the channel. $h(x)$ is the thickness of the depletion layer in the channel layer and obtained by solving the 1-D Poisson's equation.

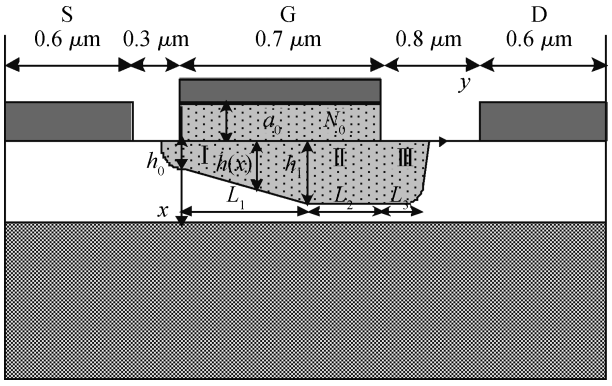

Fig. 1. Schematic diagram of the SiC MESFET with a buffer layer for the saturation regime.

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$$h(x) = a_0 \left(1 - \frac{N_0}{N_D} + \frac{V(x) + V_G + V_{bi}}{\frac{qN_D}{2\varepsilon} a_0^2} \right)^{1/2} - a_0, \quad (2)$$

where N_0 is the uniform doping concentration of the gate-buffer layer, which is smaller than that of the channel N_D. a_0 is the gate-buffer layer thickness, and ε the dielectric constant. $V(x)$ is the potential at the point x away from the source, V_G the gate bias, and V_{bi} the build-in voltage.

When the drain voltage is low, the electric field in the channel is less than the saturation field E_s and only region I exists. Based on the integration over the channel length L, the channel current is obtained as

$$I_C(V_G, V_D) = I_P \times \frac{3(u_d^2 - u_0^2) - 2(u_d^3 - u_0^3) - \frac{3a_0}{a}[(u_d^2 - u_0^2) - 2(u_d - u_0)]}{1 + Z(u_d^2 - u_0^2) + Z\frac{2a_0}{a}(u_d - u_0)}, \quad (3)$$

where $u_0(u_d)$ is the depletion layer width $h_0(h_d)$ at the source (drain) end of the channel normalized to the epilayer channel layer thickness a. I_P and Z are constants.

With the drain bias increasing gradually, the lateral electric field increases and the electron velocity rises toward its saturation value. At enough high drain bias, the channel is in a saturated state, and can be divided into three regions, as shown in Fig. 1. In region I, with its length of L_1 and nearer to the source under the gate, the electric field is low and the electron velocity is less than the saturation velocity (v_s). The saturation region below the gate and the saturation region between the gate and the drain are labeled as regions II and III, respectively. The saturation channel current is

$$I_{csat} = qN_D W a v_s (1 - u_1), \quad (4)$$

where u_1 is the normalized depletion layer thickness at the point where the electron reaches saturation velocity.

$$u_1(V_G, V_D) = \frac{h_1}{a} = \sqrt{\left(1 - \frac{N_0}{N_D}\right)\frac{a_0^2}{a^2} + \frac{V(L_1) + V_G + V_{bi}}{V_p}} - \frac{a_0}{a}, \quad (5)$$

where h_1 is the depletion layer thickness at the point where the electron reaches saturation velocity, $V(L_1)$ is the potential difference between the source and the point at $x = L_1$, where saturation velocity $v(L_1) = v_s$. V_P is a constant.

To obtain the saturation current in the channel, other equations involving u_1 or L_1 are required, which can be found by solving the 2-D Poisson's equation.

The potential drop across regions II and III achieved by solving the 2-D Poisson's equation is

$$V(L + L_3) - V(L_1) = \left[\frac{2(au_1 + a_0)}{\pi} + \frac{L_3}{3}\right] E_s \times \sinh\frac{\pi L_2}{2(au_1 + a_0)} \exp\frac{-\pi L_3}{2(au_1 + a_0)} + \frac{E_s L_3}{3}\left[2\exp\frac{\pi L_2}{2(au_1 + a_0)} + 1\right]. \quad (6)$$

The equation involving L_3 is

$$L_3^2\left\{\frac{qN_D a u_1}{\varepsilon} - E_s \exp\frac{\pi L_2}{2(au_1 + a_0)} + \frac{E_s}{\eta}\sinh\frac{\pi L_2}{2(au_1 + a_0)}\left[1 + \tan\frac{\pi a_0}{2(au_1 + a_0)}\right]\right\} = (au_1)^2 E_s\left[\exp\frac{\pi L_2}{2(au_1 + a_0)} - 1 - \sinh\frac{\pi L_2}{2(au_1 + a_0)}\exp\frac{-\pi L_3}{2(au_1 + a_0)}\right], \quad (7)$$

where

$$\eta = \tan\frac{\pi a_0}{2(au_1 + a_0)}\cos\frac{\pi a u_1}{2(au_1 + a_0)} + \sin\frac{\pi a u_1}{2(au_1 + a_0)},$$

$$V(L + L_3) = V_D - I_C R_D.$$

From the analysis above, the drain current can be achieved when the structure parameters (L, W, a, a_0, N_D, N_0) and bias voltage (V_D, V_G) are given.

To evaluate the high frequency performance conveniently, it is important to describe the small signal parameters analytically.

Based on Eq. (4), the drain conductance for the saturation regime is obtained as

$$g_{ds} = -\frac{3\gamma I_P}{2Zm_{L_1}V_P} f, \quad (8)$$

where

$$f^{-1} = 1 + \frac{1}{2m_{L_1}V_P}\left[\frac{2E_S a}{\pi}\sinh\frac{\pi(L - L_1)}{2(au_1 + a_0)} - \frac{E_S a(L - L_1)}{(au_1 + a_0)}\cosh\frac{\pi(L - L_1)}{2(au_1 + a_0)}\right] - \frac{E_S L Z}{2m_{L_1}V_P}\cosh\frac{\pi(L - L_1)}{2(au_1 + a_0)} \times \left\{\left[\frac{2u_1(1 - \gamma)}{\gamma} + \frac{(u_1^2 - u_0^2) - \frac{2}{3}(u_1^3 - u_0^3)}{\gamma(1 - u_1)^2}\right] - \frac{a_0}{\gamma a}\left[\frac{(u_1^2 - u_0^2) - (u_1 - u_0)}{(1 - u_1)^2} - 2(1 - \gamma)\right]\right\},$$

$$m_{L_1} = u_1 + \frac{a_0}{a}.$$

The expression of transconductance for the saturation regime is

$$g_{\rm ms} = -\frac{3\gamma I_{\rm P}}{2Zm_{L_1}V_{\rm P}}(k+1), \tag{9}$$

where

$$\begin{aligned} h = & -\frac{1}{2m_{L_1}V_{\rm P}}\left[\frac{2E_{\rm S}a}{\pi}\sinh\frac{\pi(L-L_1)}{2(au_1+a_0)} - \frac{E_{\rm S}a(L-L_1)}{au_1+a_0}\right. \\ & \left.\times\cosh\frac{\pi(L-L_1)}{2(au_1+a_0)}\right] + \frac{E_{\rm S}LZ}{2m_{L_1}V_{\rm P}}\cosh\frac{\pi(L-L_1)}{2(au_1+a_0)} \\ & \times\left\{\left[\frac{2u_1(1-\gamma)}{\gamma} + \frac{(u_1^2-u_0^2)-\frac{2}{3}(u_1^3-u_0^3)}{\gamma(1-u_1)^2}\right]\right. \\ & \left.-\frac{a_0}{\gamma a}\left[\frac{(u_1^2-u_0^2)-(u_1-u_0)}{(1-u_1)^2} - 2(1-\gamma)\right]\right\} \\ & -\frac{u_0E_{\rm S}LZ}{m_0V_{\rm P}}\cosh\frac{\pi(L-L_1)}{2(au_1+a_0)} \\ & \times\left[\frac{1-u_0}{\gamma(1-u_1)} - 1\right]\left(1+\frac{a_0}{au_0}\right), \end{aligned}$$

$$k = fh.$$

To find the gate–source capacitance, the magnitude of the charge in the depletion layer under the gate is needed. This can be derived from the potential distribution in the depletion layer. So, the expression of the gate–source capacitance is given as

$$C_{\rm gs} = C_{\rm g1} + C_{\rm g2} + C_{\rm g3}, \tag{10}$$

where

$$C_{\rm g1} = \frac{4\varepsilon WLV_{\rm P}I_{\rm P}}{aID}\left(C_{\rm g11} + C_{\rm g12}\right),$$

$$\begin{aligned} C_{\rm g11} = & -\frac{g_{\rm m}}{I_{\rm D}}\left[\left(1-\frac{a_0}{a}\right)\left(u_1^3-u_0^3\right) - \frac{3}{4}\left(u_1^4-u_0^4\right)\right. \\ & \left.+\frac{3a_0}{a}\left(u_1^2-u_0^2\right)\right], \end{aligned}$$

$$\begin{aligned} C_{\rm g12} = & \frac{3u_1}{2m_{L_1}V_{\rm P}}\left(u_1+\frac{a_0}{a}\right)\left(1-u_1-\frac{ZI_{\rm D}}{3I_{\rm P}}\right)(k+1) \\ & -\frac{3u_0}{2m_0V_{\rm P}}\left(u_0+\frac{a_0}{a}\right)\left(1-u_0-\frac{ZI_{\rm D}}{3I_{\rm P}}\right), \end{aligned}$$

$$\begin{aligned} C_{\rm g2} = & \frac{2\varepsilon WLZu_1}{a}\left\{\frac{g}{2Zm_{L_1}u_1}(k+1) + \frac{u_0}{m_0}\right. \\ & \left.\times\left[\frac{u_1-u_0}{\gamma(1-u_1)} + \frac{1-\gamma}{\gamma}\right]\left(1+\frac{a_0}{au_0}\right)\right\}, \end{aligned}$$

$$C_{\rm g3} = -\varepsilon E_{\rm s}Wa\left(C_{\rm g31} + C_{\rm g32}\right),$$

$$\begin{aligned} C_{\rm g31} = & \frac{k+1}{2m_{L_1}V_{\rm P}}\left\{1-\cosh\frac{\pi(L-L_1)}{2(au_1+a_0)} - \frac{\pi(1-u_1)}{2(au_1+a_0)}\right. \\ & \left.\times\sinh\frac{\pi(L-L_1)}{2(au_1+a_0)}\left[\frac{a(L-L_1)}{au_1+a_0} - \frac{Lg-L+L_1}{u_1}\right]\right\}, \end{aligned}$$

$$\begin{aligned} C_{\rm g32} = & \frac{\pi u_0LZ(1-u_1)}{2m_0V_{\rm P}(au_1+a_0)}\sinh\frac{\pi(L-L_1)}{2(au_1+a_0)} \\ & \times\left[\frac{1-u_0}{\gamma(1-u_1)} - 1\right]\left(1+\frac{a_0}{au_0}\right), \end{aligned}$$

$$\begin{aligned} g = & 1-\frac{L_1}{L} \\ & -Zu_1\left\{\left[\frac{2u_1(1-\gamma)}{\gamma} + \frac{(u_1^2-u_0^2)-\frac{2}{3}(u_1^3-u_0^3)}{\gamma(1-u_1)^2}\right]\right. \\ & \left.-\frac{a_0}{\gamma a}\left[\frac{(u_1^2-u_0^2)-(u_1-u_0)}{(1-u_1)^2} - 2(1-\gamma)\right]\right\}. \end{aligned}$$

So, the cutoff frequency can be obtained by

$$f_{\rm T} = \frac{g_{\rm m}}{2\pi C_{\rm g}}. \tag{11}$$

3. Results and discussion

In our proposed SiC MESFET structure, the gate length is 0.7 μm. Meanwhile, the thickness and doping concentration are 0.26 μm and 1.7×10^{17} cm^{-3} for the channel layer, and 0.15 μm and 1×10^{15} cm^{-3} for the gate-buffer layer between the gate and channel layer.

Figure 2 shows the effect of the gate-buffer layer on the current in the channel. It reveals that the thicker the gate-buffer layer is, the larger the drain current is. This is because the channel width is increased owing to the decrease of the depletion layer thickness in the channel when the gate-buffer layer doping concentration and thickness is increased. It is also shown in Fig. 2 that when the gate-buffer layer is increased sufficiently, the drain currents increase slowly. In fact, when the gate-buffer layer thickness is increased, the thickness of the depleted layer in the channel layer decreases more and more slowly. So, the thickness of the conduction channel and the drain currents increase more and more slowly with increasing the thickness of the gate-buffer layer.

It is one of the most important applications to act as an amplifier for the power microwave 4H-SiC MESFET. If the maximum output drain currents are not large enough, when an alternating-current (AC) large signal is input, the modulation range of the input AC large signal will be limited and thus nonlinear distortion occurs, i.e., cutoff distortion or saturation distortion. Because our proposed structure has larger maximum

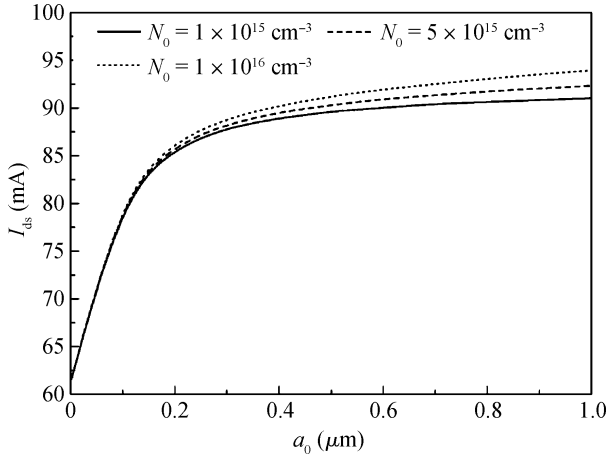

Fig. 2. Dependence of the drain current on the gate-buffer layer for $N_0 = 1 \times 10^{15}$ cm^{-3}, $N_0 = 5 \times 10^{15}$ cm^{-3} and $N_0 = 1 \times 10^{16}$ cm^{-3}. $V_{gs} = 0$ V, $V_{ds} = 5$ V.

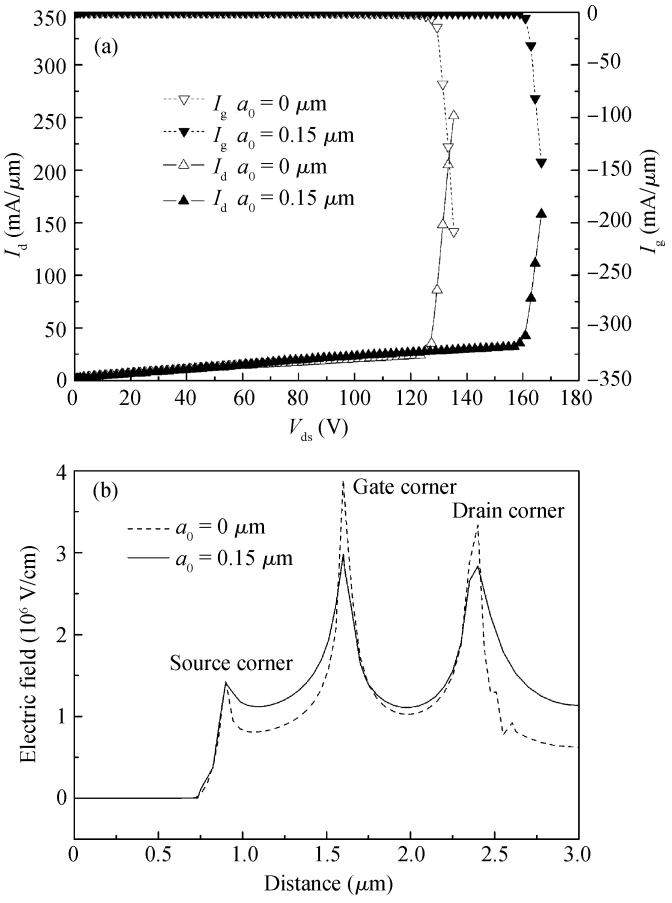

Fig. 3. The simulated breakdown characteristics. (a) Drain current and gate leakage current for $a_0 = 0$ μm (open) and $a_0 = 0.15$ μm (filled). (b) Electric field for $a_0 = 0$ μm (dash) and $a_0 = 0.15$ μm (solid).

output drain currents than that of the conventional structure, it is more applicable for the AC large signal application.

Figure 3 is the simulated breakdown characteristics for the two structures using the ISE simulator[7]. It can be seen that the breakdown voltage (V_b) for $a_0 = 0.15$ μm is 160 V, which is higher than 125 V for $a_0 = 0$ μm. Figure 3(b) plots the corresponding electric field distribution. It shows that the breakdown happened at the gate corner near to the drain side due to the electric field crowding here in both structures. However, the electric field peak is significantly lowered at the gate corner while raised at the drain corner, i.e., the surface electric field is more uniform, owing to the inserted lower doped gate-buffer layer, when compared with that of the conventional SiC MESFET. The reason for the suppression of the electric field at the gate corner is similar to that for the weakened surface electric field caused by the lightly doped drain (LDD) in a MOSFET[8].

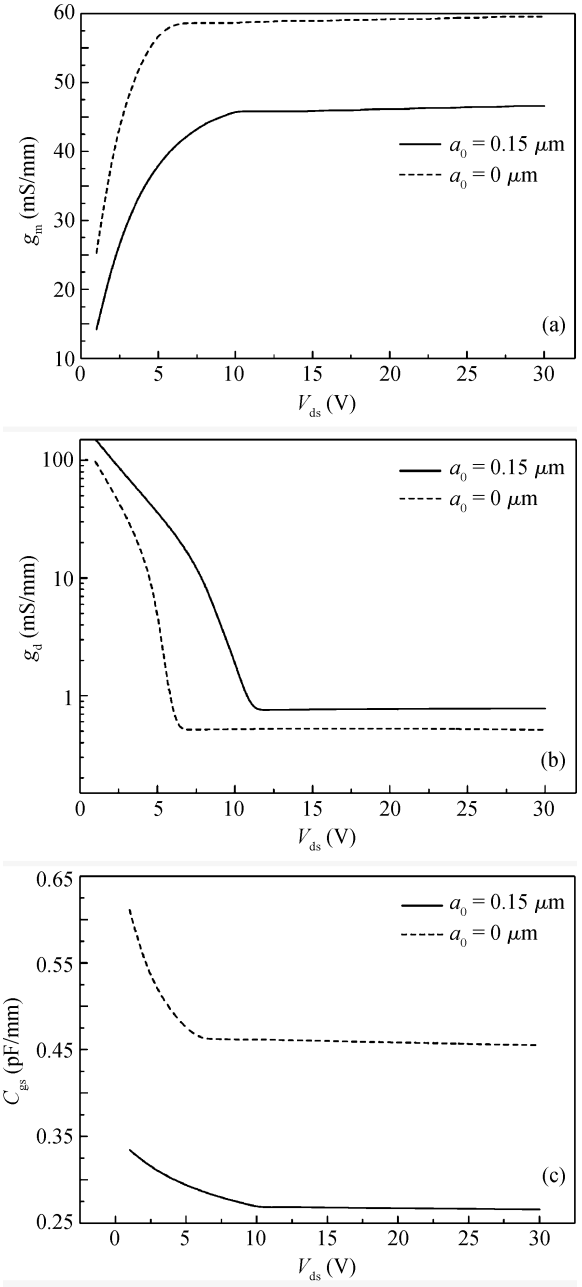

Fig. 4. Transconductance, output conductance, and gate–source capacitance versus drain voltage at $V_{gs} = 0$ V for $a_0 = 0$ μm (dash) and $a_0 = 0.15$ μm (solid).

For simplicity, the gate–source and gate–drain region channel resistances, as well as the depletion region III between the gate and drain are omitted during the calculation of small signal parameters. Figure 4 shows the transconductance, out-

Table 1. The calculated small signal parameters at $V_{gs} = 0$ V and $V_{ds} = 10$ V.

Parameter	g_m (mS/mm)	g_d (mS/mm)	C_{gs} (pF/mm)	f_T (GHz)
$a_0 = 0$ μm	58.58	0.52	0.46	20
$a_0 = 0.15$ μm	45.78	1.92	0.27	27

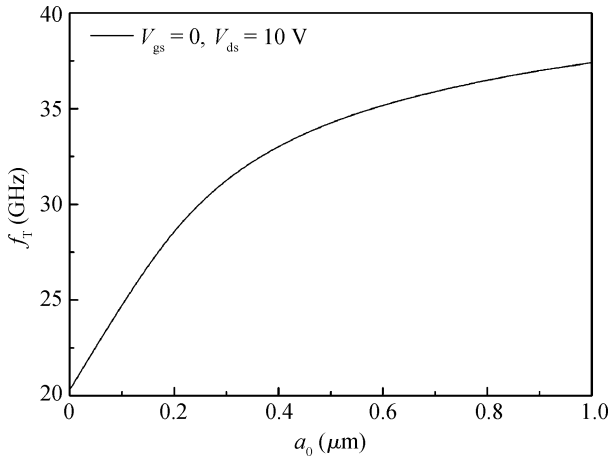

Fig. 5. Variation of the cutoff frequency f_T with the gate-buffer layer thickness a_0.

put conductance, and gate-source capacitance as a function of the drain voltage at $V_{gs} = 0$ V. It can be seen that they are independent of the drain voltage in the saturation region. At the same drain voltage, compared with the conventional structure ($a_0 = 0$ μm), the transconductance (g_m) and gate–source capacitance (C_{gs}) are decreased, while the drain conductance (g_d) is increased because there is a lower doped gate-buffer layer and the total depletion layer thickness under the gate is increased but the part in the channel is decreased. Figure 5 plots the effect of the gate-buffer layer thickness a_0 on the cutoff frequency (f_T). It reveals that the cutoff frequency is increased with increasing the gate-buffer layer thickness. However, when the thickness of the buffer layer is large enough, the cutoff frequency rises more and more slowly. In view of the degradation of the transconductance, the gate–buffer layer thickness should not be too large. Table 1 lists the calculated small signal parameters at $V_{gs} = 0$ V and $V_{ds} = 10$ V. When the gate-buffer layer thickness a_0 is 0.15 μm, the calculated cutoff frequency is 27 GHz, which is higher than 20 GHz for the conventional structure because the gate–source capacitance is more significantly decreased than the transconductance, as can be seen in Table 1.

4. Conclusion

In summary, a lower doped gate-buffer layer is inserted between the gate and the active channel layer and its effects on the direct-current (DC) and AC characteristics of the 4H-SiC MESFET are investigated. The analytical models which describe the dependence of the drain current and small signal parameters on this gate-buffer layer are derived by solving 1-D and 2-D Poisson's equations. The DC and AC parameters of the 4H-SiC MESFET with a buffer-layer thickness of 0.15 μm are calculated or simulated. The results reveal that the drain current, breakdown voltage, and cutoff frequency are all improved when compared with those of the conventional structure due to the lower doped gate-buffer layer. The results achieved in this paper will be helpful for research on power microwave semiconductor devices.

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