Yield Modeling of Rectangular Defect Outline [*]

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Abstract : In integrated circuits ,the defects associated with photolithography are assumed to be in the shape of circular discs in order to perform the estimation of yield and fault analysis. However ,real defects exhibit a great variety of shapes. In this paper ,a novel yield model is presented and the critical area model of short circuit is correspondingly provided. In comparison with the circular model currently available ,the new model takes the similarity shape to an original defect ,the two-dimensional distributional characteristic of defects ,the feature of a layout routing and the character of yield estimation into account. As for the aspect of prediction of yield ,the experimental results show that the new model may predict the yield caused by real defects more accurately than the circular model does. It is significant that the yield is accurately estimated and improved using the proposed model.

Key words : real defect ; rectangular defect model ; critical area ; yield modeling
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1 Introduction

Yield estimate can be used in production control ,material management ,timely product delivery and operations planning tools. It can be used to highlight designs that have much lower than expected yield ,to determine the cost of new devices and their resource implications. It is also the focal point of the industry that evolves from production of standard products , such as the memories of the production of ASIC and SOC products. By the yield prediction ,the measures ,including changing layout shapes ,designing rules and conditions for processes ,are adopted to obtain the maximum yields for mature processes[1,2].

Physical defects have always played an important role in IC yields ,and the design sensitivity to these physical elements has continued to increase in today' s nanometer technologies[3]. Among typical CMOS processes ,it is one of the greatest loss factors of the yield that the defect causes the electrical faults. The modeling of real defect outlines that exhibit a great variety of defect shapes is usually modeled as circular[4~10] , which causes errors of critical area estimation[11~15]. This paper presents a rectangle model of describing real defects and gives emphasis to yield model studying based on the rectangular outlines of real defects. Some experiments are performed to verify the veracity of the new model.

2 Rectangle model of a real defect

For yield model studying ,it is necessary to be-

gin by considering the outline model of real defects. The results in Ref. [13] show that the rectangular model of the real defect has a more accurate estimation on critical areas associated a special layout than that of the circular defect model. The definition of a rectangular model of a defect is given as :for a real defect ,the maximum possible extension of the real defect between two parallel straight lines , which corresponds to a horizontal routing direction of the special layout and touches the defect ,is called the length (represented by the symbol H) of the real defect. The maximum possible extension of the real defect between two parallel straight lines , which corresponds to a vertical routing direction of the special layout and touches the defect ,is called the width (represented by the symbol B) of the real defect , as can be seen in Fig. 1. Then we may define the rectangular model of real defect as a rectangle with H and B.
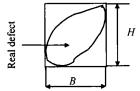

Fig. 1　Rectangular model of real defect

3　New yield model

In general , based on the circular defect outlines ,the Poisson yield model and the negative binomial model are often used to predict the yield loss from defects.

Poisson model

$$Y_F = \prod_{i=1}^{M} e^{-A_i^{(c)} D_i} \qquad (1)$$

Negative binomial model

$$Y_F = \prod_{i=1}^{M} (1 + \frac{D_i A_i^{(c)}}{\alpha_i})^{-\alpha_i} \qquad (2)$$

where Y_F denotes the yield ,which is the product of all layer yields ,and D_i is the defect density for layer i. The Poisson yield has been observed to give pessimistic yield predictions for large devices. In the better negative binomial model , α_i is the cluste-

ring parameter. Both in Poisson yield and in negative binomial model ,$A_i^{(c)}$,the critical area related to a layout for layer i and $A_i^{(c)}$,can be written as

$$A_i^{(c)} = \int_{R_{min}}^{R_{max}} A(R) h(R) dR \qquad (3)$$

where $A(R)$ is the critical area with diameter R, $h(R)$ is the distribution of defect sizes , H_{min} is the minimal diameter ,and R_{max} is the maximal diameter based on the circular model.

According to the above rectangular defect outline model ,the critical area Eq. (3) ,which is caused by a rectangle defect and a layout associated with the i process ,now can be updated by

$$A_i^{(c)} = \int_{H_{min}}^{H_{max}} \int_{B_{min}}^{B_{max}} A(H,B) h(H) b(B) dH dB \qquad (4)$$

where H_{min} is the minimal length of the rectangle defect , H_{max} is the maximal length ,B_{min} is the minimal width of the rectangle defect , and B_{max} the maximal width ,$h(H)$ is the distributed function in length ,that is , $\int_{H_{min}}^{H_{max}} h(H) = 1$, and $b(B)$ is the distributed function in width ,that is , $\int_{B_{min}}^{B_{max}} b(B) = 1$. Related to a defect with length H and width B, $A(H,B)$ is the critical area ,which is determined by the feature of layout routing and the model of a defect.

For mature processes , the distributed functions $h(H)$ and $b(B)$ are fixed and cannot be changed. Therefore ,the key to Eq. (4) is to find $A(H,B)$,which is determined commonly by the feature of layout routing and the defect model. It is well-known that IC interconnect was eventually going to be the dominate contributor to signal performance and that the largest contributor to yield loss is metal to metal shorted lines which can occur when a particle defect falls between two lines. The short critical area that is representative of a group as a whole is as follows.

Now we assume that two metals are deposited on an insulator and have a length L which is much greater than its width W ($L \gg W$). These metals have to allow an electric current to flow from one to the other. The failures in this case are short cir-

cuits caused by extra defects with a length H and a width B. The model of the critical area (see Fig. 2) is expressed as

$$A(H,B) = \begin{cases} 0, & 0 \quad H \quad P \\ (H-P)L + (H-P)B, \\ & P < H \quad W+2P \\ (P+W)L, & H > W+2P \end{cases}$$

(5)

where L, W, and P are the length of metal lines, the width of metal lines, and the spacing between two metals, respectively. Based on the rectangular defect outlines, the new model of yield is composed of Eqs. (1), (4), and (5) or Eqs. (2), (4), and (5).
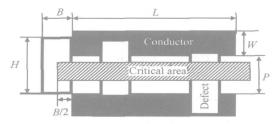

Fig. 2   Short critical area caused by rectangle defect outline

4   Validity of the new model

In order to compare the new model developed in this paper with models currently available, real extra defects were collected using a test chip. The outlines of these defects are obtained by using the segmentation method of color image processing, which was presented in the author's previous paper[13]. Based on these outlines, both the parameters H, B of the rectangular outline and the diameters of the circular outlines are respectively extracted. Using a routing unit similar to Fig. 2 (where the counts of metal lines are 32, that is, there are 32 metals on a routing unit, and $W = 0.3\mu$m, $P = 0.9\mu$m, $L = 56\mu$m), the yields are obtained using the critical area models related to the rectangular outlines and circular outlines. On the same layout and real defects, the yield, as the comparative criterion, is obtained by the Monte-Carlo method. Comparison of the new yield value with the circular

yield values is summarized in Table 1.

Table 1   Yields caused by each defect model and real defect

Defect outline model	Critical area / 10^{-4}cm^2	Fault probability	Yield
Minimal circle	1.6242	0.0151	0.9133
Maximal circle	4.7363	0.0440	0.7677
Real defect	3.7457	0.0348	0.8114
Mean circle	3.3660	0.0313	0.8287
Equivalent circle of ellipse	1.9999	0.0186	0.8944
Rectangle	3.7625	0.0350	0.8106

Table 1 shows that the yields, which are estimated by the model of maximal circle, minimal circle, real outline, mean circle, equivalent circle, and rectangle outline, are 0.9133, 0.7677, 0.8114, 0.8287, 0.894, and 0.8106, respectively. From Table 1, it can be seen that a yield of 0.8106, caused by the rectangular model, is nearest to the true yield of 0.8114 caused by real defect outline.

To verify the new model, another experiments results are given. We assume a $1/x^3$ defect size distribution and a random distribution of defect in length and width. By the features of the real layout (see Fig. 3), we obtain different sizes and different shapes defect with 9, whose maximum circular di-
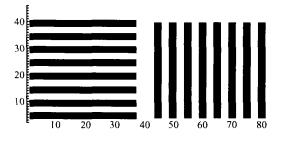

Fig. 3   Metal array layout (line width 2.5μm, line length 36μm, line spacing 2.5μm)

ameters are, 2.5, 3, 4, 5, and 7.9μm, respectively. Correspondingly, each probabilities distribution P_{D1} and P_{D5} are severally 0.11, P_{D2} is 0.22, P_{D3} is 0.33, and P_{D4} is 0.22. For the real defects, minimal circle diameter, mean circle diameter, equivalent circle diameter, rectangle outline and fault probability are calculated, as seen in Table 2. From Table 2, it can be proved that the fault probability 0.2129 caused

by the rectangular model is nearest to the true fault probability 0. 2089 caused by real defect outline. That is ,the yield caused by the rectangular model is nearest to the true yield caused by real defect outline.

Table 2   Fault probability caused by each defect model and real defect

Fault probability	S_{m1} (1)	S_{m2} (2)	S_{m3} (3)	S_{m4} (2)	S_{m5} (1)	Average value with weight
Mean circle	0	0	0.0625	0.3125	1.0	0.2014
Maximal circle	0	0.0625	0.25	0.4375	1.0	0.2986
Minimal circle	0	0	0	0.1667	1.0	0.1482
Equivalent circle	0	0	0	0.2708	1.0	0.1713
Rectangle	0	0.0431	0	0.4098	1.0	0.2129
Real defect	0	0.0418	0	0.3982	1.0	0.2089

5   Conclusion

The rectangular model for predicting IC yield is presented and confirmed by our experiment results. The comparison presented for the routing layout shows that the new model can be used to estimate yield more accurately than the existing yield model. This approach can have a significant impact on the estimation and improvement of IC yields.

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