Simulation of a Monolithic Integrated CMOS Preamplifier for Neural Recordings *

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Abstract: A monolithic integrated CMOS preamplifier is presented for neural recording applications. Two AC-coupled capacitors are used to eliminate the large and random DC offsets existing in the electrode-electrolyte interface. Diode-connected nMOS transistors with a negative voltage between the gate and source are candidates for the large resistors necessary for the preamplifier. A novel analysis is given to determine the noise power spectral density. Simulation results show that the two-stage CMOS preamplifier in a closed-loop capacitive feedback configuration provides an AC in-band gain of 38.8dB, a DC gain of 0, and an input-referred noise of 277nV$_{rms}$ integrated from 0.1Hz to 1kHz. The preamplifier can eliminate the DC offset voltage and has low input-referred noise by novel circuit configuration and theoretical analysis.

Key words: preamplifier; DC offset; input-referred noise
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1 Introduction

There is a growing interest in developing an effective communication interface connecting the human brain with a computer, a brain-computer interface[1~3] (BCI), where a preamplifier is used to sample the brain's neural signals. The design of such a preamplifier is complicated because of the electrode DC offset voltages resulting from the DC polarization of the electrode immersed in electrolyte: DC input voltages up to 100mV should not result in the saturation of the preamplifier[4,5]. In addition, to realize low equivalent input noise, monolithic integration, and small preamplifier dimensions, some characteristics are important to obtain a practical design: no severe demands should be put on resistors, nor should any capacitors larger than 100nF be contained.

Some fully integrated CMOS neural recording preamplifiers[6] use diode-capacitor feedback to filter the electrode DC offset voltages. These preamplifiers are operated in open loop, which makes the gain and output offset voltage difficult to control. Another approach commonly used to filter the electrode DC offset voltages involves loading the recording site with a high-resistance, reverse-biased diode so that this resistor and site capacitor form a high pass filter. The reverse-biased diodes suffer from optical sensitivity problems saturating the outputs of the preamplifiers, and the input-referred noise is on the order of several μV$_{rms}$ integrated from 0.1Hz to 1kHz.

In view of these disadvantages of the present

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preamplifiers, a monolithic integrated CMOS preamplifier is described in this paper. There are no resistors in this circuit, and its capacitors are on the order of pF. As a result, this preamplifier can be realized on a single die chip. The capacitive feedback configuration makes the gain of this preamplifier independent of process variations. Two AC-coupled capacitors are in combination with the large equivalent input resistor to suppress the DC offset of hundreds of mV at the electrode-electrolyte interface, while at the same time forming a high-pass filter.

2 Circuit architecture of the preamplifier

Microelectrodes are implanted in the brain cortex to extract neural signals much accurately. An electrical model of the electrode-electrolyte interface is shown in Fig. 1. V_{in} and V_{ref} represent the input and reference voltage signals of the preamplifier. Usually the reference microelectrode is attached to the electrically stable brain electrolyte, and the input microelectrode is implanted among some neurons in the brain cortex. The components in the dashed box represent the equivalent microelectrode input circuit[7]. The DC voltages V_{dcin} and V_{dcref} represent the DC offsets at the electrode-electrolyte interface. The signal source V_s is the requisite brain neural signal. R_{sp} (spreading resistor in saline) models the signal loss due to the distance between the microelectrode and the cell. C_e models the capacitor of the microelectrode-electrolyte interface. R_e (leakage resistor) accounts for the charge carriers realistically crossing the double-layer. R_1 represents the microelectrode resistor.

The circuit schematic of the preamplifier is shown in Fig. 2. Capacitors C_{in} of 5pF and C_{ref} of 100fF are used to reject the DC offsets V_{dcin} and V_{dcref}, respectively. Capacitors C_1 and C_2 configure the capacitive negative feedback loop. The in-band gain of the closed-loop preamplifier can be described as $1 + C_1/C_2 \approx C_1/C_2$ ($C_1 \gg C_2$, $C_{ref} \ll C_1$).

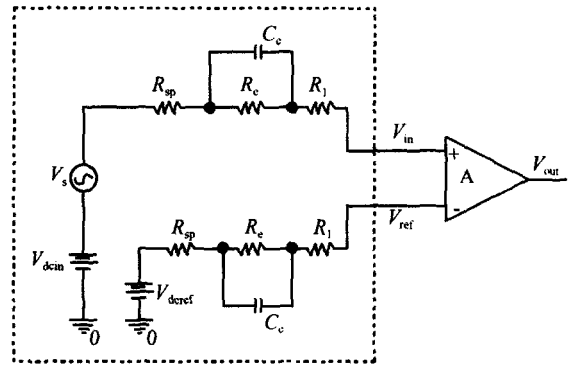

Fig. 1 Electrical model of electrode-electrolyte interface

With C_1 of 10pF and C_2 of 100fF, the AC in-band gain can almost reach 40dB.

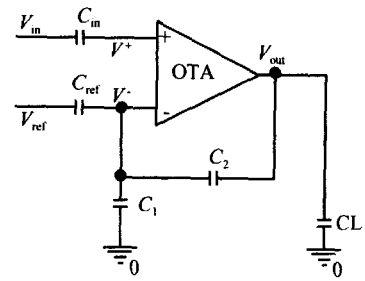

Fig. 2 Circuit schematic of the capacitive-feedback preamplifier

3 OTA design methodology

The preamplifier is composed of an OTA (operational conductance amplifier) and capacitors C_{in}, C_{ref}, C_1, and C_2 as seen in Fig. 2. The transistor-level schematic of this OTA is displayed in Fig. 3. V_{dd} is the power supply source of 5V, while V^- and V^+ are the negative and positive input ports of the OTA. The Miller capacitor C_m and MOS transistor Mm operating in the linear region are for frequency compensation.

As the preamplifier uses a capacitive-coupled input structure and capacitive-feedback configuration, the OTA must have its own DC bias circuit as shown in the left circuit of Fig. 3. Diode-connected transistors M11 and M12 are in tandem to produce a DC voltage. It is clear in Fig. 1 that a large equivalent resistance exists at the electrode-electrolyte

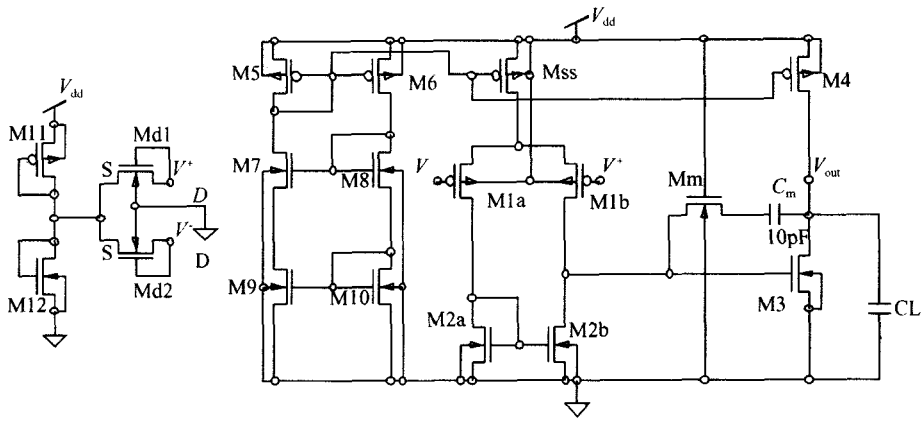

Fig. 3 Transistor-level schematic of the OTA in preamplifier

interface, so a larger equivalent input resistance of the OTA is necessary to obtain the neural signals with a large enough amplitude. In this design, diode-connected transistors Md1 and Md2 with a negative voltage between the gate and source can realize a large resistance of over $10^{11}\,\Omega$ with no effect on the inherent large resistance of the MOS input structure, and DC bias voltages V^+ and V^- are generated at the same time.

Taking into account the weakness of the neural signals of 50～500μV, low noise is an essential requirement of this preamplifier and the OTA. The noise in this OTA comes from flicker noise and thermal noise existing in the MOS transistors[8～11]. Since frequencies of brain cortex neural potentials ranges from less than 1 Hz to several kHz, flicker noise is the primary noise source. The voltage of the flicker noise is shown in Eq. (1).

$$V^2 = \frac{K}{C_{ox}WL} \times \frac{1}{f} \tag{1}$$

where K is a process-dependent constant on the order of $10^{-25}\,V^2 \cdot F$, W and L denote the transistor width and length, C_{ox} is the transistor capacitance density, and f represents the operation frequency. From this equation, it is clear that increasing the product of W and L results in the decrease of noise voltage at the expense of the increased chip area. This causes a serious problem in our application because the input of the system or the equivalent impedance of electrode-electrolyte interface has a high level, and because the active neural probe usually contains multiple recording sites so that one preamplifier is required for each recording site. In this regard, it is very important to minimize the areas of devices at the input stage while meeting the specification of the noise characteristics required for the following system.

Since the input-referred noise of the cascade-stage amplifier is dominated by that of the first amplification stage, the noise characteristics of the input stage in this OTA are emphasized and theoretically analyzed in detail in this paper. The input-stage thermal noise spectral density N_{th} is

$$N_{th} = \frac{16}{3} \times \frac{kT}{g_{M1a}}\left(1 + \frac{g_{M2a}}{g_{M1a}}\right) \tag{2}$$

where $k = 1.38 \times 10^{-23}$ J/K is the Boltzman constant. The flicker noise spectral density $N_{1/f}$ is given by Eq. (3). The total noise power spectral density of the MOS transistors N_{mos} is given by Eq. (4).

$$N_{1/f} = \frac{2}{C_{ox}} \times \frac{1}{f}\left(\frac{K_p}{W_{M1a}L_{M1a}} + \frac{K_n}{W_{M2a}L_{M2a}}\left(\frac{g_{M2a}}{g_{M1a}}\right)^2\right) \tag{3}$$

$$N_{mos} = N_{th} + N_{1/f} = \frac{16}{3} \times \frac{kT}{g_{M1a}}\left(1 + \frac{g_{M2a}}{g_{M1a}}\right) + \frac{2}{C_{ox}} \times \frac{1}{f}\left(\frac{K_p}{W_{M1a}L_{M1a}} + \frac{K_n}{W_{M2a}L_{M2a}}\left(\frac{g_{M2a}}{g_{M1a}}\right)^2\right) \tag{4}$$

According to Eq. (4), increasing the transconductance g_{M1a} and the device area will simultaneously decrease N_{th} and $N_{1/f}$, then N_{mos}. Another interesting phenomenon in this equation is that N_{mos} is basically proportional to the ratio of g_{M2a} and

g_{M1a}. Accordingly, reducing g_{M2a}/g_{M1a} leads to decrease of N_{mos}. Figure 4 plots the curve of the input-referred noise versus g_{M2a}/g_{M1a} with frequency integrated from 0.1Hz to 1kHz. As shown in Fig. 4, the input-referred noise increases with increasing g_{M2a}/g_{M1a}.

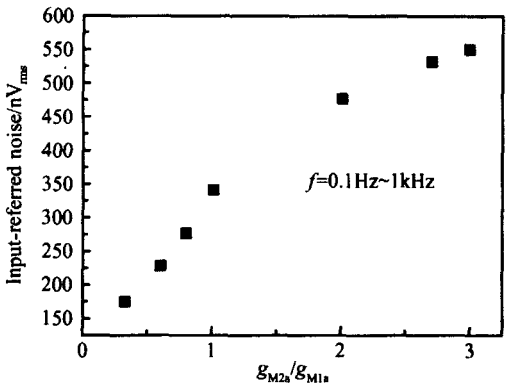

Fig. 4 Input-referred noise versus g_{M2a}/g_{M1a}

Transistor Mm and capacitor C_m compose the lead compensation configuration, and the amplitude and phase of the OTA output as functions of frequency are plotted in Figs. 5 and 6, respectively. From these curves, a satisfied phase margin of 83° is obtained.

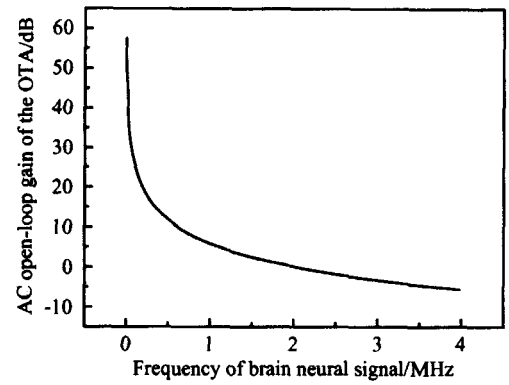

Fig. 5 AC open-loop gain of the OTA versus frequency

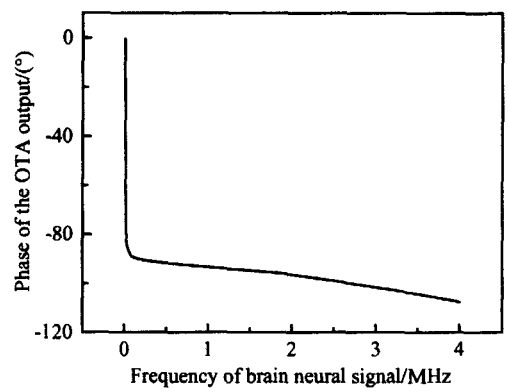

Fig. 6 OTA output phase versus frequency

In accordance with the above description, device parameters of this OTA are determined, and the ultimate device dimensions in this OTA determined by optimization design are listed in Table 1.

Table 1 Device dimensions of MOS transistors

MOS transistor	Mss	M1a	M1b	M2a	M2b	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	Md1	Md2	Mm
W/L (μm/μm)	20/4	300/4	300/4	56/4	56/4	600/4	100/4	20/4	20/4	20/4	20/4	20/4	20/4	4/4	10/4	4/4	4/4	4/4

4 Simulation results of the preamplifier

The whole circuit schematic of the preamplifier is the combination of Figs. 2 and 3. This preamplifier is simulated by the HSPICE simulator with model parameters from CSMC-HJ 0.6μm CMOS double-metal-double-poly process technology, and the capacitors will be fabricated using double poly. With the MOS transistor dimensions listed in Table 1, C_1 of 10pF and C_2 of 100fF, simulation results show that the AC in-band gain of the preamplifier is 38.8dB with frequency from 0.1Hz to 1kHz as shown in Fig. 7. Considering the signal loss due to capacitor C_{in}, the AC in-band gain of 38.8dB is a little smaller than the theoretical value of 40dB.

5 Conclusion

A novel monolithic integrated CMOS preamplifier is presented in this paper. Two AC-coupled capacitors are used to eliminate the DC offset volt-

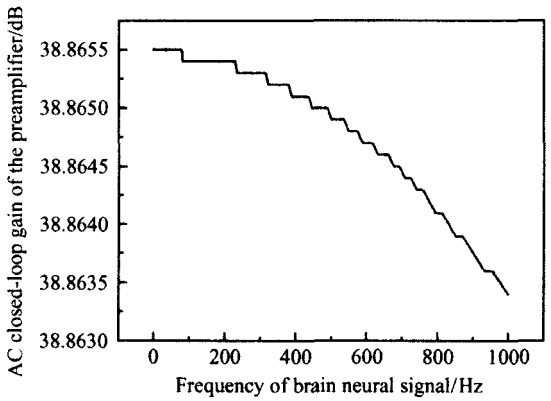

Fig. 7 AC in-band gain of the preamplifier with frequency from 0.1 Hz to 1 kHz

age in the electrode-electrolyte interface. A capacitive negative feedback circuit configuration achieves an adjustable AC in-band gain, and its expression is also provided. A novel analysis is given to determine the noise power spectral density. Theoretical analysis shows that the noise power spectral density of the OTA used in the preamplifier is proportional to g_{M2a}/g_{M1a}, and this theory is verified by simulation results. The simulation results also show that the two-stage CMOS preamplifier in a closed-loop capacitive feedback configuration provides an AC in-band gain of 38.8 dB, a DC gain of 0, and an input-referred noise of 277 nV_{rms} integrated from 0.1 Hz to 1 kHz.

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提取神经电信号的单片集成 CMOS 前置放大器的仿真研究 *

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摘要: 提出一种用于提取神经电信号的新型单片集成 CMOS 前置放大器. 在放大器输入端引入的交流耦合电容可以消除存在于电极-电解液之间的电极极化电压,栅源电压为负值的二极管连接的 nMOS 晶体管能够作为大电阻,并且占用很小芯片面积,可以通过此大电阻为前置放大器提供直流偏置,同时不影响输入阻抗值. 通过对输入级进行理论噪声分析,确定了放大器中的各个器件参数. 仿真结果表明,由于采用电容负反馈结构,此放大器的交流增益为 38. 8dB,无直流增益,在 0. 1Hz～1kHz 频率范围内,总输入等效噪声为 277nV$_{rms}$.

关键词: 前置放大器; 电极极化电压; 等效输入噪声

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隋晓红 女,1980 年出生,博士研究生,研究方向是与脑机接口方面相关的集成电路与系统,主要包括提取神经电信号的微电极制作,以及神经电信号专用的前置放大器设计.

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