Monolithic Integration of InGaP/AlGaAs/InGaAs Enhancement/Depletion-Mode PHEMTs *

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Abstract: The monolithic integration of enhancement- and depletion-mode (E/D-mode) InGaP/AlGaAs/InGaAs pseudomorphic high electron mobility transistors (PHEMTs) with a 1.0μm gate length is presented. Epilayers are grown on SI GaAs substrates using MBE. For this structure, a mobility of 5410cm^2/(V·s) and a sheet density of 1.34×10^{12}cm^{-2} are achieved at room temperature. During the gate fabrication of E/D-mode PHEMTs, a novel two-step technology is applied. The devices with a gate dimension of 1μm×100μm exhibit good DC and RF performances. Threshold voltages of 0.2 and -0.4V, maximum drain current densities of 300 and 340mA/mm, and extrinsic transconductances of 350 and 300mS/mm for E- and D-mode PHEMTs are obtained, respectively. The reverse gate-drain breakdown voltage is -14V for both E- and D-mode. Current-gain cutoff frequencies of 10.3 and 12.4GHz and power-gain cutoff frequencies of 12.8 and 14.7GHz for E- and D-mode are reported, respectively.

Key words: pseudomorphic high electron mobility transistors; enhancement-mode; depletion-mode; threshold voltage; GaAs

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1 Introduction

Due to the excellent performance of PHEMTs at high frequencies and noise figures, they have been widely used in microwave and millimeter-wave systems. Recently, extensive research has focused on PHEMTs with low power consumption and low supply-voltage, which can be achieved with direct-coupled FET logic (DCFL), for which both E- and D-mode devices are required. DCFL is one of the best logic technologies for large-scale (LSI) digital circuit applications because of its advantages over other technologies such as buffer FET logic (BFL) and source-coupled FET logic (SCFL). The advantages of DCFL include low power consumption, high speed, design simplicity (i.e. no voltage level shift), and a single power supply[1,2]. However, the main disadvantage of DCFL is its low noise margin, which is sensitive to threshold voltage variation. Therefore, a good enhancement/depletion (E/D) process for DCFL must precisely control the threshold voltage. In general, this can be achieved by the optimization of processes and the

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improvement of the devices' structure. Technologies for typical E/D-mode PHEMTs with good threshold voltage control have been reported using a two-level gate recess technology[3,4].

In this paper, we present a new monolithic integrated E/D-mode InGaP/AlGaAs/InGaAs PHEMT with a 1.0μm gate length. A novel two-step technology for the gate fabrication of E/D PHEMTs is applied. Results for DC and RF operation of the devices are presented and analyzed.

2 Device structure and technology

Figure 1 shows a cross-section view of the E/D-mode device. The material grown by MBE consists of a semi-insulating GaAs substrate, a 1.5μm AlGaAs/GaAs superlattice, a 50nm undoped $Al_{0.22}Ga_{0.78}As$ buffer layer, a 12nm undoped $In_{0.2}Ga_{0.8}As$ channel layer, a 4nm undoped $Al_{0.22}Ga_{0.78}As$ spacer layer, a planar Si-doped layer with a concentration of $3.5\times10^{12}cm^{-2}$, a 10nm undoped $Al_{0.22}Ga_{0.78}As$ layer, a 20nm undoped $In_{0.5}Ga_{0.5}P$ layer, and a 50nm n^+-GaAs cap layer doped to $5\times10^{18}cm^{-3}$. An electron mobility of $5410cm^2/(V\cdot s)$ and a two-dimensional electron gas (2DEG) density of $1.34\times10^{12}cm^{-2}$ are obtained.

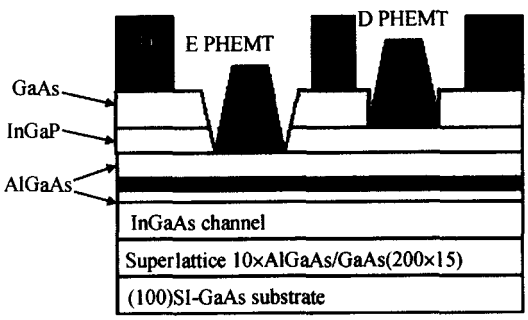

Fig. 1 Cross-section of E/D-mode PHEMTs

In typical E/D-mode PHEMTs, $Al_xGa_{1-x}As$ is often applied as an E/D-mode Schottky-barrier layer[2,3]. However, this has some disadvantages, such as DX centers and low surface potential. In overcoming these shortcomings, InGaP material has received much attention for use in PHEMTs and HBT devices due to its advantages over $Al_xGa_{1-x}As$, which include: (a) the absence of deep levels such as DX centers; (b) no deleterious effects on ohmic contacts or the FET source resistance; (c) a lower surface oxidation rate due to the absence of Al; (d) a lower surface potential (0.18eV versus 0.8eV for AlGaAs); and (e) excellent etching selectivity with respect to GaAs and AlGaAs[5,6]. In this paper, $In_{0.5}Ga_{0.5}P$ is applied as the D-mode Schottky-barrier layer and AlGaAs as the E-mode Schottky-barrier layer. This is favorable for the fabrication of E-mode PHEMTs since it makes it possible to choose gate metals with larger work functions to form the E-mode Schottky gate.

Device fabrication started with simultaneous mesa-isolation for the E- and D-mode devices using a conventional wet etching process. Since $H_3PO_4:H_2O_2:H_2O=3:1:50$ and $HCl:H_2O=1:1$ solutions have a high selection rate for GaAs/InGaP and InGaP/AlGaAs, they were used to etch the GaAs and InGaP, respectively. Using conventional evaporation and lift-off processes followed by rapid thermal annealing, ohmic contacts were formed using a new six-layer ohmic system (Ni/Ge/Au/Ge/Ni/Au). The ohmic contact resistance is typically $2.2\times10^{-7}\Omega\cdot cm^2$ after annealing at 420℃ for 1min in N_2 ambient. Gate metals were sequentially e-beam evaporated. In general, the gate fabrication of E/D-mode PHEMTs uses what is called two-level gate recess technology[2~4]. However, this technology requires complicated processes such as three photolithography alignments. Furthermore the E- and D-mode gates are fabricated with the same gate metals using this process, but it is disadvantageous for the E-mode gate to use metals with larger work functions. Therefore, we present a two-step process for the gate fabrication of E- and D-mode PHEMTs. The two steps are: (1) Apply photolithography to the E-mode gate recess and wet-etch the barrier layers InGaP and AlGaAs in turn; then evaporate the metals to form the E-mode Schottky gate; (2) after lifting off the excess metal of E-mode on the photo-resist, apply photolithography to the D-mode gate recess and wet-etch the

barrier layer InGaP;then evaporate the gate metals to form the D-mode Schottky gate.

It is worth noting that the two-step technology only needs two photolithography alignments to the source and drain. Since the space between the source and drain is relatively large,the process is easy to implement. However,it is difficult for two-level gate recess technology to be photolithography-aligned because the widths of the first and second gate recesses are often rather small.

3　Results and analysis

Drain currents as a function of source-drain voltage for E- and D-mode PHEMTs with a typical 1.0μm gate length are shown in Figs. 2 (a) and (b). Most devices exhibit excellent cut-off and pinch-off characteristics,thus indicating good confinement to the 2DEG in the channel. A maximum saturation drain current (I_{dss}) of 300mA/mm is typically recorded for E-mode PHEMTs at a drain voltage of 1.5V and a gate voltage of 1.5V,whereas for the D-mode PHEMTs,an I_{dss} of 340mA/mm is obtained at a drain voltage of 2.0V and a gate voltage of 1.6V. It is worth noting that the maximum gate-to-source supply voltages for E- and D-mode devices are as large as 1.5 and 1.6V,respectively. It is found that the I_{dss} of D-mode PHEMTs is larger than that of E-mode. This is reasonable since the total carrier density should be smaller in the E-mode PHEMTs.

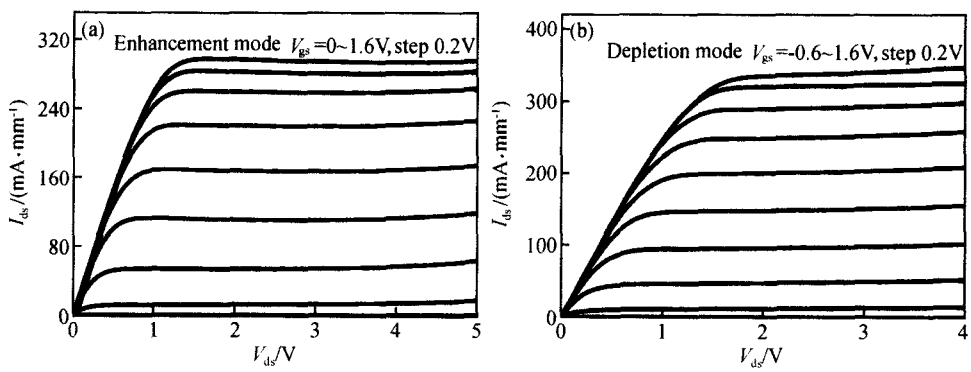

Fig. 2　Drain current characteristics of E-mode PHEMTs (a) and D-mode PHEMTs (b)

Figures 3 (a) and (b) show typical transconductance and output current (I_{ds}) characteristics of E- and D-mode PHEMTs,respectively. For a fixed drain bias of 2.0V,a maximum extrinsic transconductance around 350mS/mm (300mS/mm) at a voltage of about 0.55V (0.15V) and a drain current of about 120mA/mm (135mA/mm) is achieved for E-mode (D-mode) PHEMTs.

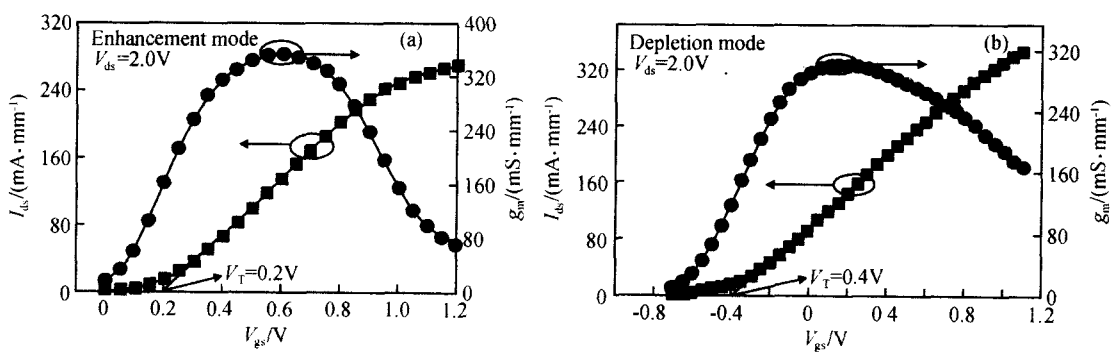

Fig. 3　Transconductance and output current characteristics of E-mode devices (a) and D-mode devices (b)

The threshold voltages of the E- and D-mode devices are 0.2 and -0.4V. Our measurements show that most devices' threshold voltages swing within ±0.1V due to the use of a highly selective InGaP etching layer. Off-state gate-drain breakdown voltages, defined as the reverse gate-drain voltage for a gate-drain current less than 1mA/mm while the source is kept floating, are measured. As illustrated in Figs. 4(a) and (b), the reverse gate-drain breakdown voltage is -14V for both E- and D-mode PHEMTs.

On-wafer RF measurements were carried out using a Cascade Micro-tech HP8510C network analyzer in the frequency range of 1 to 10GHz. *S*-parameters are measured for each device at different biasing conditions, and optimum bias conditions for current-gain cutoff frequency (f_T) and power-gain frequency (f_{max}) are determined and presented in Fig. 5. The voltages for this measurement are V_{gs} = -0.6V and V_{ds} = 2.5V for D-mode PHEMTs and V_{gs} = 0.3V and V_{ds} = 2.5V for E-mode PHEMTs. The measured values of f_T and f_{max} are 10.3/12.8GHz and 12.4/14.7GHz for the E/D-mode devices, respectively. In comparison with the results of similar works[7], all measured devices with a 1.0μm gate length exhibit excellent DC and RF characteristics, probably due to the reduced source resistance achieved by the application of the two-step technology. Unfortunately, this technology leads to a lower drain-gate breakdown voltage than the two-level gate recess technology[7,8].

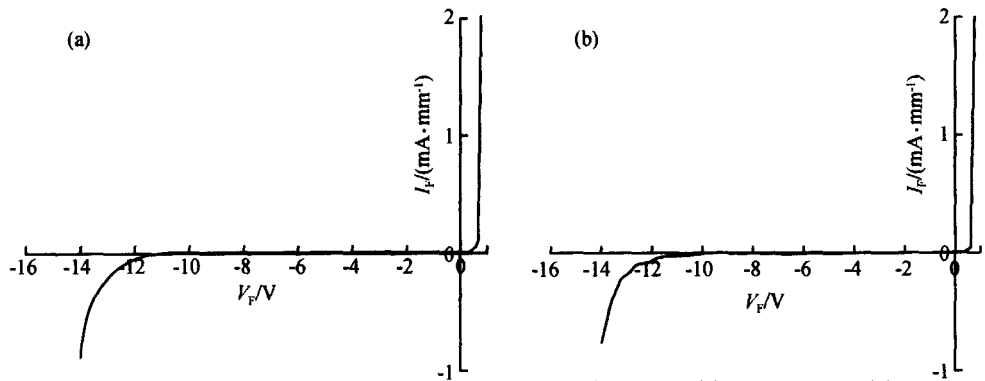

Fig. 4 Reverse gate-drain breakdown voltage characteristics of E-mode (a) and D-mode (b) devices

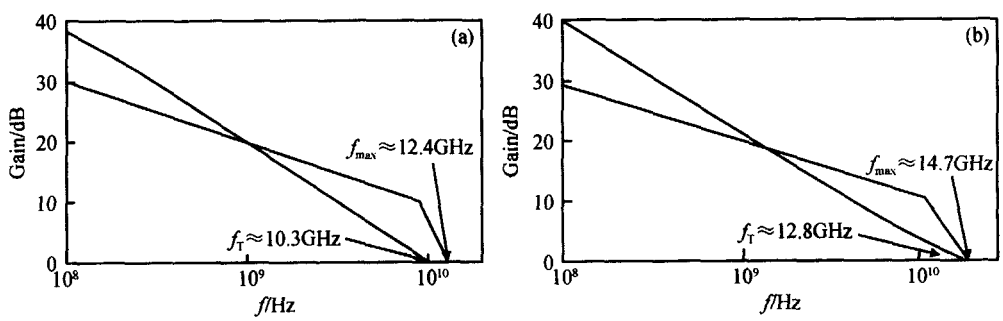

Fig. 5 Measured gains at microwave frequencies of $f_T \approx 10.3$GHz, $f_{max} \approx 12.4$GHz for the E-mode device (a) and $f_T \approx 12.8$GHz, $f_{max} \approx 14.7$GHz for the D-mode device (b)

4 Conclusion

In this paper, the monolithic integration of InGaP/AlGaAs/InGaAs E- and D-mode PHEMTs with a 1.0μm gate length is presented. Excellent DC and RF performances have been achieved with maximum I_{dss}, g_m, f_T, and f_{max} values of 300mA/

mm, 350mS/mm, 10.3GHz, and 12.4GHz, respectively for E-mode devices, and 340mA/mm, 300mS/mm, 12.8GHz, and 14.7GHz, respectively for D-mode devices. The reverse gate-drain breakdown voltage for both E- and D-mode PHEMTs is -14V. Meanwhile, a novel two-step technology for the gate fabrication of E- and D-mode PHEMTs is applied, which yields larger I_{dss}, g_m and higher f_T, f_{max}. However, the process is disadvantageous to the gate-drain breakdown voltage, and further study is currently underway, and further investigation of the applications of DCFL circuits is being conducted.

References

[1] Wantabe Y, Kajll K, Asada Y, et al. A high-speed HEMT 1.5K gate array. IEEE Trans Electron Devices, 1987, ED-34: 1253

[2] Chan Y J, Yang M T. Enhancement and depletion-mode AlGaAs/$In_{0.15}Ga_{0.85}As$ HEMTs fabricated by selective ion implantation. Electron Lett, 1993, 29(25): 2220

[3] Tong M, Nummila K, Seo J W, et al. Process for enhancement/depletion-mode GaAs/InGaAs/AlGaAs pseudomorphic MODFETs using selective wet gate recessing. Electron Lett, 1992, 28(17): 1633

[4] Mahajan A, Fay P, Arafa M, et al. Monolithic integration of InAlAs/InGaAs/InP enhancement-and depletion-mode high electron mobility transistors. IEDM, 1996: 51

[5] Chertouk M, Burkner S, Bachem K, et al. Advantages of Al-free GaInP/InGaAs PHEMTs for power applications. Electron Lett, 1998, 34(6): 590

[6] Geiger D, Mittermeier E, Dickmann J, et al. InGaP/InGaAs HFET with high current density and high cut-off frequencies. Electron Lett, 1995, 16(6): 259

[7] Tsai M K, Tan S W, Wu Y W, et al. Depletion-mode and enhancement-mode InGaP/GaAs-HEMTs for low supply-voltage applications. Semicond Sci Technol, 2002, 17: 156

[8] Dumka D C, Hoke W E, Lemonias P J, et al. High performance 0.35μm gate-length monolithic enhancement/depletion-mode metamorphic $In_{0.52}Al_{0.48}As$/$In_{0.53}Ga_{0.47}As$ HEMTs on GaAs substrate. IEEE Trans Electron Devices, 2001, 22(8): 364

GaAs 基单片集成 InGaP/AlGaAs/InGaAs 增强/耗尽型 PHEMTs *

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摘要: 提出了一种新结构单片集成增强/耗尽型(E/D) InGaP/AlGaAs/InGaAs 赝配高电子迁移率晶体管(PHEMTs). 外延层材料通过分子束外延技术生长, 在室温下, 其电子迁移率和二维电子气浓度分别为 5410cm^2/(V·s)和 1.34×$10^{12}cm^{-2}$. 首次提出了普通光学接触曝光分步制作增强与耗尽型的栅技术方法. 研制出了单片集成 E/D 型 PHEMTs, 获得良好的直流和交流特性, 最大饱和漏电流密度分别为 300 和 340mA/mm, 跨导为 350 和 300mS/mm, 阈值电压为 0.2 和 -0.4V, 增强型的 f_T 和 f_{max} 为 10.3 和 12.4GHz, 耗尽型的 f_T 和 f_{max} 为 12.8 和 14.7GHz. 增强/耗尽型 PHEMTs 的栅漏反向击穿电压都为 -14V.

关键词: 赝配高电子迁移率晶体管; 增强型; 耗尽型; 阈值电压; GaAs

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