A High Breakdown Voltage Thin SOI Device with a Vertically Linearly Graded Concentration Drift Region

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Abstract: As the thickness of an SOI layer varies, a minimum breakdown voltage is reached when the thickness is about 2μm. The vertical electric field of the SOI LDMOS with a drift region which is vertically linearly graded is constant. The vertically linearly graded concentration drift can be achieved by impurity implanting followed by thermal diffusion. In this way, the vertical breakdown voltage of SOI LDMOS with 2μm thickness SOI layer can be improved by 43 %. The on-state resistance is lowered by 24 % because of the higher impurity concentration of the SOI surface.

Key words: SOI; vertically linearly graded concentration; breakdown voltage; LDMOS
EEACC: 2560R
CLC number: TN386 **Document code:** A **Article ID:** 0253-4177(2005)12-2286-04

1 Introduction

Silicon on insulator (SOI) has emerged as a technology for fabricating power integrated circuits (PICs) because the buried oxide (BOX) provides an effective way of isolating the low-power CMOS from the power devices. PICs fabricated in thick-film SOI (>10μm) are complex and expensive because of the difficulty in etching trenches to isolate the devices[1~3]. It has been reported that high performance PICs can be fabricated in thin-film SOI (<2μm) in which the device can be isolated by LOCOS (local oxidation of silicon)[4,5]. In these reports, the vertical breakdown of the device was neglected for the low vertical ionization integration of the thin SOI layer.

In this paper, an analytical model is developed to study the vertical breakdown of LDMOS (lateral double-diffused MOS). According to this model, LDMOS with a drift region in which the concentration is vertically linearly graded is proved to have a maximum vertical breakdown voltage. A novel RESURF SOI LDMOS with a vertically linearly graded concentration drift based on CMOS technology is proposed. Compared to that of traditional LDMOS, the breakdown voltage of the novel device is improved by 43 % and on-state resistance is lowered by 24 %.

2 Analytical model

Figure 1 shows the cross section of the SOI LDMOS. X measures the horizontal position relative to the p-well/n-drift junction, and y measures the vertical position relative to the top surface of the SOI layer. The voltage applied to the p-well and n^+ substrate is 0V. L_d is the lateral distance between the p-well and the n^+ drain contact, while t_s and t_{ox} are the thickness of the SOI layer and the buried oxide, respectively. $N(y)$ is the vertical impurity concentration profile across the SOI layer, assuming that the lateral impurity concentration profile is uniform. The electrostatic potential is denoted as $\psi(x,y)$ and the electric field is $E(x,y) = E_x(x,y)\,i + E_y(x,y)\,j$, where E_x and E_y are the x-component and y-component of the electric field, respectively.

Received 21 May 2005

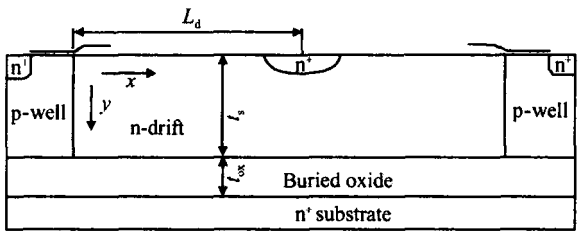

Fig. 1　Coordinate system and important device parameters of RESURF SOI n-LDMOS

The drift region with an impurity concentration that satisfies RESURF technology is depleted completely when a breakdown voltage is applied to the drain. Assuming all the impurities in the depleted region are ionized, Gauss' theorem yields a relation between the impurity concentration and the electric field:

$$N(y) = \frac{\varepsilon_{Si}\varepsilon_0}{q} \nabla \mathrm{E}(x,y) = \frac{\varepsilon_{Si}\varepsilon_0}{q}\left[\frac{\partial}{\partial x}E_x(x,y) + \frac{\partial}{\partial y}E_y(x,y)\right], \quad 0 < x < L_d \text{ and } 0 < y < t_s \qquad (1)$$

where q is the magnitude of electric charge, ε_0 is the permittivity of free space, and ε_{Si} the relative permittivity of silicon.

To achieve the highest vertical avalanche breakdown voltage for a given t_s, the vertical electric field in the depleted region is required to be vertically uniform, i. e. $\partial E_y(x,y)/\partial y = 0$. Also, the lateral electric field along the axis of symmetry ($x = L_d$) in Fig. 2 must be zero, i. e. $E_x(L_d, y) = 0$. As mentioned above, the impurity concentration is assumed to be laterally uniform. With all these conditions, we can get

$$E_x(x,y) = \frac{qN(y)(x - L)}{\varepsilon_0\varepsilon_{Si}}, \quad 0 < x < L_d \text{ and } 0 < y < t_s \qquad (2)$$

Assuming that the potential at the boundary of the p-well and n-drift region is zero, the potential at $x = L_d$ (seen in Fig. 2) is given by

$$\psi(L_d, y) = \frac{qL_d^2}{\varepsilon_{Si}\varepsilon_0}N(y) \qquad (3)$$

Differentiating Eq. (3) yields:

$$\frac{\mathrm{d}N(y)}{\mathrm{d}y} = \frac{\varepsilon_{Si}\varepsilon_0}{qL_d^2} \times \frac{\mathrm{d}\psi(L_d, y)}{\mathrm{d}y} \qquad (4)$$

By hypothesis, the vertical component of the electric field is assumed to be uniform. Therefore, $\mathrm{d}\Psi(L_d, y)/\mathrm{d}y$ = constant. Consequently,

$$\frac{\mathrm{d}N(y)}{\mathrm{d}y} = \text{constant} \qquad (5)$$

Equation (5) reveals that to get an optimal vertical electric field and a maximum vertical breakdown voltage, the impurity concentration of the drift region should be vertically linearly graded.

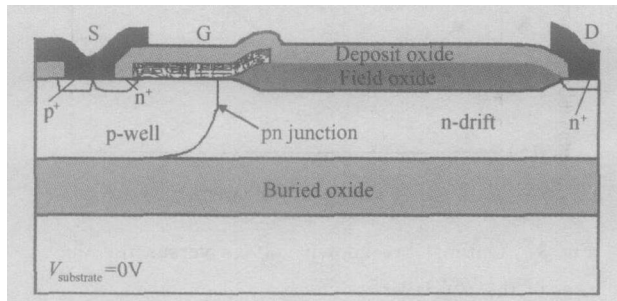

Fig. 2　Cross section of a RESURF SOI n-LDMOS based on a standard CMOS technology created using a Tsuprem-4

3　Numerical simulation

Figure 2 shows the cross section of the RESURF SOI n-LDMOS based on a standard CMOS technology, in which the drift region is the SOI layer. The device is created using a Tsuprem-4. The thickness of the buried oxide film is 2μm. The field oxide film is about 600nm thick. The p-wells are implanted by using boron with doses of 5×10^{12} cm^{-2} and an energy of 160keV, and annealed at 1150 ℃ for 1h. To achieve vertical breakdown before lateral breakdown, a long drift region of length 20μm (from pn junction to n^+ drain) is adopted. The impurity concentration of the SOI layer should be carefully adjusted to satisfy the RESURF technology. As the thickness of the SOI layer increases, the impurity concentration needed to satisfy the RESURF technology decreases (seen in Fig. 4). Medici simulation results show that all the devices break down at the interface of the SOI layer and the buried oxide under the drain, indicating that they break down vertically. Figure 3 shows the breakdown voltage versus the thickness of the SOI

layer. For thin SOI layers (< 2μm) ,the breakdown voltage decreases with the increase of the thickness of the SOI layer. For thick SOI layers (> 2μm) ,the breakdown voltage increases with the increase of the thickness of the SOI layer. The 2μm SOI layer has the lowest breakdown voltage: about 210V.

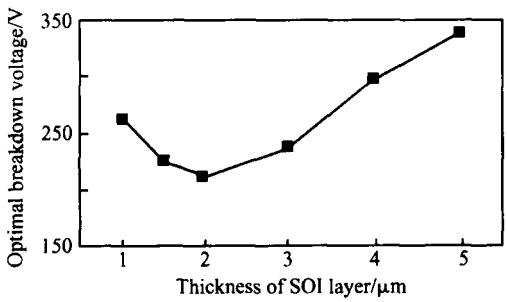

Fig. 3 Optimal breakdown voltage versus the thickness of the SOI layer

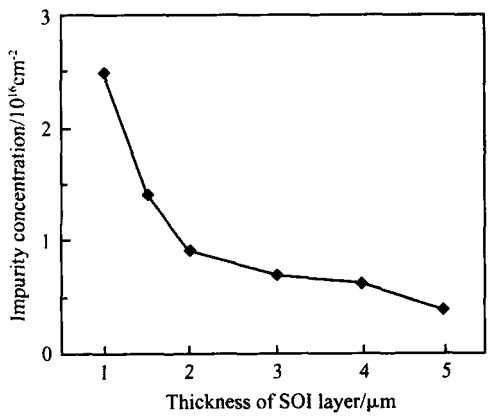

Fig. 4 Impurity concentration of SOI layer satisfying RESURF technology versus the thickness of the SOI layer

To get higher vertical breakdown voltage device in a 2μm SOI layer ,the idea introduced in Sec. 1 was adopted. According to Ref. [5] ,the vertical impurity concentration profile can be treated as a linearly graded one if the surface density is low (< $1 \times 10^{17}\ cm^{-3}$) and the diffused junction is deep. The thickness of the SOI layer of the novel device is 2μm ,and the thickness of the BOX is 2μm. The phosphorus concentration of the SOI layer is $1 \times 10^{15}\ cm^{-3}$. Phosphorus is initially implanted with doses of $2.5 \times 10^{12}\ cm^{-2}$,which are then carefully adjusted to satisfy the RESURF technology. The annealing temperature and time should also be adjusted carefully to achieve a junction depth equal to the thickness of the SOI layer. As can be seen in Fig. 5 ,the vertical impurity concentration profile is nearly linear. The breakdown voltage of the novel device is 297V in the off-state. The phosphorus implanting is implemented at the beginning ,and no additional masks are needed. Therefore ,the novel device achieves a 43 % higher breakdown voltage with no extra cost.

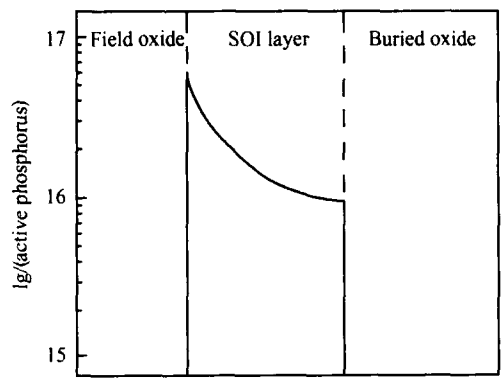

Fig. 5 Vertical phosphorus concentration profile in the drift region

In the on-state ,the vertical component of the electric field is in the positive direction ,compelling the electrons to flow near the interface of the SOI layer and the field oxide. Therefore ,the impurity concentration near the interface is important to the on-state resistance. The novel device has a lower on-state resistance due to its high impurity concentration at the interface of the SOI layer and the field oxide. As shown in Fig. 6 ,the on-state resistance of the novel device is lower than that of a conventional device by 24. 3 %.

4 Conclusion

The vertical electric field of the SOI LDMOS , of which the vertical impurity concentration profile is linear ,is held constant. The vertically linearly graded concentration of the SOI layer can be achieved by impurity implant followed by thermal diffusion. In this way ,the vertical breakdown voltage of SOI LDMOS on the 2μm SOI layer can be

improved by more than 43 %. The on-state resistance is lowered by 24 %.

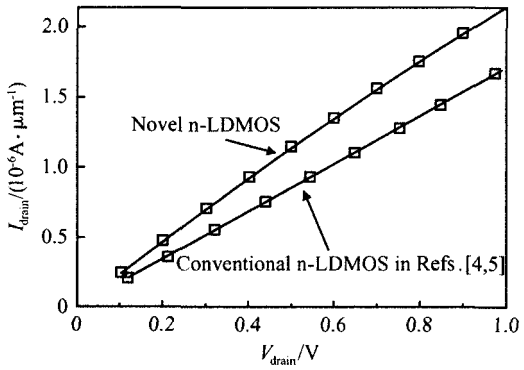

Fig. 6　On-state resistance characteristics of the novel n-LDMOS and the conventional n-LDMOS mentioned in Refs. [4,5]

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漂移区纵向线性掺杂的 SOI 高压器件研究

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摘要：随着 SOI 层厚度的变化，当 SOI 层的厚度为 2μm 时，SOI LDMOS 器件具有一个最佳的击穿电压. 如果漂移区纵向的杂质浓度为线性分布，那么它的纵向电场就会为一个常数，击穿电压会达到最大值，而这种杂质浓度线性分布的漂移区可以通过热扩散得到. 采用这种方法制得的 SOI LDMOS 的纵向击穿电压提高了 43 %，导通电阻降低了 24 %，这是因为它的表面浓度更高.

关键词：SOI；纵向线性浓度分布；击穿电压；LDMOS

EEACC：2560R

中图分类号：TN386　　**文献标识码**：A　　**文章编号**：0253-4177(2005)12-2286-04

2005-05-21 收到