An Analytical Threshold Voltage Model for Fully Depleted SOI MOSFETs

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Abstract: A new two-dimensional (2D) analytical model for the threshold-voltage of fully depleted SOI MOSFETs is derived. The 2D potential distribution functions in the active layer of the devices are obtained through solving the 2D Poisson's equation. The minimum of the potential at the oxide-Si layer interface is used to monitor the threshold voltage of the SOI MOSFETs. This model is verified by its excellent agreement with MEDICI simulation using SOI MOSFETs with different gate lengths, gate oxide thicknesses, silicon film thicknesses, and channel doping concentrations.

Key words: fully depleted SOI MOSFETs; surface potential; threshold voltage
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1 Introduction

Recently there has been an increasing interest in fully depleted SOI MOSFETs[1] because of their inherent immunity to the kink effect[2], nearly ideal sub-threshold voltage swing[3], and immunity to the short channel effect[4]. Many related models have been reported. The 2D Poisson's equations have been solved for both silicon film and buried oxide in Refs. [5,6], and thus the minimum potential has been obtained. The threshold voltage is defined as the gate voltage at which the minimum potential is capable of sustaining the fully depleted channel region. However, the Green function technique is used in solving the Poisson's equations, thereby involving infinite series and increasing the computation complexity. These models are not suitable for circuit simulation. Young's model[7] proposed the parabolic function distribution of potential in the active layer for the first time. Some other models were reported[8~12] using this assumption. Too many fitting parameters and experimental equations were used in Ref. [8], with the result that the model is hard to understand and has lost physical meaning. In Ref. [9] the threshold voltage was defined as the gate voltage at which the minimum of the surface potential equals the Fermi potential of the channel region. This is not consistent with normal conditions and will lead to a lower threshold voltage. In Ref. [10] the 2D Poisson's equation was solved in the active layer to obtain minimum potential distribution. The potential at the front interface between the gate and silicon films was defined as the gate voltage minus the built-in voltage of the Schottky barrier at the gate. This boundary condition is not accurate for SOI MOSFETs. The threshold voltage was defined as the gate voltage for which the minimum of the potential was zero. This is not accurate because at

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threshold voltage the minimum of the potential may be far from zero.

In this paper, an analytical model for fully depleted SOI MOSFETs is proposed. The parabolic function distribution of the potential in the active layer is adopted. The potential distribution at the front surface of the channel is derived. The results of this model closely agree with MEDICI simulation.

2 Theoretical model

2.1 Potential distribution analysis

The schematic structure of a fully depleted SOI MOSFET is shown in Fig. 1. Before the onset of strong inversion, Poisson's equation in the active layer can be written as

$$\frac{d^2\psi(x,y)}{dx^2} + \frac{d^2\psi(x,y)}{dy^2} = \frac{qN_{ch}}{\varepsilon_{Si}}$$
$$0 \leq x \leq T_{Si}, 0 \leq y \leq L \quad (1)$$

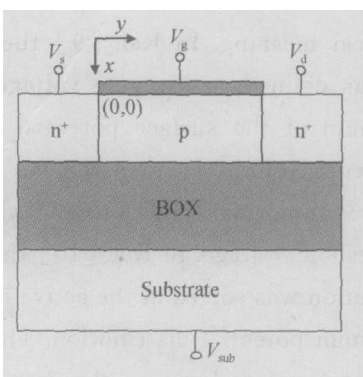

Fig. 1 Cross-section of an n-channel SOI MOSFET

where q is the electron charge and N_{ch} is the doping concentration in the channel region. Because the silicon film thickness is small, the doping concentration in the channel region is assumed to be uniform. Here ε_{Si} is the permittivity of the silicon film, T_{Si} is the thickness of the silicon film, and L is the channel length. When the drain voltage V_d is small, the x-dependence of $\psi(x,y)$ can be approximated by a simple parabolic function:

$$\psi(x,y) = \psi_f(y) + k_1(y)x + k_2(y)x^2 \quad (2)$$

where ψ_f is the potential distribution function at the interface between the gate oxide and silicon film, and $k_1(y)$ and $k_2(y)$ are functions of y independent of x. The functions $k_1(y)$ and $k_2(y)$ can be determined by the following boundary conditions:

$$\psi(T_{Si},y) = \psi_b(y) \quad (3)$$

$$\left.\frac{d\psi(x,y)}{dx}\right|_{x=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \times \frac{\psi_f(y) - V_{gfeff}}{T_{fox}} \quad (4)$$

$$\left.\frac{d\psi(x,y)}{dx}\right|_{x=T_{Si}} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \times \frac{V_{gbeff} - \psi_b(y)}{T_{box}} \quad (5)$$

where $\psi_b(y)$ is the potential distribution function at the bottom interface between the silicon film and buried oxide layer, ε_{ox} is the permittivity of the buried oxide layer, and V_{gfeff} and V_{gbeff} are the effective voltages of the front gate and back gate respectively, which are given by

$$V_{gfeff} = V_g - V_{FBf} \quad (6)$$

$$V_{gbeff} = V_{sub} - V_{FBb} \quad (7)$$

where V_g is the gate voltage, V_{FBf} is the flat-band voltage between the gate and channel, and V_{FBb} is the flat-band voltage between the channel and substrate. V_{FBf} and V_{FBb} are given as

$$V_{FBf} = \frac{kT}{q}\ln\left(\frac{N_g N_{ch}}{n_i^2}\right) + \Delta \quad (8)$$

$$V_{FBb} = \frac{kT}{q}\ln\left(\frac{N_{sub}}{N_{ch}}\right) \quad (9)$$

where k is the Boltzmann constant, T is the absolute temperature, n_i is the intrinsic carrier concentration, N_g is the doping concentration of the polysilicon gate, N_{sub} is the doping concentration of the substrate, and Δ is a fitting parameter.

Equations (3～9) can be used to determine $k_1(y)$ and $k_2(y)$.

$$k_1(y) = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \times \frac{\psi_f(y) - V_{gfeff}}{T_{fox}} \quad (10)$$

$$k_2(y) = \frac{-(1 + C_f/C_{Si} + C_f/C_b)\psi_f(y) + (C_f/C_{Si} + C_f/C_b)V_{gfeff} + V_{gbeff}}{T_{Si}^2(1 + 2C_{Si}/C_b)} \quad (11)$$

Substituting Eq. (2) into (1) yields the differential equations:

$$\frac{d^2\psi(y)}{dy^2} - \alpha\psi(y) = \beta \tag{12}$$

$$\alpha = \frac{2(1 + C_f/C_{Si} + C_f/C_b)}{T_{Si}^2(1 + 2C_{Si}/C_b)\eta} \tag{13}$$

$$\beta = \left(\frac{qN_{ch}}{\varepsilon_{Si}} - 2\frac{(C_f/C_{Si} + C_f/C_b)V_{gfeff} + V_{gbeff}}{T_{Si}^2(1 + 2C_{Si}/C_b)} \right) / \eta \tag{14}$$

where $C_f = \varepsilon_{ox}/T_{fox}$ is the front gate oxide capacitance, $C_{Si} = \varepsilon_{Si}/T_{Si}$ is the silicon film capacitance, $C_b = \varepsilon_{ox}/T_{box}$ is the buried oxide layer capacitance, and η is a fitting parameter. Equation (12) can be solved by using the following boundary conditions: $\psi(0) = \psi_{bi}$, $\psi(L) = V_{ds} + \Phi_{bi}$, where Φ_{bi} is the built-in potential across the body-source junction, and $\Phi_{bi} = kT\ln(N_{ch}N_{ds}/n_i^2)/q$. N_{ds} is the doping concentration of the source and drain. Then $\psi(y)$ can be solved by

$$\psi(y) = -\frac{\beta}{\alpha} + \frac{\phi_{bi} + V_{ds} + \beta/\alpha - (\phi_{bi} + \beta/\alpha)\exp(-\sqrt{\alpha}L)}{2\sinh(\sqrt{\alpha}L)}\exp(-\sqrt{\alpha}(L - y)) + \frac{2(\phi_{bi} + \beta/\alpha)\sinh(\sqrt{\alpha}L) - \phi_{bi} - V_{ds} - \beta/\alpha + (\phi_{bi} + \beta/\alpha)\exp(-\sqrt{\alpha}L)}{2\sinh(\sqrt{\alpha}L)}\exp(-\sqrt{\alpha}y) \tag{15}$$

2.2 Threshold voltage

The position of the minimum front surface potential can be obtained by solving the equation $d\psi(y)/dy = 0$. It is given by

$$y_0 = \frac{L}{2} + \frac{1}{2\sqrt{\alpha}} \times \ln\left(\frac{\phi_{bi} + \beta/\alpha - (\phi_{bi} + V_{ds} + \beta/\alpha)\exp(-\sqrt{\alpha}L)}{\phi_{bi} + V_{ds} + \beta/\alpha - (\phi_{bi} + \beta/\alpha)\exp(-\sqrt{\alpha}L)} \right) \tag{16}$$

Substituting Eq. (16) into (15) can give the value of the minimum front surface potential:

$$\psi_{f,min} = -\frac{\beta}{\alpha} + 2\{[\phi_{bi} + \frac{\beta}{\alpha} - (\phi_{bi} + V_{ds} + \frac{\beta}{\alpha}) \times \exp(-\sqrt{\alpha}L)][\phi_{bi} + V_{ds} + \frac{\beta}{\alpha} - (\phi_{bi} + \frac{\beta}{\alpha}) \times \exp(-\sqrt{\alpha}L)]\}^{1/2} \frac{\exp(-\sqrt{\alpha}L/2)}{1 - \exp(-2\sqrt{\alpha}L)} \tag{17}$$

Figure 2 (a) shows the potential distribution at the front surface between the gate oxide and silicon film. The dashed lines represent the potential distribution at a small drain voltage (0.05V), and the solid lines represent the potential distribution at a large drain voltage (1V). When the drain voltage is large, a small error will be introduced by the 2D effect, which affects the surface potential but not the threshold voltage model because it is based on a small drain voltage.

Compared to devices with long channel length, the devices with short channel length have a higher potential minimum. This reduces the channel barrier. So a short channel device has a smaller threshold voltage. As the drain voltage increases, the potential minimum and the channel barrier are reduced. This effect is called drain-induced barrier

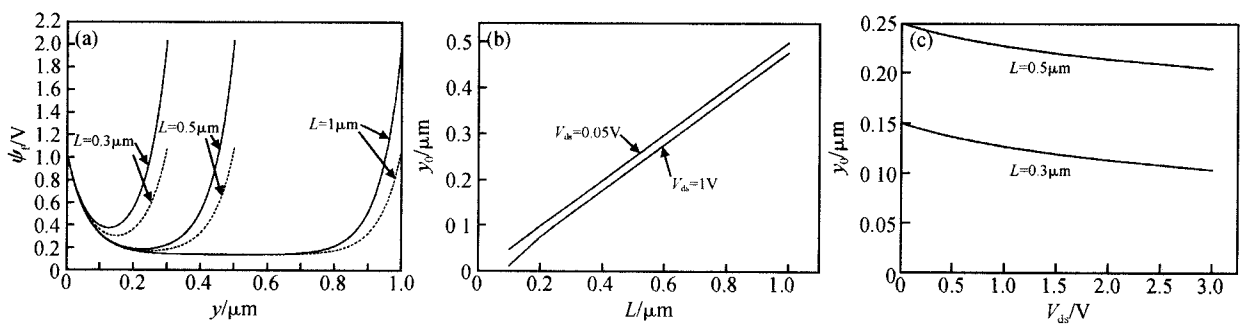

Fig. 2 (a) Calculated front surface potential distribution The device parameters are: T_{fox} = 10nm, T_{Si} = 100nm, T_{box} = 320nm, $N_{ch} = 1.2 \times 10^{17}\,cm^{-3}$. The substrate bias is 0V. The dashed lines show the data for V_{ds} = 0.05V, and the solid lines for V_{ds} = 1V; (b) Calculated location of potential minimum as a function of channel length; (c) Calculated location of potential minimum as a function of drain voltage

lowering (DIBL). DIBL in short channel devices is more evident than in long channel devices as shown in Fig. 2(a).

For long channel devices, $\exp(-(\alpha)^{1/2}L) \ll 1$. When the drain voltage is small, the second term of Eq. (16) is approximately zero, and $y_0 \approx L/2$. That means the potential minimum occurs at the center of the channel for devices with large channel length (see Fig. 2(a)). But this is not true for devices with short channel length because of the short channel effect (SCE). As the drain voltage increases and channel length decreases, the second term of Eq. (16) cannot be omitted. The location of the potential minimum gets closer to the source (see Figs. 2(b) and (c)).

The threshold voltage can be defined quantitatively as the gate voltage where $\psi_{f,\min}$ becomes $2\Phi_b$. Here Φ_b is the Fermi barrier and can be given as

$$\phi_b = \frac{kT}{q}\ln\left(\frac{N_{ch}}{n_i}\right) \tag{18}$$

For devices with a large channel length, the second term of Eq. (17) is approximately zero. The following equations are obtained by substituting $\psi_{f,\min} = 2\Phi_b$ into Eq. (17):

$$\frac{\beta}{\alpha} = -2\phi_b \tag{19}$$

Solving Eq. (19) can give the threshold voltage of devices with large channel length.

$$V_{th0} = \frac{qN_{ch}T_{Si}^2(1 + 2C_{Si}/C_b) - 2\varepsilon_{Si}V_{gbeff} + 4\phi_b\varepsilon_{Si}(1 + C_f/C_{Si} + C_f/C_b)}{2\varepsilon_{Si}(C_f/C_{Si} + C_f/C_b)} + V_{FBf} \tag{20}$$

For devices with small channel length, the second term of Eq. (17) cannot be omitted. The following approximation is used: $\exp(-(\alpha)^{1/2}L) \ll 1$, $1 - \exp(-(\alpha)^{1/2}L) \approx 1$ and the following equations are obtained:

$$a = 1 - 4\exp(-\sqrt{\alpha}L) \tag{21}$$

$$b = 2\psi_{f,\min} - 8\exp(-\sqrt{\alpha}L)\phi_{bi} - 4\exp(-\sqrt{\alpha}L)V_{ds} \tag{22}$$

$$c = 4\psi_{f,\min} - 4(\phi_{bi}^2 + \phi_{bi}V_{ds})\exp(-\sqrt{\alpha}L) \tag{23}$$

$$d = \frac{-b + \sqrt{b^2 - 4ac}}{2a} \tag{24}$$

$$\frac{\beta}{\alpha} = d \tag{25}$$

The threshold voltage can be obtained by solving Eq. (25). Notice that Eq. (25) resembles Eq. (19), except for the right side. Substituting Eq. (21) into (24) and $\psi_{f,\min} = 2\Phi_b$, $\Phi_b = -d/2$ into Eq. (20), the threshold voltage of devices with small channel length can be obtained.

3 Model verification

The threshold voltage versus gate length for different gate oxide thicknesses is plotted in Fig. 3. The threshold voltage decreases with the decrease of gate oxide thickness because the coupling between gate and channel is greater for devices with a thinner gate oxide. And the dependence of the threshold voltage on gate oxide thickness is reduced when the gate oxide is small. Therefore a thin gate oxide is more attractive in practice. But if the gate oxide is too thin, a leakage current may occur because of the tunneling effect. A material with a high permittivity can prevent leakage current while retaining a small equivalent oxide thickness (EOT).

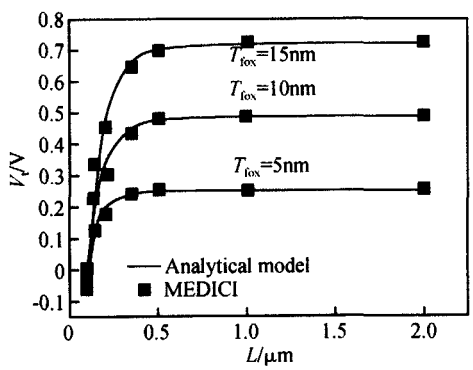

Fig. 3 Threshold voltage versus gate length for different gate oxide thicknesses The device parameters are: $T_{Si} = 100\text{nm}$, $T_{box} = 320\text{nm}$, $N_{ch} = 1.2 \times 10^{17}\text{cm}^{-3}$, $V_{ds} = 0.05\text{V}$.

The threshold voltage versus gate length for different silicon film is plotted in Fig. 4. The

threshold voltage of devices with smaller silicon film thicknesses is lower than that of the devices with larger silicon film thicknesses. This is because there is less charge to be coupled by the gate for the devices with a small silicon film thickness. It also shows that the dependence of threshold voltage on silicon film thickness is small when the devices have a thinner silicon film. It seems that the silicon film should be thin enough. In practice, if the silicon film thickness is less than a critical thickness, tunneling will occur. Compared with the devices that have a thick silicon film, devices with a thin silicon film must have a higher channel doping concentration to fulfill a given threshold voltage requirement.

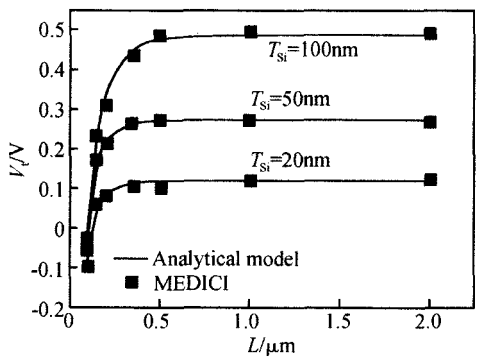

Fig. 4　Threshold voltage versus gate length for different silicon film thicknesses　The devices parameters are: T_{fox} = 10nm, T_{box} = 320nm, N_{ch} = 1.2 ×10^{17} cm^{-3}, V_{ds} = 0.05V.

The threshold voltage versus gate length for different channel doping concentrations is plotted in Fig. 5. It can be seen that the devices with a higher channel doping concentration have a higher threshold voltage, and the dependence of threshold voltage on channel doping concentration is large for these devices. So there must be a tradeoff during the course of device design.

4　Conclusion

In this paper an accurate threshold voltage model for SOI MOSFETs has been proposed. It involves only two fitting parameters. This model has been verified by comparison with simulation results for the devices with different gate oxide thicknesses, silicon film thicknesses, and channel doping concentrations. The simulated data agree closely with the predictions of the model. This model has a simple function form and has no complex mathematical computations such as infinite series. It is easily to be embedded into circuit design software and will play an important role in device and process design.

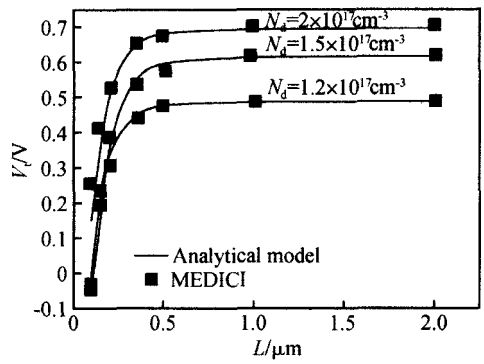

Fig. 5　Threshold voltage versus gate length for different channel doping concentrations　The devices parameters are: T_{fox} = 10nm, T_{box} = 320nm, T_{Si} = 100nm, V_{ds} = 0.05V.

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全耗尽 SOI MOSFETs 阈值电压解析模型

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摘要: 提出了一种新的全耗尽 SOI MOSFETs 阈值电压二维解析模型. 通过求解二维泊松方程得到器件有源层的二维电势分布函数, 氧化层-硅界面处的电势最小值用于监测 SOI MOSFETs 的阈值电压. 通过对不同栅长、栅氧厚度、硅膜厚度和沟道掺杂浓度的 SOI MOSFETs 的 MEDICI 模拟结果的比较, 验证了该模型, 并取得了很好的一致性.

关键词: 全耗尽 SOI MOSFETs; 表面势; 阈值电压

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