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On-State Breakdown Model for High Voltage RESURF LDMOS*

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Abstract: An analytical breakdown model under on-state condition for high voltage RESURF LDMOS is proposed. The model considers the drift velocity saturation of carriers and influence of parasitic bipolar transistor. As a result, electric field profile of n-drift in LDMOS at on-state is obtained. Based on this model, the electric SOA of LDMOS can be determined. The analytical results partially fit to our numerical (by MEDICI) and experiment results. This model is an aid to understand the device physics during on-state accurately and it also directs high voltage LDMOS design.

Key words: LDMOS; safe operating area; breakdown voltage
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1 Introduction

LDMOS is very easy to be integrated into a CMOS or a BiCMOS process which facilitates the fabrication of control, logic circuits and power switches on a single chip. An optimized LDMOS is much more efficient in terms of on-state voltage drops and switching losses compared to power bipolar junction transistor (BJT). Today, the devices are becoming smaller thus require a SOA as wide as possible because these devices are still used in the power application. The tradeoffs between breakdown voltage and on-resistance are well-known features of both lateral and vertical DMOS transistors. But the tradeoffs and restrictions imposed by the "safe operating area" are less familiar. The SOA defines limits on the excursion of the operating point in the I_d-V_{ds} plane. To be corrected, the SOA should also include thermal limitations, however, these can be treated separately[1].

Khemka *et al*. has elucidated the thermal and electrical limitation to the dynamic SOA of large area devices through measurements and transient electrical-thermal simulations[2]. Chung *et al*. has numerically analyzed the mechanism of the electrical-thermal coupling nature in a LDMOS device, and found that activation of the parasitic bipolar component resulted from the diffusion and generation currents lead to the thermally driven snapback breakdown[3]. Based on simulation results, Hower *et al*. found that a high electrical field peak occurs at drift-drain junction, when a large current flows though LDMOS and it produces significant impact ionization at the drain of devices. Generation holes current will lead parasitic bipolar transistor turn on, then it is pointed out that a significant impact ionization appears near the drain with 2D devices simulator[4~6]. Both of the two types analysis have a common viewpoint, but the positions where impact ionization occurs are different. Furthermore, based on analysis results of Hower, Lee *et al*. proposed an optimized structure for improving SOA area, in which body holes current is reduced in order to prevent parasitic bipolar transistor from turning on[7]. Parthasarathy *et al*. used a deep

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drain structure to reduce the electrical field near the drain of devices, then the impact ionization will be reduced and holes current will be decreased, then defer parasitic bipolar transistor turning on[8,9]. Although the LDMOS SOA has been discussed in a number of papers, the details of the device physics which determine the SOA boundary are still somewhat unclear and further work is needed.

In this paper, an on-state breakdown model for high voltage (600V) LDMOS has been proposed for the first time and the electrical SOA, which is defined by a specific boundary line in the I_d-V_{ds} plane, has been discussed.

2 Breakdown models under on-state condition

Figure 1(a) shows a cross-section of n-channel LDMOS with breakdown voltage of 600V. In all n-channel LDMOS transistors, there are parasitic npn transistors that can turn on under a certain condition. This phenomenon happens when a sufficient "base-emitter" voltage develops across the body-source junction. It is due to holes current, where the holes are supplied by the carriers' generation mechanisms at the drain edge due to the impact ionization under the high electrical field.

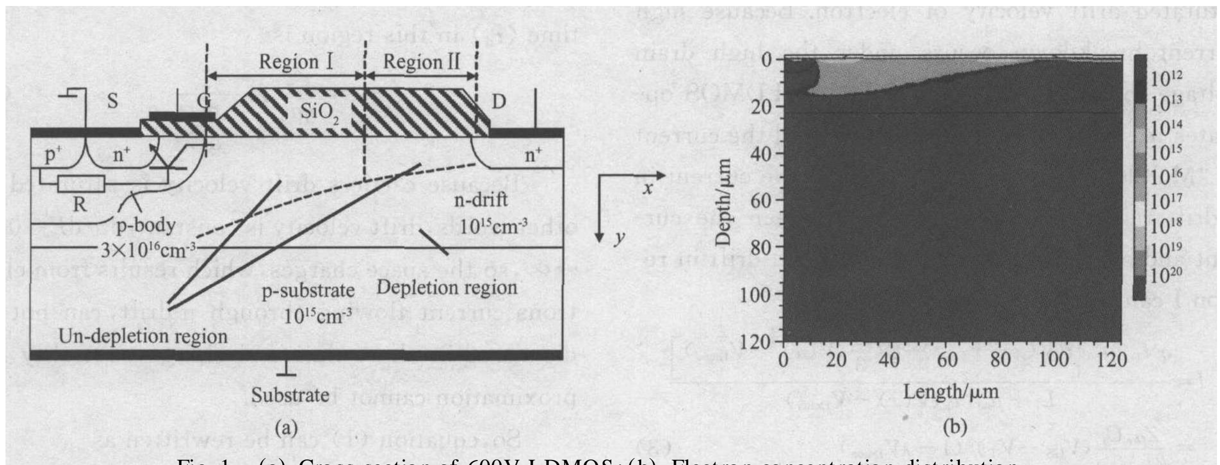

Fig. 1 (a) Cross-section of 600V LDMOS; (b) Electron concentration distribution

When the parasitic npn transistor turns on, the total current through the drift of LDMOS increases. It acts just as positive feedback, then the snap-back behavior appears and the on-state breakdown voltage at high current decreases. Because the high current breakdown is due to impact ionization generation in the drift of LDMOS, electric field profile will be analyzed in detail under the high current condition. The behavior within the n drift region can be explained by considering a rectangular block of n-region with p-type substrate. The electron concentration distribution in the LDMOS has been obtained with 2D devices simulator MEDICI, and the results are shown in Fig. 1(b). So the n-drift region can be divided into two regions: depletion and un-depletion region. Considering electron current and ionized doping in undepletion n-drift region, the surface electric field is met Eq. (1), which is developed from Poisson's and Continuity equations. Holes current and holes profile can be ignored, because they are so insignificant that they can not influence electric field profile in the n-drift.

$$\frac{I}{Zt(x)} = q\mu_n\left(\frac{\varepsilon_{Si}}{q} \times \frac{d^2V}{dx^2} + N_D\right)\left(-\frac{dV}{dx}\right) \qquad (1)$$

where N_D is doping concentration in the n-drift region, V and $n(x)$ respectively are voltage and electrons concentration in undepletion drift region, q is unit electron charge, ε_{Si} is dielectric coefficient of silicon, $t(x)$ is thickness of un-depletion drift region, I is the total drain currents of LDMOS, μ_n is mobility for electron, which is a function of electric field, Z is the width of devices. Equation (1) is a

high order and non-linear differential equation, which is hard to be solved. In order to solve such a differential equation, some approximations must be made. As an approximation, the un-depletion n-drift region can be divided into two regions.

Region I is in n-drift near "n-channel", where electric field is lower and electron drift velocity is unsaturated. Because dielectric relaxation time is smaller than lifetime of carriers in this condition, charge neutrality approximation can be used. The mobility is a function of electric field,

$$\mu_n = \frac{\mu_{n0}}{1 + \mu_{n0}\left(\frac{dV}{dx}\right) / v_s} \quad (2)$$

where μ_{n0} is low field mobility of electron and v_s is saturated drift velocity of electron. Because high current breakdown occurs under the high drain voltage condition, the "MOSFET" in LDMOS operates in saturated consent regime. And the current of "MOSFET" should be equated to the current in n-drift region. The relationship between the current and electrical potential along the n-drift in region I can be written as follows.

$$I = \frac{qN_D Z\mu_{n0}\left[t(V(x) - V_{Dmos}) - \zeta\times\frac{2}{3}(V(x)^{\frac{3}{2}} - V_{Dmos}^{\frac{3}{2}})\right]}{L_I + \mu_{n0}/v_s(V(x) - V_{Dmos})}$$

$$= \frac{Z\mu_n C_i}{2L_{channel}}(V_{GS} - V_T)^2(1 - \lambda V_{Dmos}) \quad (3)$$

where $V(x)$ is voltage along the drift region, V_{Dmos} is "drain" voltage of "MOSFET" within LDMOS, t_0 is the thickness of n-drift region, N_A is the concentration of the p-type substrate, L_I and $L_{channel}$ are the length of low electric field region (region I) and that of "MOSFET" channel respectively. λ is the channel length modulation parameter, because the concentration of p-body is greater than that of n-drift, λ almost equals to 1. ζ is defined as

$$\zeta = \sqrt{\frac{2\varepsilon_{Si} N_A}{qN_D(N_A + N_D)}} \quad (4)$$

From Eq. (3), V_{Dmos} can be obtained. Based on solutions of Poisson's and Continuity equation, in the region I where electron drift velocity is unsaturated, the electrical field can be obtained as

$$|E(x)| = \frac{I}{qN_D Z\mu_{n0}}\left(\zeta V(x)^{1/2} - t + \frac{I}{qN_D Z v_s}\right)^{-1} \quad (5)$$

Based on Eq. (4), we can find that the electric field $|E(x)|$ increases with increasing $V(x)$. Because $V(x)$ is increasing with x, $|E(x)|$ is increasing with x. In region I, the peak electric field with the value of the critical electric field (E_s) for carriers drift velocity saturating, is at the boundary of region I and region II. So the voltage V_I at the boundary of region I and II is given as below.

$$V_I = \frac{qN_D Z\mu_{n0} t/E_s/ - I\left(1 + \frac{\mu_n}{v_s}/E_s/\right)}{qN_D Z\mu_{n0}\zeta/E_s/} \quad (6)$$

Region II is in n-drift near the drain of LDMOS. In this region, carriers drift velocity is saturated and electric field is higher than E_s. Based on space charge relaxation theory, dielectric relaxation time (τ_d) in this region is

$$\tau_d = \frac{\varepsilon_{Si}}{qn_0} \times \frac{1}{\frac{dv}{dE}} \quad (7)$$

Because carriers drift velocity is saturated, in other words, drift velocity is constant, $dv/dE = 0$, $\tau_d \to \infty$, so the space charges, which results from electrons current flowing through n-drift, can not be dismissed in short time and charge neutrality approximation cannot be used.

So, equation (1) can be rewritten as

$$\frac{I}{Zt(x)} = qv_s\left(\frac{\varepsilon_{Si}}{q} \times \frac{d^2V}{dx^2} + N_D\right) \quad (8)$$

From earlier analysis, the electric field and voltage at the boundary of region I and region II is E_s and V_I, and voltage at the drain of LDMOS is V_D. As a solution of the differential equation, the electrical field profile of the region II, where electron drift velocity is saturated, can be obtained as

$$|E(x)| = \left[\frac{4I}{2v_s\varepsilon_{Si}\zeta^2}\left[t\ln\left(\frac{t - \zeta V_I^{1/2}}{t - \zeta V(x)^{1/2}}\right) + \zeta(V(x)^{1/2} - V_I^{1/2})\right] - \frac{2qN_A}{\varepsilon_{Si}}(V_I - V(x)) + E_s\right]^{1/2} \quad (9)$$

Then the breakdown voltage in on-state can be obtained from the above expressions, when the peak electric field in n-drift reaches to a value of critical electric field for avalanche breakdown (E_c).

In all n-channel LDMOS transistors, there are parasitic npn transistors that can turn on under certain conditions. From electrical field of n-drift region during on-state, it is shown that at high V_D impact ionization exists at drain edge. Then electron-hole pairs are generated and the second electrons current flows to the drain, meanwhile, the second holes current flows to the source, which will cause the parasitic npn transistor turning on. Considering the y column of electric field is almost zero at the edge of deplete layer in n-drift, so the generation holes current, which is caused by impact ionization, mainly flows into p-body region while that flowing through p-sub/n-drift can be neglected. The value of second holes current J_{p0} at p-body edge is

$$J_{p0} = J_{n0} \times \frac{\int \alpha \mathrm{d}x}{1 - \int \alpha \mathrm{d}x} \tag{10}$$

where α is coefficient of impact ionization, J_{n0} is electrons current of LDMOS in which impact ionization is not considered. When the voltage drop is larger than forward bias (V_{bi}) of pn junction, the parasitic bipolar transistor turns on. The condition for the parasitic bipolar transistor to turn on is

$$\int \alpha \mathrm{d}x = \frac{V_{bi}}{RJ_{n0} + V_{bi}} \tag{11}$$

where R is parasitic resistance in p-body.

After the parasitic bipolar transistor turns on, the parasitic transistor operates at common emitter amplification status. Considering the parasitic transistor, the current multiplication coefficient M^* of the structure can be rewritten as

$$M^* = \frac{J_{n0} + J_{p0}}{J_{mos}} = \frac{J_{mos} - \beta V_{bi}/R}{J_{mos}} \times \frac{1}{1 - \beta \int \alpha \mathrm{d}x / (1 - \int \alpha \mathrm{d}x)} \times \frac{\int \alpha \mathrm{d}x}{1 - \int \alpha \mathrm{d}x} \tag{12}$$

where β is the current gain of parasitic bipolar transistor. When $M^* \rightarrow \infty$, the LDMOS avalanche breakdown occurs, and the integral of impact ionization is

$$\int \alpha \mathrm{d}x = \frac{1}{\beta + 1} \tag{13}$$

Considering the effects of parasitic bipolar transistor in LDMOS, the integral of impact ionization, which is obtained from Eq. (13), is $1/(\beta + 1)$ times of that not considering parasitic bipolar transistor. In fact, because of the amplification of the parasitic bipolar transistor, the increase of the total current of devices will cause the peak electric field increasing further. Because the impact ionization rate is strongly depended upon electric field, the effective critical electric field (E_c^*) for avalanche breakdown during the parasitic npn transistor turn-on, can be rewritten as

$$E_c^* \approx (\beta + 1)^{-1/7} E_c = \eta E_c \tag{14}$$

where η is defined by reduced fact of critical electric field. Considering the parasitic bipolar transistor in LDMOS, on-state breakdown voltage can be rewritten by replacing E_c by E_c^*.

3　Results and discussion

In order to verify the on-state breakdown model, 600V RESURF LDMOS on 20μm epitaxial layer grown on p-type 〈100〉 silicon wafers had been fabricated and simulated with 2D-device simulator MEDICI. Device structure is shown in Fig. 1. The channel length is 3μm and the length of n-drift is 90μm. Concentration of p-sub, n-drift and p-body are 10^{15}, 10^{15}, and $3 \times 10^{16} \mathrm{cm}^{-3}$ respectively.

Figure 2 shows surface electric field distributions in 600V LDMOS at $V_g = 5\mathrm{V}$. Solid lines without symbols are analytical results and lines with symbols are numerical results by MEDICI. The analytical results are partially fit to our numerical (by MEDICI) and experiment results.

Figure 3 shows the relationship of breakdown voltage and gate voltage V_g, and another experiment results from Ref. [10] also have been shown to compare with our theory analytical results. The results of analysis well fit with simulation results. From Eq. (7), the relationship between the breakdown voltage and the current of devices is square function. The more current flows through LDMOS, the lower on-state breakdown voltage is. Be-

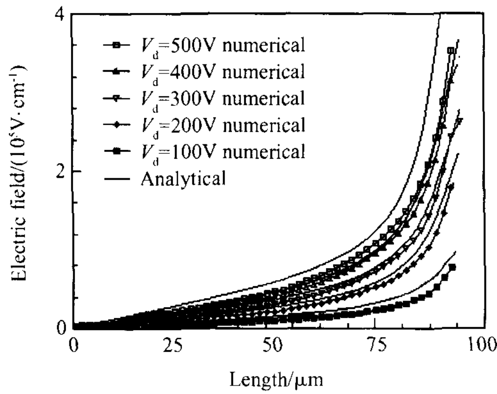

Fig. 2 Surface electric field distributions in 600V LDMOS at $V_g = 5$V Solid lines are analytical results and lines with symbol are numerical results by MEDICI.

cause the current is dependent on gate voltage, on-state breakdown voltage is a function of V_g. In high voltage LDMOS, the concentration of the n-drift is low, so the effect of channel length modulation for MOS can be ignored.

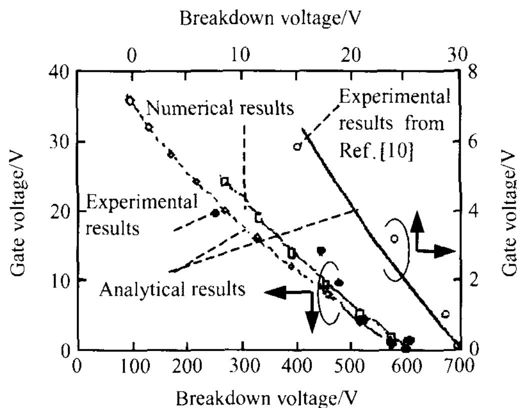

Fig. 3 Simulation, experimental, and analytical results for on-state breakdown voltages as a function of V_g

Usually, the optimization design of RESURF LDMOS is that the lateral breakdown voltage is designed as same as the vertical breakdown voltage. To improve both steady breakdown voltage and on-state breakdown voltage, the value of N_D will be designed a little smaller than that of normal one.

On-state breakdown voltage depends on mobility; it is quite different from forward block voltage. Under the high electric field, the lattice scattering is enhanced; the mobility t of carriers will be reduced. From Eqs. (4) and (8), the reduction of carriers mobility is associated with that of critical electric field for avalanche breakdown, then the on-state breakdown voltage will be decreased by the reducing of carriers mobility under the high electric field.

Another important factor, which influences the on-state breakdown voltage, is current gain β for the parasitic bipolar transistor. The higher β is associated with the lower on-state breakdown voltage. As we know, β depends on the concentration and the junction depth of p-body. To decrease β, it is necessary that the higher concentration and the deeper junction for p-body region should be designed. At the same time, the parasitic resistance in p-body region also influences the parasitic bipolar transistor. Turn-on of the parasitic bipolar transistor will be prevented by increasing concentration of p-body and reducing parasitic resistance R. On the other hand, because the concentration and the depth of p-body region will influence threshold voltage and enhance the effect of channel length modulation, there is a trade-off in devices design. One of the effective methods is constructed a bury layer with high concentration in p-body region to ensure that LDMOS has a certain threshold voltage and also to improve on-state breakdown voltage.

When $\int \alpha \mathrm{d}x \geq \frac{V_{bi}}{RJ_{n0} + V_{bi}}$, the parasitic bipolar transistor will turn on; when $\int \alpha \mathrm{d}x \geq \frac{1}{\beta + 1}$, the avalanche breakdown in LDMOS occurs. Usually, $V_{bi}/(RJ_{n0} + V_{bi})$ is not equal to $1/(\beta + 1)$, and both values of the two expressions are less than 1. So there are two kinds of physical pictures about on-state breakdown of LDMOS. When $V_{bi}/(RJ_{n0} + V_{bi}) < 1/(\beta + 1) < 1$, the parasitic bipolar transistor turns on first and only the current of LDMOS is increasing, but avalanche breakdown does not occur. With the voltage of drain increasing, the electric field reaches to the peak value, avalanche breakdown occurs and snapback phenomenon happens. When $1/(\beta + 1) < V_{bi}/(RJ_{n0} + V_{bi}) < 1$, the ava-

lanche breakdown occurs immediately after the parasitic bipolar turns on. In this case, the snapback phenomenon can not be found. To avoid snapback phenomenon and to improve on-state breakdown voltage, the values of $1/(\beta+1)$ and $V_{bi}/(RJ_{n0}+V_{bi})$ are designed as coequality and high as possible.

4 Conclusions

An analytical breakdown model under on-state condition for RESURF LDMOS has been proposed in this paper. The model considers the drift velocity saturation for carriers and the influence of parasitic bipolar transistor, and electric field profile of n-drift in LDMOS at on-state can be obtained. Based on this model, the electric SOA of LDMOS can be determined. The analytical results are partially fit to our numerical (by MEDICI) and experimental results. Some important factors, which influence the on-state breakdown voltage of LDMOS, such as the concentration of p-body and p-sub, the size and the concentration of drift region, have been discussed. The snapback phenomenon caused by parasitic bipolar transistor has been explained. This model is an aid to understand the device physics during on-state in accuracy and it also directs high voltage LDMOS design.

The fundamental mechanisms that determine LDMOS safe operating area include thermal SOA and electric SOA. Only electric SOA has been partially described in this paper, so some further work is needed.

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高压 RESURF LDMOS 开态击穿模型*

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摘要: 建立了高压 RESURF LDMOS 的开态击穿模型. 该模型考虑了载流子的速度饱和现象和寄生双极性晶体管的影响,获得了开态下 LDMOS 漂移区中的电场分布. 基于该模型可以计算出高压 RESURF LDMOS 的电学 SOA. 数值模拟和实验结果部分验证了模型的正确性. 该模型有助于深入理解 LDMOS 开态击穿的物理过程,可用于指导高压 LDMOS 的设计.

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