

A 2.5Gb/s GaAs MESFET Clock Recovery and Decision Circuit^{*}

ZHAN Yan, XIA Guan-qun, WANG Yong-sheng, ZHAO Jian-long and ZHU Chao-song

(Shanghai Institute of Metallurgy, The Chinese Academy of Sciences, Shanghai 200050, China)

Abstract: A 2.5Gb/s depletion-mode GaAs MESFET clock recovery and decision circuit is described, which applies to the optical fiber communication. The circuit consists of a clock recovery circuit, including a preprocessor, phase detector (PD), low-pass filter (LPF) and voltage controlled oscillator (VCO) and a decision circuit, including a comparator and a latch. The SPICE simulation result confirms the high frequency 2.5GHz of the clock recovery and the high speed 2.5Gb/s of the decision circuit. The 2.5Gb/s decision circuit has proved to be able to deal with the input signal and produce a digital output signal after it being sampled by a clock signal.

Key words: GaAs; MESFET; clock recovery; decision

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1 Introduction

GaAs integrated circuits have some distinct advantages such as high speed, low power dissipation, wide operation temperature and high radiation hardness. And GaAs applies to the optical fiber communication, satellite communication, mobile communication, high speed test systems, etc^[1]. Optical fiber communication, a new communication technique, is promising in acting as the core of B-ISDN (broad integrated services digital network)^[2], due to its broadband, large capacity, far transmitting distance, lightness antijamming and saving energy. The clock recovery and decision circuit plays an important role in the receiver of the communication system, which comprises a clock recovery circuit and a decision circuit. Some overseas papers have been found to report the clock recovery circuit^[3-6] and the decision circuit^[7,8], but not including the clock recovery circuit or the decision circuit, while few domestic papers reported can be

found on the clock recovery circuit and the decision circuit.

We have designed a 2.5Gb/s depletion mode GaAs MESFET clock recovery and decision circuit. Proved by SPICE simulation, the clock recovery circuit can get a 2.5GHz clock signal from the input signal, while the decision circuit can get a 2.5Gb/s digital output signal after it being sampled by a clock signal after low or high level recognition. The test result shows that the decision circuit operates properly at the speed of 2.5Gb/s.

2 Circuit Design and Simulation

The clock recovery and decision circuit is shown in Fig. 1, which consists of a clock recovery circuit and a decision circuit. The former includes a preprocessor, phase detector (PD), low-pass filter (LPF) and voltage controlled oscillator (VCO), while the latter includes a comparator and a latch. The power supply V_{ss} is $-5.2V$. A pair of double frequency signals is produced by using the prepro-

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ZHAN Yan born in 1974, PhD candidate. Her research interests include GaAs devices and circuits.

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cessor after the pair of antiphase input signals, V_{IN1} and V_{IN2} , has been pretreated. By using PD, the phase of the signal is compared with that of the VCO output signals before discrepancy is generated in signals due to the difference between these two phases. The signals having been filtered out of the high-frequency part by the LPF makes the output frequency of the VCO close to that of the pretreated signals. When the two frequencies are same, the phase difference will be stable and the VCO be latchdown, and then a pair of antiphase recovery clock signals, V_{CLK1} and V_{CLK2} are exported. V_{IN} is an input signal (V_{IN1} or V_{IN2}). V_{REF} is the reference voltage. Whether the output of the comparator is low or high can be determined after V_{IN} is compared with V_{REF} . Sampled by recovery clock, the latch can generate the output of the whole circuit V_{O1} and V_{O2} .

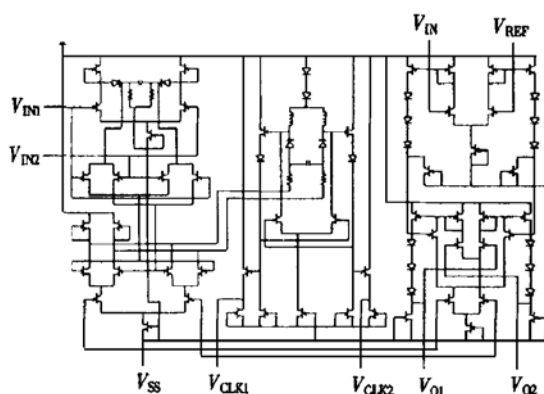


FIG. 1 Schematic Clock Recovery and Decision Circuit

The clock recovery and decision circuit is simulated and optimized by SPICE. The power supply V_{SS} is $-5.2V$. Input V_{IN1} ($-3V$ — $5V$) and V_{IN2} ($-5V$ — $3V$) are a pair of antiphase pulse signals. $2.5GHz$ clock signals can be obtained from the input signals in the clock recovery part. Let V_{IN} of the decision part be V_{IN1} . V_{REF} is $-4V$. When V_{CLK1} is low and V_{CLK2} is high, the latch is locked and V_{O1} and V_{O2} keep the original states. On the contrary, the latch can read the signals from the comparator. If V_{IN} is low, V_{O1} will be low and V_{O2} be high. Figure 2 shows the simulated transient curves

of the clock recovery and decision circuit at the transfer speed of $2.5Gbit/s$.

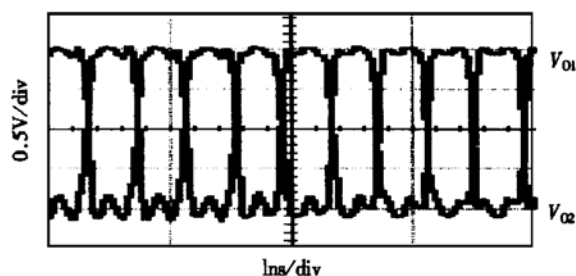


FIG. 2 Simulative Transient Curves of Clock Recovery and Decision Circuit

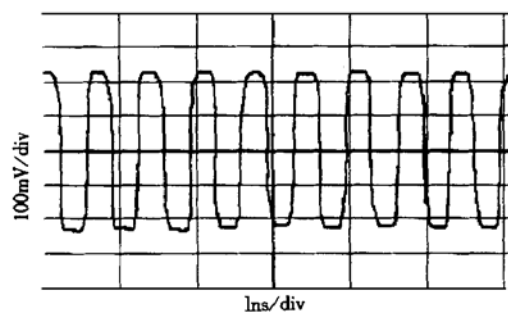
3 Results and Discussion

Because of the restrictive condition, only the decision circuit can be fabricated by using lithography in seven steps. The process flow includes the semi-insulating GaAs substrate subdamage layer etch, direct double Si ion implantation, anneal at $900^{\circ}C$, mark etch, B ion isolation implantation, AuGeNi/Au ohmic metal deposition and anneal at $450^{\circ}C$, Ti/Pt/Au Schottky gate metal deposition, twice Cr/Au routing metal deposition, and polyimide isolation.

The corresponding testing board is also designed and fabricated. The chip pasted on the board with silver conduct-glue is connected with the board by aurum filament in the testing box. Tested with HP oscillograph, the decision circuit shows the ability to deal with the input signal and produce the digital output signal when it has been sampled by a clock signal. The transfer speed of the circuit is $2.5Gbit/s$. The circuit exports a pair of antiphase signals. Figure 3 shows one of the outputs V_{O1} waveforms in the test.

4 Conclusion

The clock recovery and decision circuit designed is confirmed by the SPICE simulation result. The clock recovery circuit can get a $2.5GHz$ clock signal from the input signal while the decision circuit can get a $2.5Gb/s$ digital output signal

FIG. 3 V_{O1} Waveforms Tested

sampled by clock signal after low or high level recognition. The test result shows that the decision circuit operates properly at the speed of 2.5Gb/s.

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2. 5Gb/s GaAs MESFET 定时判决电路*

詹 琰 夏冠群 王永生 赵建龙 朱朝嵩

(中国科学院上海冶金研究所, 上海 200050)

摘要: 设计了 2.5Gb/s 光纤通信耗尽型 GaAs MESFET 定时判决电路. 通过 SPICE 模拟表明恢复的时钟频率达 2.5GHz, 判决电路传输速率达 2.5Gb/s. 实验证明经时钟信号抽样后判决电路可产生正确的数字信号, 传输速率达 2.5Gb/s.

关键词: GaAs; MESFET; 时钟恢复; 判决

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詹 琰 1974 年出生, 博士研究生, 从事 GaAs 器件与电路研究.

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