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Unified MOSFET Short Channel Factor Using Variational Method*

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Abstract: A new natural gate length scale for MOSFET's is presented using Variational Method. Comparison of the short channel effects is conducted for the uniform channel doping bulk MOSFET, intrinsic channel doping bulk MOSFET, SOI MOSFET and double gated MOSFET. And the results are verified by the 2D numerical simulation. Taken all the 2-D effects on front gate dielectric, back gate dielectric and silicon film into account, the data validity of electrical equivalent oxide thickness is investigated by this model, as shows that it is valid only when the gate dielectric constant is relatively small.

Key words: Poisson's equation; variational method; deep submicron; MOSFET; short channel effect

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1 Introduction

It is well known that short channel effect is one of the most important constraints that determine the down scaling of MOSFET's. The relationship between the device structure configuration and short channel effect is first expressed empirically in Ref. [1]. And recently, due to its simplicity and physical insight, parabolic potential[2] and BOX[3] method are widely used[4—7] to analyze the short channel effect in the Deep Submicron MOSFET's. But they all neglect the two dimensional effects in the front and back gate dielectrics, which may be significant in thick high-permittivity insulators[8]. Another drawback in their deductions is that the source/drain boundary conditions are not fully satisfied[9].

In the following section, a unified analytical model is established to simulate the short

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channel effect in bulk and SOI MOSFET's using variational method first introduced in Ref. [10]. According to the method we applied, SOI and bulk MOSFET can be treated in the same analytical framework even when we considering the 2-D effect in the front and back gate (for SOI devices) dielectrics. So it is very suitable to do comparative study of 2-D effect in different MOS technologies, which is done in section 3. And the result is verified by 2-D numerical simulations. In section 4, the validity of electrical equivalent oxide thickness approximation is investigated with this model. The results show it lacks predictive accuracy when the gate dielectric constant is too large.

2 Derivation

The distinct feature of solving the Poisson's Equation with the Variation Method is the ability to deal with the discontinuity of the dielectric constant at different material interface in the solution domain. Unlike the multi-zone approach[11], we can consider the region constituted by different materials as one domain and solve it directly. For purpose of this derivation, the two-dimensional area for the potential analysis is approximated, as shown in Fig. 1, which includes front gate dielectric, fully depleted silicon film and back gate dielectric. For bulk and partial depleted SOI MOSFET, the silicon film and back gate dielectric parts are reduced to the channel depletion layer.

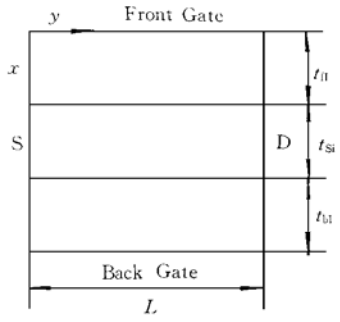

FIG. 1 Two Dimensional Area of a SOI MOSFET for Short Channel Effect Analysis

Using superposition, the potential distribution in this area can be written as

$$\phi(x,y) = \phi_0(x) + \Delta\phi(x,y)$$

where $\phi_0(x)$ is the 1-D, i.e., long-channel solution to Poisson's Equation satisfying the top and bottom boundary conditions; and $\Delta\phi(x,y)$ is the solution to Laplace's Equation, which accommodates the potential applied to the source and drain. Because $\Delta\phi(x,y)$ satisfies the Laplace's Equation, it must minimize the functional[12]

$$J[\Delta\phi(x,y)] = \frac{1}{2}\int_0^{\infty} dy \int_0^{d} \epsilon(x)\left[\left(\frac{\partial\Delta\phi(x,y)}{\partial x}\right)^2 + \left(\frac{\partial\Delta\phi(x,y)}{\partial y}\right)^2\right] dx \qquad (1)$$

where d is the sum of front gate dielectric thickness t_{fi}, silicon film thickness t_{Si} and the back gate dielectric thickness t_{bi} ($d = t_{fi} + t_{Si} + t_{bi}$), and $\epsilon(x)$ is the permittivity function, which is defined as

$$\epsilon(x) = \begin{cases} \epsilon_i & \text{when } 0 \leqslant x < t_{fi} \\ \epsilon_{Si} & t_{fi} \leqslant x < t_{fi} + t_{Si} \\ \epsilon_i & t_{fi} + t_{Si} \leqslant x < d \end{cases}$$

where ϵ_i is the front and back gate dielectric permittivity and ϵ_{Si} is the silicon film dielectric permittivity. Though DIBL effect can be included in our deduction, for simplicity we

neglect the applied drain voltage. So the source and drain boundary conditions are the same. And we can meet the source/drain boundary condition simultaneously if we assume[10]

$$\Delta\Phi(x,y) = \Delta\Phi(x,0)f(y) \tag{2}$$

and

$$f(0) = f(L) = 1$$

where

$$\Delta\Phi(x,0) = \Phi_{S/D}(x) - \Phi_0(x)$$

is the difference between the source/drain boundary condition $\Phi_{S/D}(x)$ and 1-D solution $\Phi_0(x)$. Substitute (2) into (1) and minimize it using Euler's condition[12], we get $f(y)$ which satisfies following ordinary differential equation

$$l^2 \frac{d^2 f(y)}{dx^2} - f(y) = 0 \tag{3}$$

where

$$l = \left[\frac{\int_0^d \epsilon(x)\,\Delta\Phi_S(x,0)\,dx}{\int_0^d \epsilon(x)\left[\frac{d\Delta\Phi_S(x,0)}{dx}\right]^2 dx} \right]^{1/2} \tag{4}$$

(4) is the unified short channel factor for bulk and SOI MOSFET. From (3), we know l has the same physical meaning as the length scale used previously in Ref. [4, 5], i.e., the 2-D effect is small when l is small.

3 2-D Effect Comparison in Different MOS Structures

Due to its general validity, (4) can serve as a vehicle for different device structure to have a 2-D effect comparison. To get the value of l, only the source/drain boundary condition and 1-D solution are needed. So before further detailed numerical simulation we can get a concept of 2-D effect in new device structure, which is important in device design.

For an example, we compare the 2-D effect in the uniform doped-channel bulk MOSFET, intrinsic channel bulk MOSFET, SOI MOSFET and double-gated SOI MOSFET. Their schematic plot of 1-D solutions and source/drain boundary conditions are shown in Fig. 2. The boundary conditions at the dielectric edges are assumed to be linear [11] in this plot. To conduct a fair comparison, the thin silicon film of (c) is as thick as the depletion layer thickness of (a), (b). Due to the symmetry of the structure, two kinds of silicon film thickness for (d) are applied in this study, one (DSOI1) equals that of (c), and the other (DSOI2) is twice that of (c). The uniform channel doping concentration for (a) equals $1\times10^{17}\text{cm}^{-3}$, which determines the depletion layer thickness of (a) and (b) to be 0.10322μm. The other device parameters are as follows: front gate oxide thickness 10nm, buried oxide thickness for SOI 200nm, the thin film doping concentration for SOI and double gated MOSFET being $6\times10^{16}\text{cm}^{-3}$. The difference between the source/drain

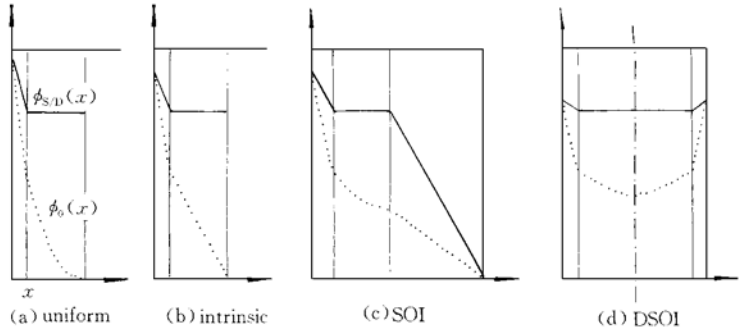

FIG. 2 Schematic Plot of 1-D Solutions and Source/Drain Boundary Conditions for (a) Uniform Channel Doping Bulk MOSFET, (b) Intrinsic Channel Doping Bulk MOSFET, (c) SOI MOSFET and (d) Double-Gated SOI MOSFET.

boundary condition and 1-D solution at the front gate/channel interface is about 0.2V (our calculation shows l is not sensitive to the gate bias). The calculated result of l is shown in Table 1. Also shown in this table is the result using the model in Ref. [4].

Table 1 Calculated Result of l for Different Device Structures (unit: m)

Device Structure	DSOI1	DSOI2	Intrinsic	Uniform	SOI
Calculated l using our model	0.048	0.084	0.075	0.080	0.089
Calculated l using [4]'s model	0.039	0.056	0.035	0.035	0.056

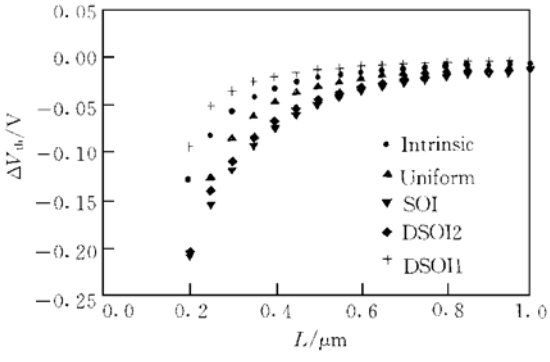

FIG. 3 Threshold Voltage Roll-Off for Different Device Structures

The discrepancy between the two model's results is apparent. Our model determines $l_{DSOI1} < l_{intrinsic} < l_{uniform} < l_{DSOI2} < l_{SOI}$, while Ref. [4]'s model determines $l_{intrinsic} = l_{uniform} < l_{DSOI1} < l_{DSOI2} = l_{SOI}$. To check the real situation, 2-D numerical simulation for these device structures is carried out using MEDICI[13] with the result shown in Fig. 3, where $\Delta V_{th} = V_{th}(L) - V_{th}(3\mu m)$. Threshold voltage V_{th} is defined as the gate voltage at drain current $I_{ds} = W/L \times 0.1\mu A$ with V_{ds} being 0.05V. This figure agrees with our model's result very well.

4 Investigation of Electrical Equivalent Oxide Thickness Approximation

In order to further increase the current driven ability and overcome the short channel effect in the ultra-short channel devices, sub-2nm gate oxide is applied in recent research.

But the ultra-thin gate oxide also introduces the unacceptable high tunneling gate current. To solve the problem, relative thick high- permittivity dielectric is suggested acting as an alternative to the gate oxide. This approach is motivated by the electrical equivalent oxide thickness concept, i. e., if the ratios of gate dielectric thickness to permittivity are the same, the device characteristics should be the same. Obviously, this conclusion reglects the 2-D effects in the gate dielectric and their action in thick high-permittivity dielectric is questionable. To demonstrate this point, we apply (4) to the different gate dielectric double-gated MOSFET short channel effect analysis. If the 1-D solution in the double-gated MOSFET silicon film is approximated as a constant (as is the real situation if the silicon film is intrinsic), (4) can be simplified as further

$$l = \left[\frac{1}{3} \left(\frac{\epsilon_I t_{ox}^{eq}}{\epsilon_{ox}} \right)^2 + \frac{\epsilon_{Si}}{2\epsilon_{ox}} t_{Si} t_{ox}^{eq} \right]^{1/2} \tag{5}$$

where ϵ_{ox} is the gate dielectric permittivity, $t_{ox}^{eq} \equiv t_I \epsilon_{ox}/\epsilon_I$ is the electrical equivalent oxide thickness, where t_I is the front and back gate dielectric thickness. Figure 4 shows the dependence of the scale length l on the gate dielectric constant ϵ_I/ϵ_0 for several values of t_{Si} and t_{ox}^{eq}, where ϵ_0 is the permittivity of the free space. This plot suggests that the equivalent oxide thickness approximation only be valid at a relative small dielectric constant (approximately < 10), and the effectiveness of applying high-permittivity dielectric as gate material would degrade out of this range. The numerical simulation result further confirms our conclusion, which is shown in Fig. 5. The uniform distribution of these points confirms our model can model the 2-D effect in the gate dielectric for a wide range of ϵ_I.

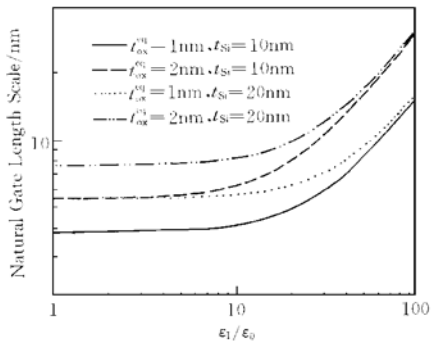

FIG. 4　Plot of Natural Gate Length Scale Versus Dielectric Constant for Some Different Values of Equivalent Oxide Thickness t_{ox}^{eq} and Silicon Film Thickness t_{Si}

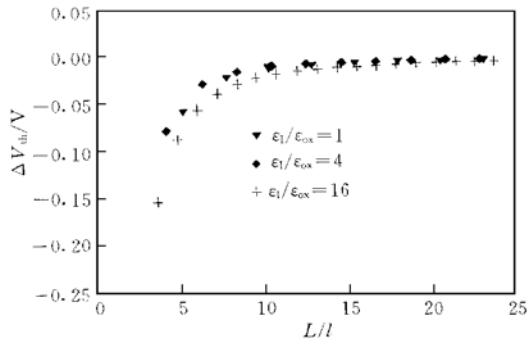

FIG. 5　2-D Simulation Result of ΔV_{th} Versus L/l for Different ϵ_I
The silicon film doping concentration is 6×10^{16}cm^{-3} and t_{ox}^{eq}= 2nm, t_{Si}= 20nm.

5 Conclusion

In conclusion, we present a simple unified scaling theory in this paper, which applies to different device structures. Compared to other quasi-2-D methods, our approach also includes the 2-D effects in the front and back gate dielectrics. 2-D effect comparisons between different device structures and different gate dielectric constant are conducted in this work, and all the model predictions are confirmed by 2-D numerical simulations.

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