第 21 卷第 6 期　　半 导 体 学 报　　Vol. 21, No. 6
2000 年 6 月　　CHINESE JOURNAL OF SEMICONDUCTORS　　June, 2000

A Novel Depletion-Mode MOS Gated Emitter Shorted Thyristor

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Abstract: A Novel MOS-gated thyristor, depletion-mode MOS gated emitter shorted thyristor (DMST), and its two structures are proposed. In DMST, the channel of depletion-mode MOS makes the thyristor emitter-based junction inherently short. The operation of the device is controlled by the interruption and recovery of the depletion-mode MOS P channel. The perfect properties have been demonstrated by 2-D numerical simulations and the tests on the fabricated chips.

Key words: thyristor; MOS gate
EEACC: 2560; 2560L; 2560R
CLC number: TN134; TN323^{+}.4　**Document code**: A　**Article ID**: 0253-4177(2000)06-0536-06

1 Introduction

More attention has been given to the MOS-gated thyristor and several device structures of MOS-gated thyristor have been reported, such as MOS-controlled thyristor (MCT)[1], depletion-mode thyristor (DMT)[2], field assisted turn-off thyristor (FATO)[3], emitter switched thyristor (EST)[4], base-resistance-controlled thyristor (BRT)[5] and base coupled insulated gate thyristor (BC-IGTH)[6], etc. They operate the same trigger mechanism on thyristor having some differences in structures and operation when driving the device turn-off. However, the turn-off of devices above is basically controlled by the enhancement-mode MOS.

Two new structures of the depletion-mode MOS-gated emitter shorted thyristor (DMST), are reported in this paper. The essential difference between DMST and the former reported one in structure is that the turn-off of thyristor is controlled by the depletion-mode MOS in DMS and the emitter short structure is inherent, which is necessary to

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Received 21 June 1999, revised manuscript received 2 March 2000

turn off the thyristor. One advantage of our device in structure is that it can be turned off at zero gate voltage or the opposite gate voltage of the turn-on, and the nonuniform turn-off[5] can be improved, which is caused by different charge-time constants of gate voltage. The results from 2-D numerical simulations and tests on the fabricated chips show the excellent performance of DMST.

2 Device Structure and Physics

The cross-section structures of DMST Ⅰ and DMST Ⅱ are shown in Fig. 1(a) and (b), respectively. The enhancement-mode N channel MOS for turn-on thyristor, which is not given here, is formed by N emitter region, P base region and N^- drift region and is designed in the local region of a device. The depletion-mode P channel MOS for turn-off thyristor is composed of P base region, P channel region and the P^+ diverter region connected to the cathode. Obviously, the channel of depletion-mode MOS makes the thyristor emitter-base junction inherently short. The only difference between DMST Ⅱ and DMST Ⅰ is the depletion-mode P channel MOS in the former integrated in the surface of N^- drift region. The depth of P channel is designed to be its maximum depletion layer width.

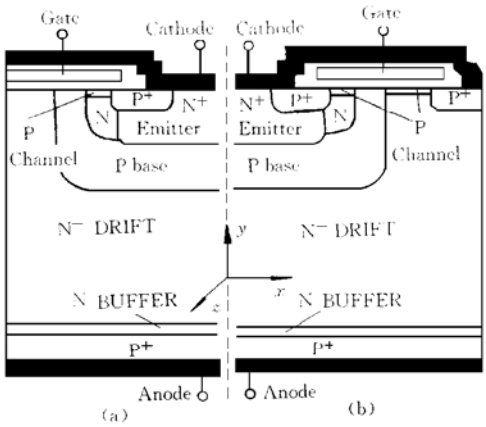

FIG. 1　Cell Cross-Sections of DMAT
(a) DMST Ⅰ, (b) DMST Ⅱ. The MOS for turn-on is located in local region and not given here.

At the application of positive gate bias, the P channel of depletion-mode MOS is depleted and the short of emitter-base junction disappears. At the same time, the reversed N channel of the enhancement-mode MOS is obtained on the surface of P base region, so electrons flow from cathode to N^- drift region passes through the reversed channel, driving the thyristor latched up. When the gate voltage reduces below the threshold voltage or to zero, the enhancement-mode MOS is turned off and the P channel of the depletion-mode MOS recovered. As a result, the device turn-off is accomplished when the majority of the carriers stored in P region flow via P channel to cathode. The maximum controllable current density of a device depends on the channel resistance of shorted emitter-base junction. The shorter the channel is, the smaller the emitter short resistance would be, so that the controllable current capability would be higher.

In DMST Ⅱ, two P channels of depletion-mode MOS on the surface of N emitter region and N^- drift region are parallel. So the shorted emitter resistance of DMST Ⅱ is less than that of DMST Ⅰ, as the DMST Ⅱ is allowed to have a higher maximum controllable current capability than DMST Ⅰ.

The controllable current capabilities of other MOS-gated thyristor, such as MCT, BRT and so on, mainly depend on the resistance of enhancement-mode MOS reversed channel, which is used to short the emitter-based junction of thyristor. This resistance is related to the carrier density and carrier mobility in the reversed channel. The carrier mobility will be reduced due to the surface electrical field scattering caused by gate voltage. In DMST, the carrier density in the P channel of depletion-mode MOS has the same order with that of the enhancement-mode MOS reversed channel. However, the turn-off operation is completed at zero gate bias, so the surface electrical field scattering could be avoided when carriers move from P base to the cathode in the channel of depletion-mode MOS at a constant high mobility. In addition, the DMST can also be turned off at a negative gate voltage, as has been done in MCT, DMT and BRT, etc. and the accumulation layer will be formed on the P channel surface of the depletion-mode MOS. So the smaller emitter shorted resistance is, the higher the maximum controllable current density and faster switch speed would be respected.

3 Device Simulation

2-D numerical simulations for DMST Ⅰ and DMST Ⅱ have been done with PISCES. The structure parameters of DMST Ⅰ are: N^- drift region and N buffer are doped with $1.2\times10^{14}cm^{-3}$ and $1.0\times10^{16}cm^{-3}$ in concentration, 45μm and 10μm in thickness, respectively. N^+, N emitter and P base, P^+ diverter region are doped with $2.0\times10^{19}cm^{-3}$, $8.0\times10^{16}cm^{-3}$, $3.0\times10^{16}cm^{-3}$, $1.0\times10^{20}cm^{-3}$ of surface concentration and 1.4μm, 1.2μm, 5.0μm, 0.7μm in depth respectively. The P channel is doped with $3.0\times10^{17}cm^{-3}$ of surface concentration, 1.5μm in channel length and the maximum width of the depletion layer to process the simulation is chosen as the junction depth. Gate oxide layer is 100nm in thickness. In DMST Ⅱ, the P^+ diverter region surface concentration in the N^- drift region is $1.0\times10^{20}cm^{-3}$ with depth of 3.0μm, the other parameters are the same as DMST Ⅰ's. Life time in the drift region is 1.0μs. The parameters above are chosen from the blocking capabilities over 500V. The P base area of DMST Ⅰ and DMST Ⅱ is about 51% of the whole cell area.

The I-V curves of DMST and MCT have been simulated for comparison at the gate voltage of 10V. The results show that the I-V characteristics of DMST Ⅰ is almost similar to that of in a wide range. But in DMST Ⅱ, the forward drop increases slightly when the anode current density is larger than $300A/cm^2$, and the increment is 0.25V when the anode current density is $1000A/cm^2$. The P channel and the P^+ diverter region in the surface of N^- drift region affect the forward drop in DMST Ⅱ. The shift of the forward drop will be down if the P channel length and P^+ diverter regions width on the surface of N^- drift region are reduced.

The transient simulations of DMST Ⅰ and DMST Ⅱ have been done with a certain resistive load. The gate voltage ramps down from 10V to 0V within 0.1μs. The simulation results show that anode voltage does not make an apparent effect on the maximum control-

lable current. The transient simulation results are shown in Fig. 2 at the anode current density of 240A/cm^2. From this figure, the DMST Ⅰ and DMST Ⅱ are of the turn-off time less than 0.5μs and 0.1μs, respectively. There is no storage time for DMST Ⅱ and it is turned off as the gate voltage down to zero. There is a storage time for DMST Ⅰ. It is also found that DMST Ⅰ is turned off in a relative small current density as the gate voltage down to zero, and then the storage time disappears. The storage time is related to the current density. However, current falls rapidly in different current densities. Also the turn-off curve of DMST Ⅱ is shown in Fig. 2 at the current density of 800A/cm^2 with its turn-off time less than 0.9μs. The simulations demonstrate that the maximum controllable current densities are over 600A/cm^2 and 1000A/cm^2 respectively for DMST Ⅰ and DMST Ⅱ in the cases above. The lateral size and junction depth of P base affect the maximum controllable current density, too.

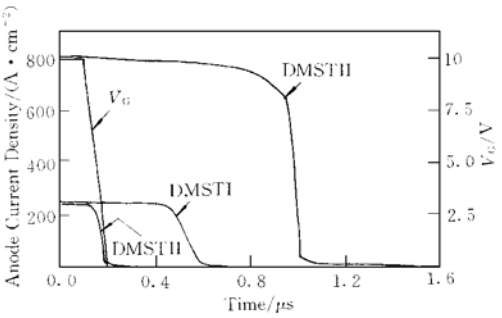

FIG. 2　2-D Transient Simulation Curves for DMST Ⅰ and DMST Ⅱ. Anode is loaded by resistive load and with voltage of 300V. Gate voltage is ramped down from 10V to zero within 0.1μs.

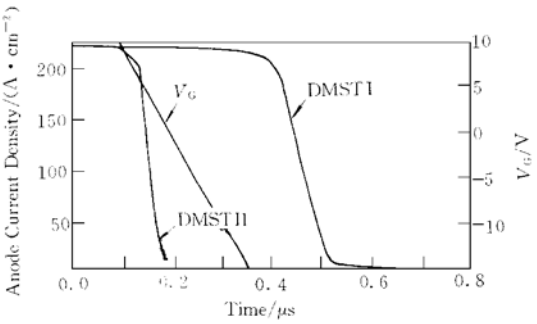

FIG. 3　2-D Transient Simulation Curves for DMST Ⅰ and DMST Ⅱ. Gate voltage is ramped down from 10V to −15V within 0.25μs.

Comparing the turn-off simulation when gate voltage varies from 10V to −15V with that when the voltage from 10V to 0V, the maximum controllable current density and the turn-off time in DMST Ⅰ and DMST Ⅱ are increased by 12% and reduced by 10% at least, respectively. It shows that the accumulation layer formed in P channel surface reduces the resistance of shorted emitter-base junction. Figure 3 presents the transient simulation results of turn-off when the gate voltage varies from 10V to −15V within 0.25μs, with the anode current density 240A/cm^2. The turn-off time of DMST Ⅰ and DMST Ⅱ descreases to 0.43μs and 0.09μs, respectively.

4　Experimental Results

The experimental devices of DMST Ⅰ and DMST Ⅱ have been fabricated in the n-type epitaxial wafer on the P^+ < 100> substrate. The resistivity and thickness of N^- drift region are 32Ω·cm and 46μm respectively. The buffer layer is 10μm thick with 1.0×10^{16}

cm^{-3} doping. Three planar field rings are used. The parameters are chosen to obtain a blocking voltage over 500V. The single-cell device and multicell device of DMST Ⅰ and DMST Ⅱ have been fabricated in the smae wafer. The structure parameters are almost the same as those used the simulation. The ratio of the thyristor area to the cell area is 58% for both single-cell and multicell devices. P based in single-cell device is designed to be $28\mu m \times 208\mu m$. The multicell active region area is $2.1 \times 10^{-3} cm^{-2}$.

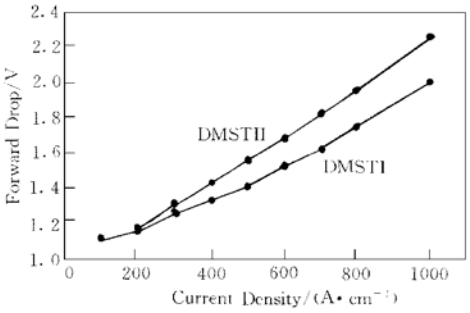

FIG. 4 Forward Properties from Tests on DMST Ⅰ and DMST Ⅱ at Gate Voltage of 15V

The measurements have been done on the forward characteristics of fabricated chips at the gate voltage of 15V. It shows that the forward drops of DMST Ⅰ and DMST Ⅱ are quite similar at small current densities. The forward drop of DMST Ⅱ is 0.2V higher than that of DMST Ⅰ's at $660A/cm^2$. Figure 4 shows the experimental curves of the multicell device. The forward drop in multicell device is slightly larger than that in single-cell's at the same anode current density.

The switch properties are measured by decreasing the gate voltages in DMST Ⅰ and DMST Ⅱ to zero, applying the anode voltage of 200V and adjusting the load resistance to obtain a maximum controllable current density. The results are as follows: the maximum controllable current densities of DMST Ⅰ and DMST Ⅱ are $810A/cm^2$ and $1060A/cm^2$ respectively for the single-cell device, however, which can exceed $960A/cm^2$ and $1260A/cm^2$ if the gate voltage is operated from 15V to −15V. For the multicell device, the maximum controllable current density of DMST Ⅰ is $460A/cm^2$ and DMST Ⅱ $600A/cm^2$, which can exceed $500A/cm^2$ and $650A/cm^2$ respectively when the gate voltage varies from 15V down to −15V. The maximum controllable current density in multicell device is less than that in single-cell's. In the fabricated devices, the channel length of DMST Ⅰ is $1.8\mu m$, in the emitter region and N^- drift region of DMST Ⅱ are $1.8\mu m$ and $2.2\mu m$ respectively. It is notable that the optimized size of junction depth in P channel equals to the width of its maximum depletion layers. Thus, the forward drop will increase if the junction is deeper while the capability for turn-off current will decrease if the junction is shallower.

5 Conclusion

The operational principle of DMST and its two structures are presented in this paper. The properties of DMST can be improved greatly if the structures are optimized. Compared with the MOS-Gated thyristors having an enhancement-mode MOS turn-off gate, DMST has following advantages: 1) It can be turned off at zero gate voltage as well as at the negative gate voltage. 2) The carriers in the depletion-mode MOS channel keep a higher mobility due to the less surface field scattering at the application of the zero gate voltage for

turn-off. The accumulation layer will be formed in P channel surface of depletion-mode MOS at the negative gate bias for turn-off. Thus, DMST can get a higher controllable current capability. 3) The switch capability of DMST is obviously improved because of the inherent resistance of shorted emitter.

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