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CMOS FinFET Fabricated on Bulk Silicon Substrate*

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Abstract: A CMOS FinFET fabricated on bulk silicon substrate is demonstrated. Besides owning a FinFET structure similar to the original FinFET on SOI, the device combines a grooved planar MOSFET in the Si substrate and the fabrication processes are fully compatible with conventional CMOS process, including salicide technology. The CMOS device, inverter, and CMOS ring oscillator of this structure with normal poly-silicon and W/TiN gate electrode are fabricated respectively. Driving current and sub-threshold characteristics of CMOS FinFET on Si substrate with actual gate length of 110nm are studied. The inverter operates correctly and minimum per stage delay of 201-stage ring oscillator is 146ps at V_d= 3V. The result indicates the device is a promising candidate for the application of future VLSI circuit.

Key words: FinFET; groove; design; fabrication; device characteristics; CMOS; bulk Si substrate
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1 Introduction

FinFET[1] is the most promising structure of various double gates devices and is capable of utilizing for mainstream IC industry. Original FinFET is a single nMOS[1] or pMOS[2] device and fabricated on ultra-thin Si film of SOI substrate. It shows excellent sub-threshold characteristic for the very thin Si fins. This paper demonstrates a design and fabrication of a FinFET on bulk silicon substrtate in detail. This device not only includes a FinFET structure but also owns a grooved planar MOSFET since its substrate is not insulator as original FinFET. The process flow is a little different from original FinFET and fully compatible with conventional CMOS process, including salicide technology. Two kinds of gate electrode, poly-silicon gate and W/TiN metal gate, are also implemented. The characteristics of the CMOS device, inverter, and CMOS oscillator are analyzed.

2 Device structure design

The double gates (DG) MOSFET shows better SCE immunity since two opposite gates shield the conducting channel. Figure 1 shows schematic diagram of the proposed device structure. Device is constructed on the normal bulk silicon substrate unlike the SOI substrate of original FinFET. Figure 1(a) is a scheme of 3D view of device. Figure 1 (b) is the scheme of 3D view of device after removing the gate material in order to disclose the Si island. Figures 1(c), (d), and (e) are SEM photos of the fabricated device. Source and drain are along the direction of channel (x-axis) and connecting the channel directly. Gate electrode is along the direction of y-axis and bridges over the two sides of

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Si island. The gate electrode in our design is a little different from original FinFET. It consists of three parts, except double gates, including a top gate, which is a 3/4-around gate to control the channel. Figure 1(e) is a SEM cross-section photo of the fabricated structure along the y-axis and illustrates this difference. The silicon island or Si fin is under the gate. In this work, final thickness of Si island is about 70nm. Figure 1(d) is a SEM cross-section photo along the x_0-axis. x_0-axis is parallel to the x-axis and at the placement in the trench outside the Si island. There is a groove in the Si substrate beyond the location of Si island. The gate electrode is a "T" gate and buried into the groove. It is isolated to the source and drain by a sidewall. Simultaneously, the gate is restricted between the spacers in the groove and it means that the gate is defined by the gap between spacers. The spacer-defining gate can achieve a smaller gate length than the limit of lithography resolution because the RIE process forms the spacer and its width can be controlled by the thickness of the deposition for spacer. The device can be designed with many parallel Si islands in the groove to increase driving current. Figure 1(c) is the planform of the fabricated device with seven Si islands.

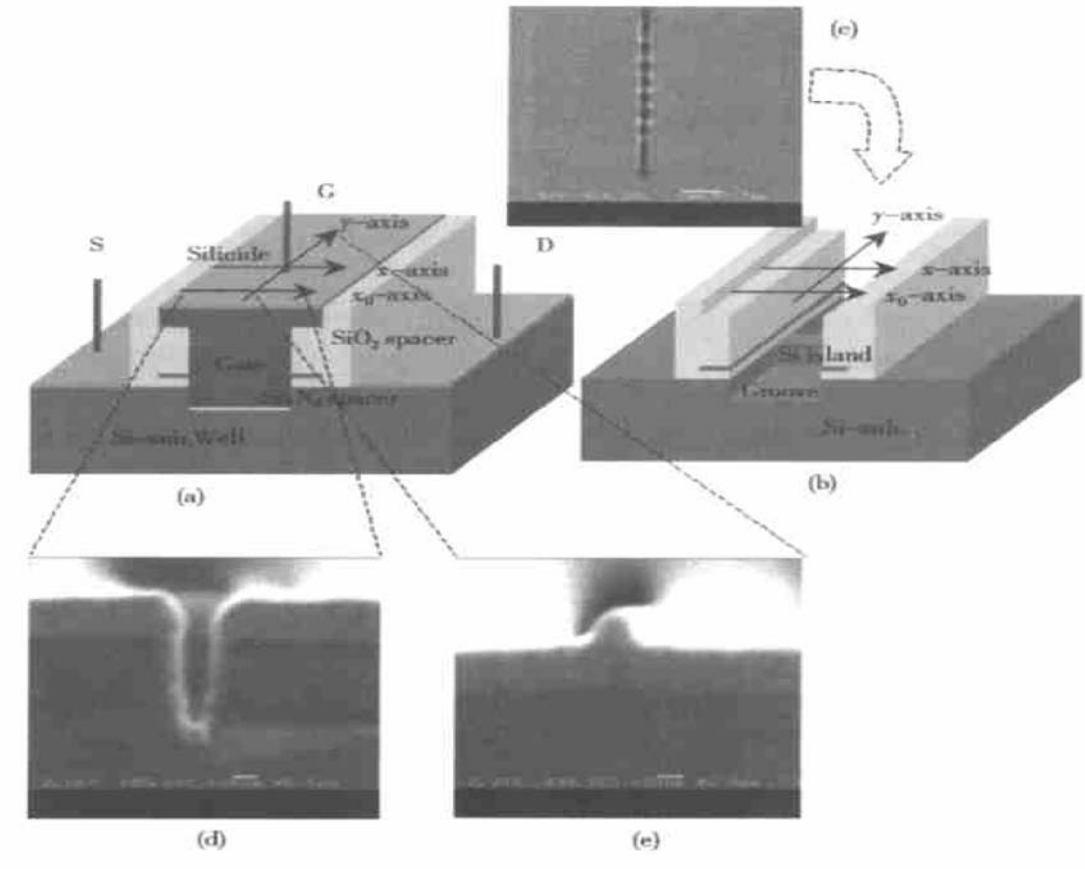

Fig. 1 (a) 3D view of FinFET on Si substrate; (b) 3D view of FinFET on Si substrate after the removal of gate material; (c) Top view of SEM; (d) SEM cross-section view in the direction of x_0-axis; (e) SEM cross-section view in the direction of y-axis of a fabricated FinFET on Si substrate

The most difference between this design and original FinFET is the former exists a planar grooved conducting channel parallel the channel of Si island. The grooved planar MOSFET on bulk silicon substrate can suppress the SCE effectively since its channel is at the bottom of the groove, the

source and drain are little raised for them to form zero or negative junction depth, so that there are two energy barriers at the corner of the groove, which is of benefit to SCE. The results of 3D device simulation indicates deteriorate the advantages of double gates, but also bring more drain current than original FinFET. The relation between the groove device and FinFET will be discussed in detail in the other paper.

Our previous work[3] has shown how to determine the structure parameters of the structure, including gate length, thickness of gate dielectric, thickness and height of Si island, thickness of spacer insulator, lateral diffusion length of source/drain in the channel, and profile of channel doping, gate electrode material etc. Optimizing these parameters are on the base of theory analysis, 3D device simulation, and process considerations. There are some other parameters related to our device structure, such as width of trench, thickness of top isolation layer, S/D junction depth etc., need to further consider.

3 Device fabrication

Figure 2 shows the process flow of our CMOS FinFET fabricated on Si substrate. The starting material is normal p-type 〈100〉 100mm Si wafer, and with a doping concentration of $1\times10^{15}\,cm^{-3}$. The twin-well process was used in order to be compatible with the normal deep sub-micron CMOS process. Surface concentration of the twin-well was equal to $1\times10^{17}\,cm^{-3}$. Then, the active area was defined and isolated by a two-step recessed LOCOS process[4]. This technology could get a nearly planar surface as STI and was beneficial for later groove etching.

In the following steps, a multi-layer insulator, HTO (high temperature oxide)/Si_3N_4/LTO (20nm/35nm/350nm) was formed. Then, a groove pattern on the sandwich layer was defined using EB direct writing for UV Ⅲ resist. The printed width of the groove was 200nm. Figure 1(d) shows its final profile and actual width along the surface of Si was 220nm. After the top LTO layer in the groove was removed by RIE, several parallel Si island patterns perpendicular to the groove were also defined by the EB direct writing. The line width after development was 130nm and it was much larger than the desired value of thickness of Si island. A resist ashing technology was used and the line width was reduced to sub 90nm. After removal of sacrificed oxide, the final thickness of Si island was 70nm, which is shown in the Fig. 1(c) and Fig. 1(e). The subsequent anisotropic etching processes removed Si_3N_4/HTO, and then bulk Si. The depth of etched Si was 100~105nm, which ensured the junction of the source and drain of planar grooved device was at the nearly same level as the bottom of groove.

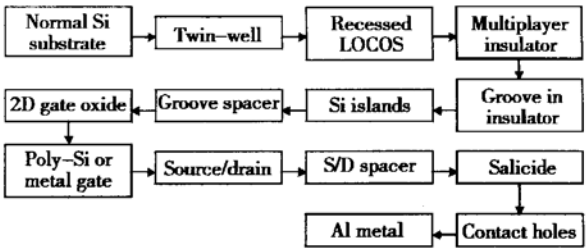

Fig. 2 Process flow of CMOS FinFET on normal Si substrate

A Si_3N_4 layer was then deposited by LPCVD over the whole wafer. The thickness of this layer was confined by the relationship: $T_{Si_3N_4}<(L_{groove}-L_g)/2$. Here, L_{groove} was width of groove and L_g was desired gate length. As a final result of this work, $T_{Si_3N_4}$ was equal to 90nm. A following Si_3N_4 etching forms the spacer in the groove. The profile of spacer in the groove decides the actual length of gate: $L_g=L_{groove}-2T_{Si_3N_4}(1-\Delta)$. Figure 1(d) indicates final thickness of Si_3N_4 spacer was equal to 55nm and L_g was equal to 110nm which was along the surface of the Si substrate. Δ is the lateral shrinkage rate of over-etching the Si_3N_4 layer. Δ must be larger than the ratio of height of Si island and thickness of top isolation layer (about 30%) so as to fully remove the spacer cling to the Si island a-

long the direction of y-axis. Next, a sacrificial oxide is grown to a thickness of 15nm by the dry O_2 oxidation. In this work, the proposed channel doping engineering was not adopted for simplifying process. After the sacrificial oxide was removed in the diluted HF solution, the residual top isolation layer on the Si island in the grooved had already been removed, which was easily removed because the island was very narrow. A 2.5nm gate oxide was subsequently fabricated at 830℃ in dry O_2 furnace. Two kinds of gate electrode materials, including poly-silicon and metal were deposited for the different wafers. Thickness of poly-silicon was 200nm. The metal gate was a multi-layer——TiN/W/TiN (35nm/100nm/15nm). W/TiN was the hottest metal material available to the gate of CMOS device. It was a near mid-gap material and showed good thermal durability, which was necessary for later rapid thermal annealing (RTA) about 1000℃. A top LTO layer of 200nm was also deposited and it shielded the doping ions passing through the metal gate during source/drain implantation with a large dose. In addition, the layer was the inhibitor of silicide reaction on the metal gate.

Next, a 0.3μm gate pattern at the groove was exposed on the gate material. After the unwanted gate material and top isolation layer was removed, the final "T" type gate was formed, which fully covered the recessed groove and Si islands. 45keV, $4\times10^{15}cm^{-2}$ of $^{75}As^{+}$ and 25keV, $3\times10^{15}cm^{-2}$ of $^{49}BF_2^{+}$ were then implanted into the wafer for the formation of source/drain of nMOS and pMOS respectively. RTA at 1005℃ activated the doping ions. Very shallow extension of source/drain for the normal planar device was not used in this structure for the reason that the FinFET was the whole Si island but the surface transmitting current, so that the SCE was a little effected by the junction depth. Following by the formation of another SiO_2 spacer adhere to the T-type gate, a Ti salicide process was used. The sheet resistance of Ti-silicide with a large area was 4.2Ω/□. Finally, the BPSG was deposited and metal interconnection was produced.

4 Results analyses

Various CMOS devices, inverters, and CMOS ring oscillators were fabricated on the wafer. Figures 3(a) and (b) show the subthreshold and output current characteristic for grooved nMOS FinFET on bulk Si with the actual gate length of

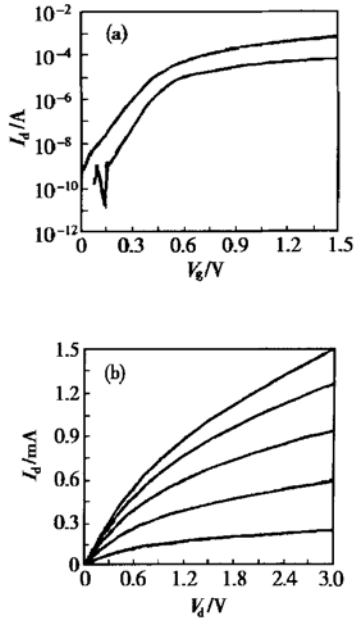

Fig. 3 (a) Subthreshold characteristic (V_d = 0.1V and 3V); (b) Output current characteristic ((V_g - V_t) from 0V to 3V) for nMOS FinFET fabricated on bulk Si substrate L_g = 110nm, W = (W_A + 14H_{Si}) = 5.4μm

110nm. Figures 4(a) and (b) show these characteristics for pMOS. The gate electrode for the device was poly-silicon and there were seven Si islands in the groove as shown in Fig. 1(c). The space between two neighbouring islands was 0.3μm. nMOS drive current was 278μA/μm at (V_g - V_{th}) = 3V and V_d = 3V. V_{th} was 0.12V for nMOS, here V_{th} was defined as the value of V_g at I_d = 1nA/μm, and the off-state current (V_g = 0V) is less than 20pA/μm. The effective channel width (W) was nearly defined as (W_A + 2nH_{Si}). The W_A was the width of the active area in the direction of y-axis and W =

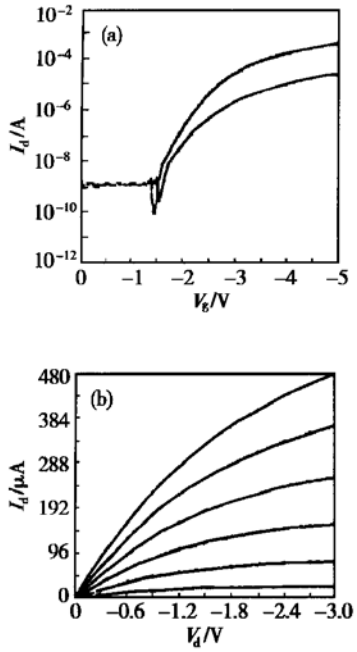

Fig. 4　(a) Subthreshold characteristic(V_d= − 0.1V and − 3V); (b) Output current characteristic((V_g − V_t) from − 0V to − 3V) for pMOS FinFET fabricated on bulk Si substrate　L_g= 110nm, W= (W_A + 14H_{Si}) = 5.4μm

4μm. The n is the number of Si islands and n= 7, which is shown in Fig. 1(c). H_{Si} is the height of Si island and H_{Si}= 100nm. However, the definition of effective channel width is very conservative. Simulation data indicate the thin Si island owns much more high current density than that of planar grooved device, but the former has to be charged with the great device width of the later. Actually, the device without Si island is also fabricated on the wafer. After the driver current offered by the grooved device is removed, the nMOS drive current of pure Si island is over 450μA/μm under the same bias (It will be discussed in detail in other paper). On the other hand, the absolute value of V_{th} of pMOS is very large, about 2.0V (− 2.0V), so the driving current is very small, about 90μA/μm at V_g − V_{th} = − 3V and V_d = − 3V. The large pMOS threshold voltage is due to an unreasonable doping concentration in the n-well.

The subthreshold swing and drain induced barrier lowering (DIBL) of CMOS device are 90mV/dec and 50mV/V for nMOS, 180mV/dec and 30mV/V for pMOS, respectively. Because the modulating effect of drain junction under different V_d in pMOS, the DIBL voltage is smaller than that of nMOS. Comparing to the normal planar MOSFET with the same channel doping, the FinFET on Si substrate shows better SCE immunity. However, it is much worse than that of original FinFET. The reason maybe: (1) the actual thickness of Si island is too large and should be less than 50nm reference to the theoretical analyses; (2) a better channel doping profile is necessary to reduce the effect of groove device. Figures 5(a) and (b) show the output wave for the CMOS groove FinFET inverter and ring oscillator. The input voltage is transformed perfectly in the inverter. The average per stage delay of 201-stage ring oscillator is 146ps at V_d= 3V.

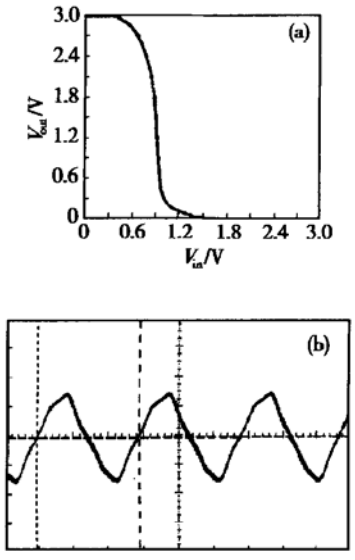

Fig. 5　Output waves of inverter (a) and 201-stage ring oscillator (b) of the CMOS FinFET on bulk Si substrate at V_d= 3V　Delay of oscillator is equal to 146ps/stage.

Results of the device with W/TiN gate are much worse than that with poly-silicon for the process reason, which is not presented here.

5　Conclusion

A FinFET structure was fabricated successful-

ly at the first time on the normal bulk Si substrate. It combines both FinFET and grooved planar MOSFET that means it is a mixed gate device products. Unlike original FinFET, its process flow of fabrication is fully compatible with conventional CMOS process. Not only the CMOS device, but also the CMOS inverter and oscillator are manufactured. The device and circuit can operate correctly. It first demonstrates the feasibility of self-aligned double gate device integrated into normal deep submicron CMOS process on bulk Si substrate. By optimizing channel engineering, gate material, and process conditions, especially thinning and densing the Si island with an improved lithography technology and improving the control of S/D depth, the device will achieve a greater drive current and suppress SCE more efficiently.

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体硅衬底上的 CMOS FinFET*

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摘要: 介绍了一种制作在普通体硅上的 CMOS FinFET. 除了拥有和原来 SOI 上 FinFET 类似的 FinFET 结构, 器件本身在硅衬底中还存在一个凹槽平面 MOSFET, 同时该器件结构与传统的 CMOS 工艺完全相容, 并应用了自对准硅化物工艺. 实验中制作了多种应用该结构的 CMOS 单管以及 CMOS 反相器、环振电路, 并包括常规的多晶硅和 W/TiN 金属两种栅电极. 分析了实际栅长为 110nm 的硅基 CMOS FinFET 的驱动电流和亚阈值特性. 反相器能正常工作并且在 V_d= 3V 下 201 级 CMOS 环振的最小延迟为 146ps/门. 研究结果表明在未来 VLSI 制作中应用该结构的可行性.

关键词: FinFET; 凹槽; 设计; 制作; 器件特性; CMOS; 体硅

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