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Design Aspects of CMOS Compatible On-Chip Antenna for Applications of Contact-Less Smart Card

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Abstract: Design aspects of CMOS compatible on-chip antenna for applications of contact-less smart card are discussed. An on-chip antenna model is established and a design method is demonstrated. Experimental results show that system-on-chip integrating power reception together with other electronic functions of smart card applications is feasible. In a 6×10^{-4}T magnetic field of 22.5MHz, an on-chip power of 1.225mW for a 10kΩ load is obtained using a 4mm^2 on-chip antenna.

Key words: on-chip antenna; contact-less smart card; CMOS
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1 Introduction

The Smart Card market enters a new period of booming number of applications in various domains. More countries are willing to use this technique. Smart Cards are becoming more and more ubiquitous.

Since most applications require low-cost and low-power systems, integrating the whole system including the antenna on a single chip should pave a way to new reliable low-cost contact-less smart card chips.

There are four concerns that dominate the on-chip antenna design: antenna area, parasitic series resistance, bulk capacitance, and induced voltage. There have been solutions such as fabricating of antenna on insulators, using MEMS technologies, taking advantage of low resistivity metal materials and making use of ferrite cores[1~6]. However, to obtain low-cost integration of antennas, increasing of process complexity should be avoided.

Since the first on-chip antenna making use of conventional CMOS process, there're only a few researches and applications reported on CMOS compatible implementation of on-chip antenna[7~9].

In this paper, we dicuss the design aspects of CMOS compatible on-chip antenna of smart card applications. An experimental chip is presented to demonstrate our design.

2 Inductive coupling principle

As illustrated in Fig. 1, from the mutual inductance between the on-chip antenna and the reader/writer antenna, power supply, clock signal and data are recovered.

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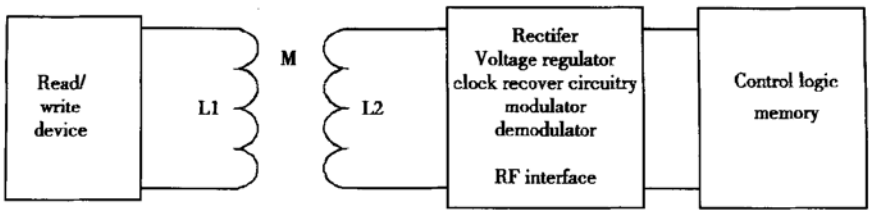

Fig. 1 Illustration of inductive coupling

The open-circuit voltage (V_{2P-P}) induced on the on-chip antenna L_2 as a function of the current (I_{1P-P}) in the reader/writer antenna is given by

$$V_{2P-P} = MI_{1P-P} \tag{1}$$

Using the Biot-Savart law to the reader/writer antenna and Faraday's law to the on-chip antenna, we can calculate the mutual inductance (M) by

$$M = 2\pi f u_0 A \frac{R^2}{2(X^2 + R^2)^{3/2}} \tag{2}$$

where f is the operating frequency, u_0 is vacuum permeability (No magnetic materials are considered here), A is the total equivalent on-chip antenna area, R is the radius of the reader/writer antenna, and X is the coupling distance, as illustrated in Fig. 2.

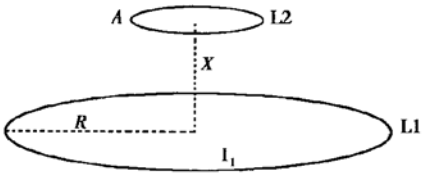

Fig. 2 Coupling between two antennas

From formula (2), we can see that when R, I_1, and X are fixed, the open circuit voltage is determined by f and A. For smart card application, operating frequency f is also fixed, therefore, in order to get sufficiently high open circuit voltage, an enough equivalent on-chip antenna area A must be guaranteed.

For a square planar spiral on-chip antenna, as shown in Fig. 3, its equivalent area is given by

$$A = l^2 + (l - 2e)^2 + \cdots + (l - 2ne)^2 \tag{3}$$

which can be simplified into

$$A = nl^2 - 2len(n + 1) + (2/3)e^2n(n + 1)(2n + 1) \tag{4}$$

where n is number of turns, l is external side of the square, and e is pitch of the spiral.

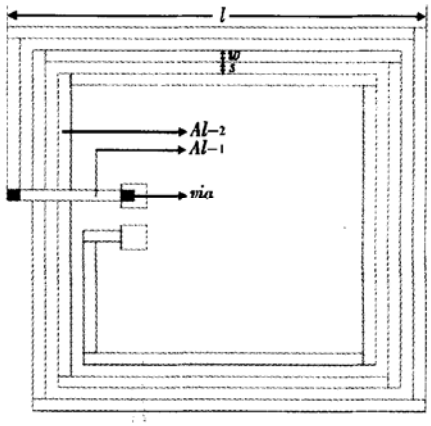

Fig. 3 Spiral on-chip antenna

3 On-chip antenna modeling

For Si-based RF IC's, the three-port lumped physical model of on-chip antenna illustrated in Fig. 4 is widely used in the literatures[10, 11].

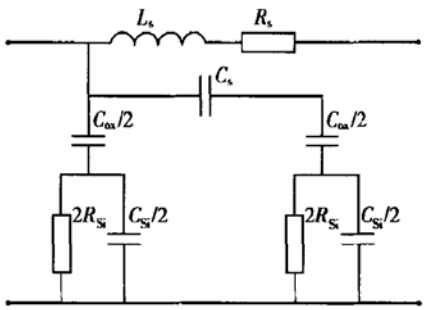

Fig. 4 Three-port lumped physical model

In the model, the inductance L_s and other passive component values are predicted as

$$L_s = 0.01205(l - ne)n^{5/3}\ln 4(l - ne)/ne \tag{5}$$

$$R_s = \rho l_A/[w\delta(1 - e^{-t/\delta})] \quad (6)$$

$$C_s = nw^2\epsilon_{ox}/t_{oxmetal} \quad (7)$$

$$C_{ox} = l_A w \epsilon_{ox}/t_{ox} \quad (8)$$

$$C_{Si} = l_A w C_{sub} \quad (9)$$

$$R_{Si} = l/(l_A w G_{sub}) \quad (10)$$

where ρ is metal resistivity, δ is metal skin depth, t is metal thickness, w is metal width, l_A is total metal length, $t_{oxmetal}$ is thickness of oxide between spiral and underpass, t_{ox} is thickness of oxide between spiral and substrate, C_{sub} is substrate capacitance per unit, and G_{sub} is substrate conductance per unit.

In this model, L_s represents the spiral inductance, which is computed using the Greenhouse method. R_s is the metal series resistance. This resistance symbolizes the energy loss in the spiral interconnect structure. The series feedforward capacitance C_s accounts for the capacitance due to the overlaps between the spiral and the center-tap underpass. The effect of the fringing capacitance between adjacent metal lines is neglected, because the adjacent turns are nearly equipotential. C_{ox} represents the oxide capacitance between the spiral and the substrate. The silicon substrate capacitance and resistance are modeled by C_{Si} and R_{Si}, respectively.

However, the physical phenomena behind the substrate effects are complicated to characterize. Furthermore, as on-chip antenna occupies substantially chip area, it can potentially be the source and receptor of detrimental noise coupling. References [12, 13] provide CMOS compatible methods to decoupling the antenna from the substrate, which used a patterned ground shield or p-n junction to improve isolation. Using these methods, we can get a much simplified model as shown in Fig. 5 and at the same time preserve the antenna characteristics[11, 12].

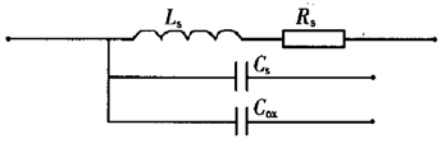

Fig. 5 Simplified model

Since smart card applications usually work at frequencies from kilo- to mega-Hz, at which substrate noise coupling is relatively insignificant[14]. So when a substrate isolation method is used, this simplified model is sufficiently accurate and will be used in the following discussion.

Here L_s, R_s, C_s, and C_{ox} can be calculated by formula (5) ~ (8). For smart card application frequencies since the metal skin depth δ is much greater than metal thickness t (1μm or so in CMOS technology), formula (6) can be simplified as

$$R_s = \rho l_A/[wt] \quad (11)$$

where

$$l_A = 4[l + (l - 2e) + \cdots + (l - 2ne)] = 4n[l - (n + 1)e] \quad (12)$$

4 Design aspects of on-chip antenna

4.1 Antenna area and total equivalent area

The most critical aspect of the on-chip antenna implementation is antenna area. Economic estimates show that the area less than 4mm^2 seems to represent a good challenge[8]. This results in a maximum external side length of the square antenna l_{max}= 2mm.

As mentioned in section 2, on-chip implemented antenna must provide sufficient power for all the electronic functions foreseen for smart card applications. Therefore in the first place the antenna must have an enough total equivalent area A, which determines the induced open-circuit voltage. According to Faraday's law,

$$V_{2P-P} = 2\pi f BA \quad (13)$$

when the operation frequency (f) and the magnetic induction intensity (B) is fixed, V_{2P-P} is determined by A.

As the induced voltage must be rectified to obtain a DC power voltage, the open circuit DC output ($V_{DC-OPEN}$) is halved from V_{2P-P} with a voltage loss of about 0.7V using a full wave rectifier, which can be expressed by

$$V_{DC-OPEN} = 1/2V_{2P-P} - 0.7V \quad (14)$$

When the required minimum $V_{DC\text{-}OPEN}$ is determined, the minimum total equivalent area can be calculated. Using formula (4), (13), and (14), we can get the first equation using the geometric dimensions of the on-chip antenna as variables,

$$A = nl^2 - 2len(n+1) + (2/3)e^2n(n+1)(2n+1) = 2(V_{DC\text{-}OPEN} + 0.7)/(2\pi f B) \quad (15)$$

where $l_{max} = 2$mm.

From formula (15), as the external side of the antenna l is in the range of 1mm to 2mm, and the pitch of the spiral e is only a few micron meter, we can get the conclusion that number of turns n and external side l should be as large as possible, and pitch of the spiral e should be as narrow as possible considering the total equivalent area.

4.2 Antenna inductance, serial resistance, and parasitic capacitance

Referring to formula (7), (8), (11), and (12), we can get the expression of antenna inductance, serial resistance R_s and parasitic capacitance C using on-chip antenna geometric dimensions,

$$L_s = 0.01205(l - ne)n^{5/3}\ln 4(l - ne)/ne \quad (5)$$

$$R_s = \rho 4n[l - (n+1)e]/[wt] \quad (16)$$

$$C = C_{ox} + C_s = 4n[l - (n+1)e]w\epsilon_{ox}/t_{ox} + nw^2\epsilon_{ox}/t_{oxmetal} \quad (17)$$

R_s should be minimized as it symbolizes the energy loss in the antenna, which means that number of turns n and external side l should be minimized, and pitch of the spiral e and metal line width w should be maximized when R_s is considered.

Unlike on-chip coil used as passive low noise components in other microwave or RF applications where the self-resonant frequency of the coil should be adjusted far beyond the operation frequency, here antenna inductance and parasitic capacitance are used to tune the antenna. This means the self-resonant frequency should be tuned nearly equal to the operation frequency. Thus, after the approximate ranges of n, l, and w, e are determined by the requirements of total equivalent area (A) and serial resistance (R_s), they should be fine adjusted to tune the antenna. This means when the antenna itself can resonate by adjusting geometric dimensions, no extra tuning capacitance is needed.

4.3 Substrate isolation

Although substrate losses are insignificant for most smart-card-application frequency and the simplified model shown in Fig. 5 is sufficiently accurate, substrate isolation methods should be better to be used to improve the antenna performance.

The substrate losses are caused by two ways. One is the vertical potential drop in the semiconductor caused by the electric field penetrating from the antenna, which is modeled by C_{Si} and R_{Si} shown in Fig. 4. The other is the eddy currents induced by the magnetic field of the spirals.

Yue *et al.*[12] put a patterned ground shield under the antenna, as shown in Fig. 6. Using this technique, the electric field of the antenna is terminated before reaching the silicon substrate, which means the antenna characteristics are much more independent on the substrate.

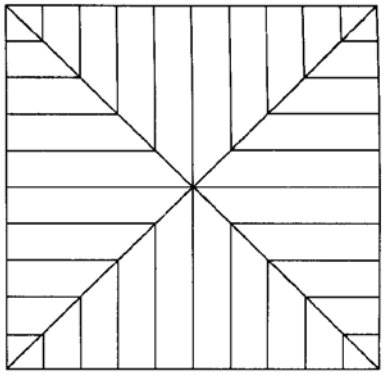

Fig. 6 Patterned ground shield

Liu et al.[13] used substrate p-n junction to block eddy currents, as shown in Fig. 7.

Using this method, inductor Q value can be improved by 40% as reported.

5 Experimental setup

We made use of a standard 1.2μm E^{2}PROM CMOS process with two metal layers. The spiral of

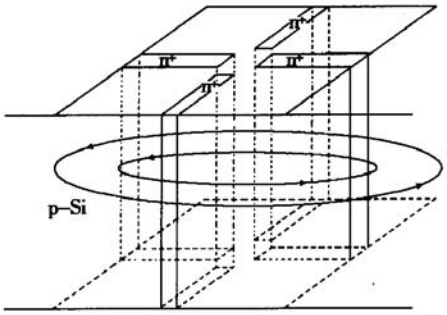

Fig. 7 Substrate pn junction

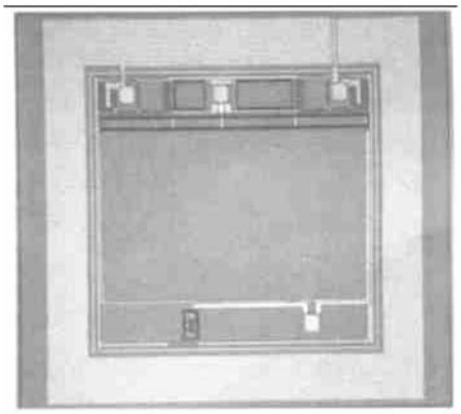

Fig. 8 Photograph of On-Chip Antenna

the antenna was formed by the second metal layer (Al2) and the underpass was formed by the first metal layer (Al1). The sheet resistance for Al1 was 35Ω and 25Ω for Al2. The isolating oxide thickness between the first metal and the silicon substrate was about 1.2μm. Inter-metal dielectrics (BPSG and PSG) between the two metal layers was deposited and planarized with a final thickness of 0.8μm.

The test antenna used a planar square spiral structure. Geometric dimensions were as listed: n= 30, l= 2mm, w= 6μm and e= 10μm. Using formula (5), (15), (16), (17), the values of the parasitic components were calculated as: L_s= 1.85μH, R_s= 1kΩ, C= 25pF, and the total equivalent antenna area A = 117mm^2. The antenna self-resonance frequency should be at 23.4MHz according to the calculated L_s and C.

The photograph of the fabricated on-chip antenna is shown in Fig. 8. The circuitry consists of an on-chip antenna, a full wave rectifier (FWR), and an on-chip 100pF capacitor. The FWR is made from pMOS transistors, instead of more classical diodes, which are not compatible to CMOS processes.

To achieve better yield, we use both of the above-mentioned substrate isolation solutions. A patterned ground shield as illustrated in Fig. 6 is formed directly under the antenna with poly-2 to terminate electric field from the antenna, and N^+ wells on the substrate as illustrated in Fig. 7 are formed to stop eddy currents in the substrate.

6 Results and discussion

Parasitic parameters were measured using HP 4284A. As were the measured values: L_s= 2μH, R_s = 1.15kΩ, C= 27pF. The measured antenna self-resonance frequency was 22.5MHz.

All the measured R_s, L_s, and C are 10~ 15% larger than the calculated value, because we haven't taken the underpass and via into account in formula (5), (15), (16), and (17).

Using the simplified model shown in Fig. 5 and the measured L_s and C, the antenna self-resonant frequency should be at 21.6MHz. Compared to the measured antenna self-resonance frequency of 22.5MHz, this result can sufficiently verify our model.

At 22.5MHz, in the magnetic field of about 6Gauss, we measured an open-circuit DC output of 4.6V. According to formula (14), the induced open-circuit voltage of the on-chip antenna was 10.6V. This value verifies our design using formula (15).

For the magnetic field above, an output DC voltage of 3.5V was obtained for a 10kΩ load. This is equivalent to an available on-chip power of 1.225mW, sufficient for the on-chip implementation of all the electronic functions foreseen for smart card applications.

7 Conclusion

Design aspects of CMOS compatible on-chip antenna for smart card applications are discussed. An on-chip antenna model is established and a design method is demonstrated. Experimental results show that system-on-chip integrating power reception together with other electronic functions such as RF communication and signal processing is feasible. Future investigations will focus on the design of a contact-less smart card using on-chip antenna.

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用 CMOS 工艺实现非接触式 IC 卡天线的集成化设计

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摘要：论述了用 CMOS 工艺实现非接触式 IC 卡天线的集成化需要考虑的各个方面，建立了集成天线的模型，给出了合理的设计方案，并通过实验验证了模型和设计方案. 实验结果表明，采用片上天线完全可以提供非接触式 IC 卡工作所需要的能量. 在频率为 22.5MHz、感应强度为 6×10^{-4}T 的磁场中，面积为 2mm×2mm 的集成天线可以为 10kΩ 的负载提供 1.225mW 的能量.

关键词：集成天线；非接触式 IC 卡；CMOS

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