第 24 卷第 5 期 半 导 体 学 报 Vol. 24, No. 5
2003 年 5 月 CHINESE JOURNAL OF SEMICONDUCTORS May, 2003

CMOS Mixers for 2.4GHz WLAN Transceivers

Chi Baoyong and Shi Bingxue

(*Institute of Microelectronics, Tsinghua University, Beijing* 100084, *China*)

Abstract: A down-conversion mixer and an up-conversion mixer for 2.4GHz WLAN transceivers are presented. The down-conversion mixer uses a class-AB input stage to get high linearity and to realize input impedance matching and single-ended to differential conversion. The mixers are implemented in 0.18μm CMOS process. The measured results are given to show their performance.

Key words: WLAN transceivers; mixer; Gilbert cell
EEACC: 1250
CLC number: TN43 **Document code**: A **Article ID**: 0253-4177(2003)05-0472-04

1 Introduction

Mixers are widely used in modern communication systems in order to realize frequency translation of the carrier signals. Their performance has an important effect on the dynamic range of the whole communication systems. Usually, the mixers must have high linearity, low noise figure, and good port isolation. Moreover, their input/output impedance must be matched to 50Ω for monolithic mixers.

In this paper, we present a down-conversion mixer for 2.4GHz WLAN receivers and an up-conversion mixer for 2.4GHz WLAN transmitter. They have been implemented in 0.18μm CMOS process. The measured results are given to show the mixer performance.

2 Down-conversion mixer

The schematic of the down-conversion mixer is shown in Fig. 1. It could be divided into three parts: input stage, switching pairs, and output buffer. The input stage consists of M1~M3. It converts the single-ended input voltage into differential currents. The input stage works in class-AB mode to have a high linearity[1~3]. The g_m of M1 is set to 50mS to fulfill the wide-band input impedance matching. To maintain the symmetry, the g_m of M3 is also set to 20mS. The switching pairs consist of M4~M7 driven by LO signals. Their sizes are optimized to get a low noise figure. Two open-drained nMOSs are used as the output buffer, whose role is to isolate the mixer core from the off-chip load.

The mixer has been implemented in 0.18μm CMOS process. Figure 2 shows the die microphotograph. The die shape is not the regular rectangle for the reason that it is only one block in the whole die.

To reduce the effect of the package on the circuit performance, the bare die is directly bonded on a printed circuit board (PCB) with all required external components mounted on it. The outputs of the buffer are converted into a single-ended signal

Chi Baoyong male, PhD candidate. His work focuses on the analog circuit design and RF front-end circuit design.
Shi Bingxue male, professor. His research interests include mixed-signal circuit design, VLSI implementations of artificial neural networks and fuzzy logic, DC-DC converters, and RF circuits.

Received 25 August 2002, revised manuscript received 13 December 2002

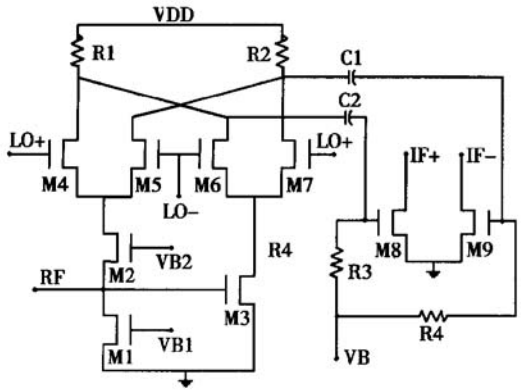

Fig. 1 Schematic of down-conversion mixer

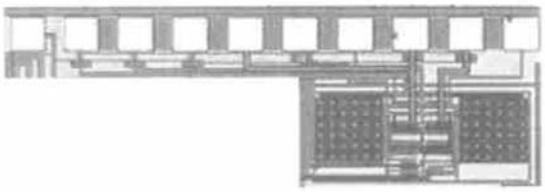

Fig. 2 Layout of down-conversion mixer

by a differential to single-ended conversion circuit and then connected to the test equipments through a SMA connector. The differential to single-ended conversion circuit uses the most popular topology as shown in Fig. 3. L2 is the AC choke inductor used to bias the transistors in the output buffer. C3 is the AC-coupled capacitor. C1, C2, and L1 should satisfy the following formula:

$$f_{IF} = \frac{1}{2\pi\sqrt{2L_1C_1}} \quad \text{and} \quad C_1 = C_2$$

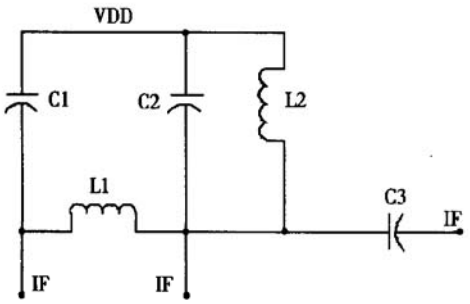

Fig. 3 Differential to single-ended conversion circuit

The measured conversion gain is − 4.5dB as shown in Fig. 4. The input RF power level is − 20dBm with a frequency of 2.40GHz; the LO power level is 6dBm with a frequency of 2.16GHz. It must be mentioned that the − 4.5dB conversion gain includes all the off-chip loss: SMA connector, PCB, and coaxial-cable. Such loss is difficult to measure due to frequency-translation operation. We only estimate the loss is 2~ 3dB.

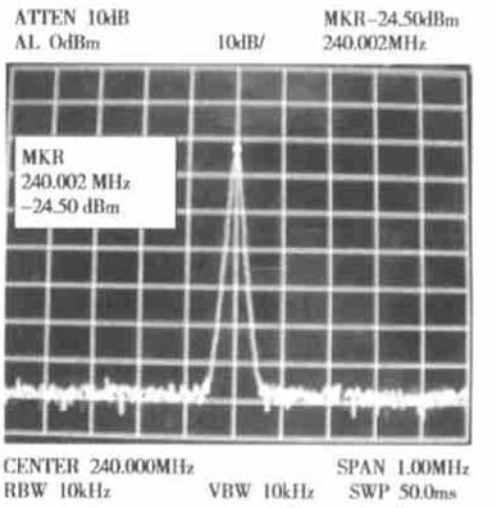

Fig. 4 IF output spectrum of the down-conversion mixer

Linearity is another parameter. Due to limited conditions, we only measure 1dB compression point (P_{1dB}). Figure 5 shows the measured results. It could be deduced from the figure that the input P_{1dB} is about 1dBm.

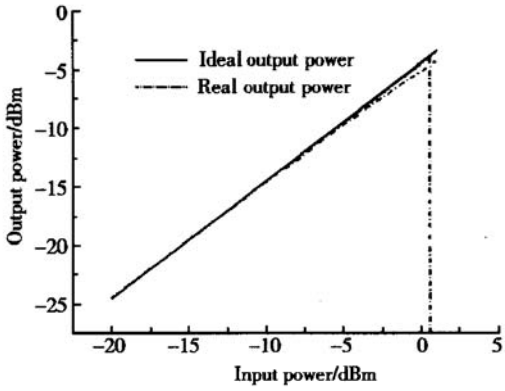

Fig. 5 Magnitude response of the down-conversion mixer

Noise figure and input port return loss are also measured, and the results are summed in Table 1. It must be mentioned that the results include all

the off-chip loss which is about 2~ 3dB. It must be deducted for the true performance of the down-conversion mixer.

Table 1 Performance summary of the down-conversion mixer

Conversion gain	P_{1dB}	Noise figure	S_{11}
- 4.5dB	1dBm	18dB	- 10dB

The power consumption is 40mA when the power supply is 1.8V. Only 10mA current is consumed by the mixer core, and the other is consumed by the output buffer to drive 50Ω load. If the mixer is integrated together with other RF blocks, the output buffer will not needed and its current consumption could be saved.

3 Up-conversion mixer

The schematic of the up-conversion mixer is shown in Fig. 6. It is a standard Gilbert cell multiplier. The input impedance matching is realized by the off-chip 50Ω resistors. The output RF signals are converted into single-ended signal by a RF balun and connected to the measured equipments through a SMA connector. At the input port, a simply single-ended to differential conversion is realized by a simple LC network.

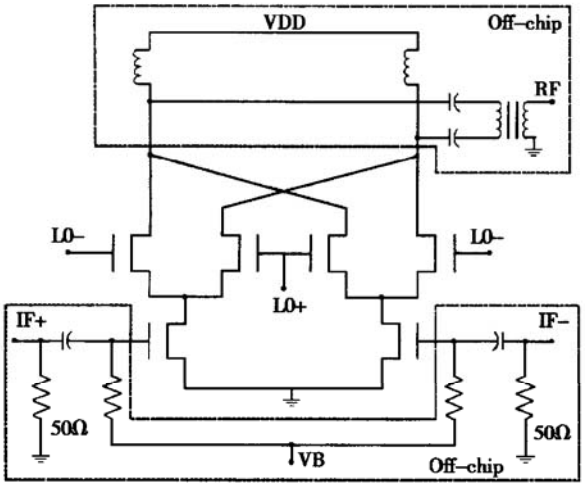

Fig. 6 Schematic of the up-conversion mixer

The up-conversion mixer has also been implemented in 0.18μm CMOS process. Its microphotograph is shown in Fig. 7. And the measured results are summed in Table 2. The results also include all the off-chip loss which is about 2~ 3dB. Moreover, The RF balun will induce excess 1dB loss, and the input off-chip 50Ω resistors will directly add the noise figure by 1dB. All these must be deducted for the true performance of the up-conversion mixer.

The power consumption is 14.6mA when the power supply is 1.8V.

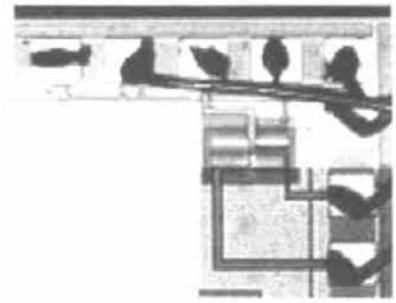

Fig. 7 Microphotograph of the up-conversion mixer

Table 2 Performance summary of the up-conversion mixer

Conversion gain	P_{1dB}	Noise figure	LO-RF isolation	IF-RF isolation
- 0.50dB	- 19dBm	13dB	- 25.33dB	- 18dB

4 Conclusion

The paper presents a down-conversion mixer and an up-conversion mixer for 2.4GHz WLAN transceivers. Although the circuits have to be improved to satisfy the performance requirements of IEEE 802.11b transceivers, they could be taked as a start-point to realize the whole integrated transceivers.

References

[1] Gilbert B. The micromixer, a highly linear variant of the gilbert mixer using a bisymmetric class-AB input stage. IEEE J Solid-State Circuits, 1997, 32(9): 1412

[2] Orsatti P, Piazza F, Huang Qiuting. A 20-mA-receive, 55-mA-transmit, single-chip GSM transceiver in 0.25-μm CMOS. IEEE J Solid-State Circuits, 1999, 34(12): 1869

[3] Huang Qiuting, Orsatti P, Piazza F. GSM transceiver front-end circuits in 0.25-μm CMOS. IEEE J Solid-State Circuits, 1999, 34(3): 292

用于 2.4GHz 无线局域网收发机的 CMOS 混频器

池保勇　石秉学

(清华大学微电子学研究所, 100084　北京)

摘要: 描述了采用 CMOS 工艺技术, 用于 2.4GHz 无线局域网收发机的上变频器/下变频器的实现. 由于采用 class-AB 类工作模式的输入级, 该下变频器具有很高的线性度. 同时, 该输入级也完成了输入阻抗匹配和单端信号到差分信号的转换功能. 它们采用 0.18μm CMOS 工艺实现. 为了说明它们的性能, 文中给出了每个模块的测试结果.

关键词: 无线局域网收发机; 混频器; Gilbert 单元

EEACC: 1250

中图分类号: TN43　　**文献标识码**: A　　**文章编号**: 0253-4177(2003)05-0472-04

池保勇　男, 博士研究生, 研究方向为模拟和射频前端电路设计.

石秉学　男, 教授, 研究方向包括数模混合信号设计、人工神经网络和模糊逻辑的 VLSI 实现、DC-DC 变换器和射频电路设计技术.

2002-08-25 收到, 2002-12-13 定稿