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Signal Integrity for 0.18μm CMOS Technology

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Abstract: The signal integrity problem in 0.18μm CMOS technology is analyzed from simulation. Several rules in this phenomenon are found by analyzing the crosstalk delay and noise, which are helpful for the future circuit design.

Key words: interconnect delay; signal integrity; crosstalk; noise

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1 Introduction

The driving force behind the spectacular advancement of the integrated circuit technology in the past thirty years has been the exponential scaling of the transistor feature size, i.e. the minimum dimension of a transistor. The feature size decreased from about 2μm in 1985, to about 1μm in 1990 and to 0.10μm today (2003). It has been following the Moore's Law[1] at the rate of a factor of 0.7 reductions every three years. Such exponential scaling will continue for several years as projected in National Technology Roadmap for Semiconductors[2].

According to the simple scaling rule described in Ref.[3], when the devices and interconnects are scaled down in all three dimensions by a factor of $S(S<1)$, the intrinsic gate delay and the interconnect delay have been influenced differently by the factor S[4]. The intrinsic gate delay is reduced by a factor of S, but the delay of global interconnects increases by a factor of S^{-2}. As a result, the interconnect delay has exceeded the device delay and become the dominating factor in determining system performance. At the same time, in order to prevent the interconnect resistor from not to increase too fast, the interconnect is produced as high as possible, so the height to the width ratio of the interconnect is increasing. As a result, the coupling capacitance between adjacent interconnects in the same metal level will become a major component in the total capacitance. The coupling capacitance will cause crosstalk delay and noise to the interconnects. In 0.18μm technology, these parasitic effects are obvious, and in some cases it can make chip fail. So interconnect delay and crosstalk must be analyzed and optimized in 0.18μm technology circuit design.

2 Signal integrity

As we all know, any signal in digital system can tolerate certain level of noise and delay. When the signal cannot reach the certain level of voltage in certain time, we call this phenomena signal integrity problem, as shown in Fig. 1[5].

As mentioned above, the coupling capacitance can cause crosstalk delay and noise to the interconnect, so it must be in consideration for the circuit design, in fact crosstalk has become one of the critical problems in DSM chip designs as a result of technology evolution.

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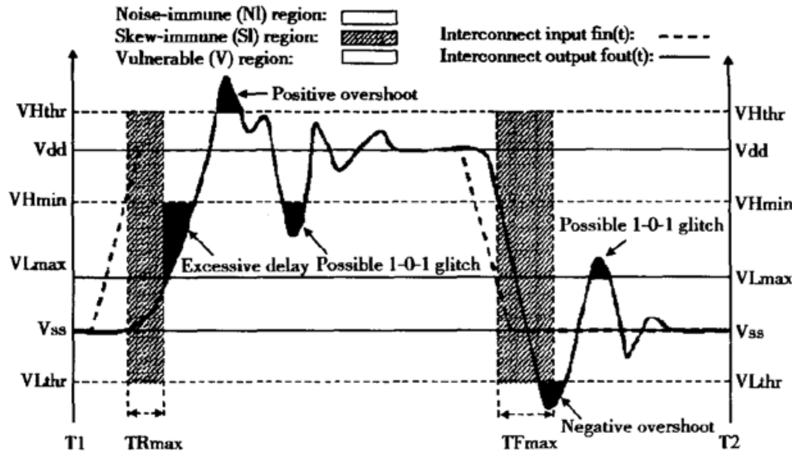

Fig. 1　Practical diagram of integrity loss metric

Impact of the crosstalk in 0.18μm technology is investigated using the simulation test structures as shown in Fig. 2. We use HSPICE to simulate the test circuit. In all test structures, they have the same supply voltage V_{DD}. In situation (a) of Fig. 2, there is only one interconnect, and no coupling capacitance, its delay is just determined by its intrinsic capacitance C_{intr}(C_{bottom} + C_{top}) and its resistance. That is to say, this delay is the intrinsic delay D_{intr}. In situation (b), there are three minimum width interconnects arranging parallel in minimum spacing. The middle interconnect switches, and the other two keep inactive. In situation (c), these three interconnects switches in the same direction simultaneous. In situation (d), the middle interconnect switches in the opposite direction with its two neighbors. Structure (e) is used for noise simulation. The delay simulation result is shown in Figs. 3, 4,

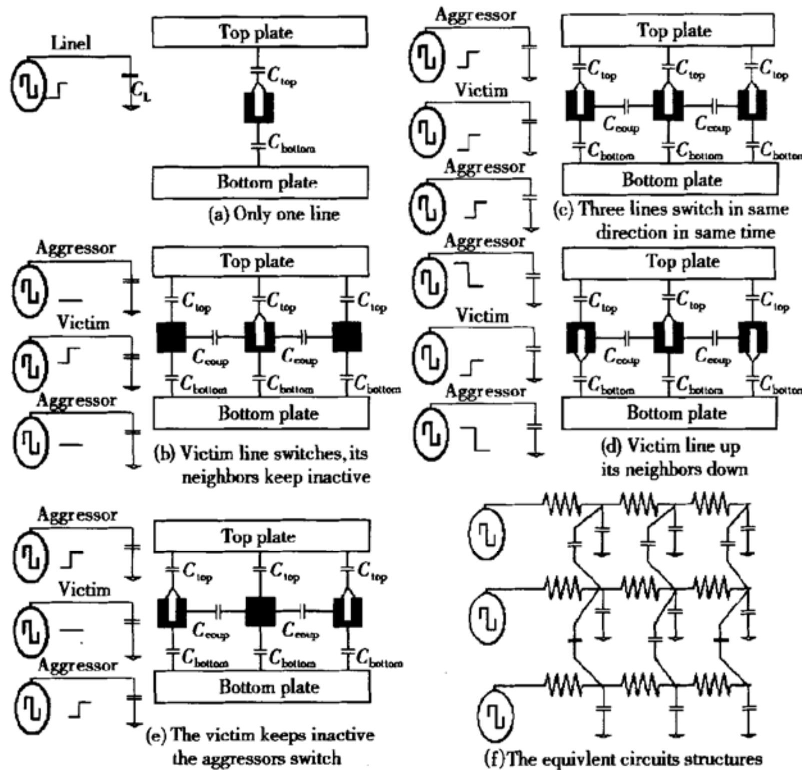

Fig. 2　Schematics of test structures for interconnects crosstalk simulation

and 5. From the simulations, we can get some conclusions:

(1) The interconnect delay increases with the interconnect length.

(2) In (b), (d) test structures, the delay does not equal to intrinsic delay. Coupling capacitance causes crosstalk delay D_{extra}.

(3) In (b), (c), (d) test structures, the circuits have the same coupling capacitances, but their delays are different, so the capacitive crosstalk delay is relevant to switching patterns.

(4) In (c) test structure, the delay equals to intrinsic delay. That is to say, in this situation the coupling capacitance has no influence on the circuit delay.

(5) As shown in Fig. 4, the capacitive crosstalk delay is sensitive to the spacing.

(6) Situation (d) is the worst case, in this situation the circuit has the longest delay, its D_{extra} is several times of the D_{intr}, and so this situation should be avoided in the circuit design.

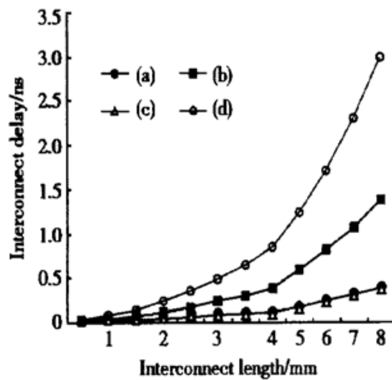

Fig. 3 Interconnects delay & interconnects length at different switch patterns

From foregoing simulation, we know that the role of the coupling capacitance is greatly dependent on the relative switching patterns of the interconnects. So when calculating the interconnect delay, it is not easy to decide how to calculate the crosstalk delay D_{extra}. Some researchers[6] deal with the coupling capacitance in the following ways.

(1) If one net switches and the other remains

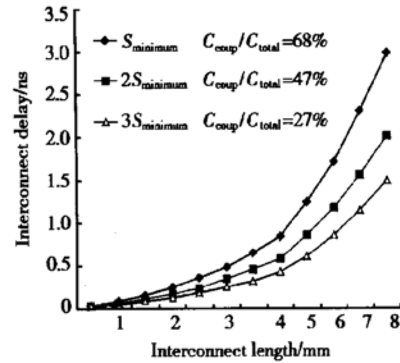

Fig. 4 Delay versus spacing and interconnect length

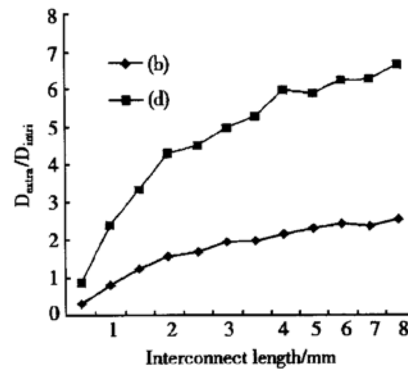

Fig. 5 D_{extra}/D_{intr} change with interconnect length and switching patterns

inactive, then the grounded equivalent coupling capacitance C_{equal} is modeled as C_{coup}.

(2) If the two nets switch at the same time in the opposite directions, then the C_{equal} is modeled as $2C_{coup}$.

(3) If both nets switch at the same time in the same direction, then the C_{equal} is modeled as 0.

Our simulation is consistent with arithmetic (3), if the switching interconnects have the same situation such as the same supply voltage, the same switch direction, and the same interconnect size. If these situations change, the results will be different. The other two are not consistent with our simulations, as shown in Fig. 6. It implies that it is not accurate to calculate the interconnect delay using equivalent coupling capacitance C_{equal}. From our simulations, we learn that coupling capacitance crosstalk delay is relative with the interconnect length, switch patterns, and spacing. Of course, it is sensitive to some other factors too: interconnect width, driver strength, shielding, and so on.

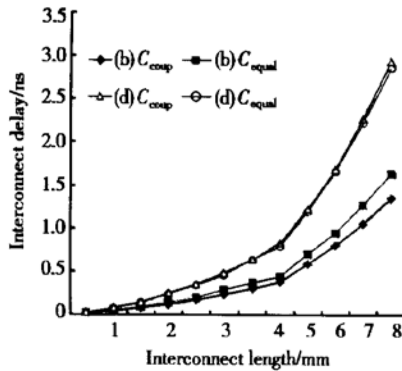

Fig. 6　Interconnect delay versus interconnect length

Coupling capacitance not only impacts on interconnect delay, but also on interconnect noise. The V_{DD} we use to simulate is 1.8V, the peak noises at different interconnect length, spacing, and switching patterns are shown in Figs. 7 and 8. The results imply that the situation (e) is

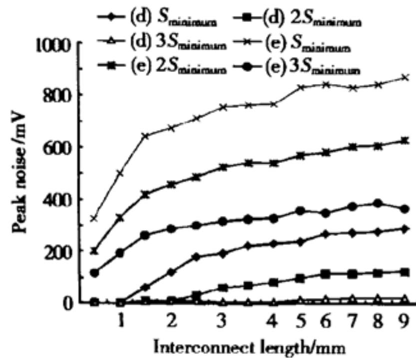

Fig. 7　Peak noise with interconnect length versus interconnect spacing and switching patterns

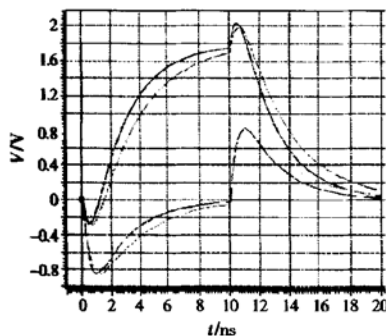

Fig. 8　Signal influenced by capacitive crosstalk

the worst case; in this case, the voltage spike is large enough to cause logic faults on sequential elements. So the crosstalk noise must be taken into consideration in the circuit design in 0.18μm technology.

3　Conclusions

Several measurements are performed for the various test patterns for the analysis of signal integrity problems in 0.18μm technology. We analyze the crosstalk delay and crosstalk noise in different switching patterns from the simulation, we learn in which case the capacitive crosstalk causes the worst crosstalk delay and in which case it causes the worst crosstalk noise. These worst cases must be avoided for the circuit design. We also prove that it is not accurate to calculate the interconnect delay using equivalent coupling capacitance C_{equal}. In a word, the signal integrity problem in 0.18μm technology is serious, in some cases the crosstalk delay can be several times of the interconnect intrinsic delay, and the crosstalk noise can cause logic fault. So how to optimize the interconnect delay and signal integrity is very important in the future technology circuit design.

References

[1] Elmore W C. The transient response of damped linear networks. J Appl Phys, 1948, 19: 55

[2] International Technology Roadmap for Semiconductors 2002 update

[3] Bakoglu H B. Circuits, interconnections, and packaging for VLSI. Addison-Wesley, 1990

[4] Cheng Chungkuan, Lillis J, Lin Shen, et al. Interconnect analysis and synthesis. John Wiley&Sons, 2000

[5] Nourani M, Attarha A. Built-in self-test for signal integrity. In: Proc Design Automation Conf, (DAC' 01), 2001: 792

[6] Sapatnekar S S. A timing model incorporating the effect of crosstalk on delay and its application to optimal channel routing. IEEE Trans Comput-Aided Des Integr Circuits Syst, 2000, 19(5): 550

0.18μm CMOS 工艺条件下的信号完整性分析

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摘要：通过模拟分析了 0.18μm CMOS 工艺条件下的信号完整性问题. 在进行串扰延迟和噪声分析中发现了一些规律, 这些规律对以后的设计有一定的指导意义.

关键词：互连线延迟；信号完整性；串扰；噪声

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