

# Improving Characteristics of Integrated Switched-Capacitor DC-DC Converter by CMOS Technology\*

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**Abstract:** An integrated 3.3V/1.2V SC DC-DC converter operating under 10MHz with a fixed duty ratio of 0.5 is presented. To improve the output current of the converter, CMOS technology is adopted to fabricate the switching devices, and mutually compensatory circuitry technology is also employed to double the output current furthermore. The simulation results using Hspice simulation software, show that the output currents of a single unit circuit and two unit circuits connected in a mutually compensatory manner of the improved converter is about 12.5mA and 26mA, respectively. The power conversion efficiency of the mutually compensatory circuit can amount to 73%, while its output voltage ripple is less than 1.5%. The converter is fabricated in standard Rohm 0.35 $\mu$ m CMOS technology in Tokyo University of Japan. The test result indicates that the output current of 9.8mA can be obtained from a single unit circuit of the improved converter.

**Key words:** DC-DC converter; CMOS technology; monolithic integration

**PACC:** 7420; 0660E

**CLC number:** TN401

**Document code:** A

**Article ID:** 0253-4177(2003)12-1239-05

## 1 Introduction

As a big progress has been made on downsizing the feature dimension of CMOS technology, the system on a package (SOP) technology has attracted much attentions and interests of electrical and electronic engineers who are concerned with the increasing demands for compact and portable electronic equipments. The size and weight reduction on various electronic devices leads to gradual trend towards research on integrated switch-mode DC-DC converters using inductors, transformers or capacitors as energy-storage elements<sup>[1-3]</sup>. Inductors and transformers being inductive elements are hard to be made on a die, so the integrated switched-capacitor (SC) DC-DC converter is a promising candidate for the power supplies with high density of power in SOP. What's more, diodes and large ca-

pacitors usually exist in the existing SC DC-DC converters, which make it difficult to realize the manufacture of these converters in the mature CMOS technology process.

Therefore, an approach is discussed in this paper to enhance the output current of the integrated SC DC-DC converters by employing CMOS technology and mutually compensatory circuit structure. Considering that the typical standard I/O voltage is 3.3V or 3.0V and the core voltage of some CPU and memories is 1.3V or 1.2V when ICs are scaled to the deep sub micron dimensions<sup>[4,5]</sup>, a 3.3V/1.2V SC DC-DC converter has been chosen as a demonstrative sample in this work.

In our earlier work, a monolithically integrated 12V/5V SC DC-DC converter with 10MHz operation frequency and duty ratio of 0.5 was fabricated<sup>[6]</sup>, in which NMOS and PMOS were used as the

\* Project supported by National Natural Science Foundation of China (No. 50177027)

switches. The simulation result of its output current was only about 1mA since NMOS and PMOS had a larger on-state resistance.

In this work, CMOS switches instead of NMOS and PMOS are used and the main circuit of the SC DC-DC converter is improved by combination of two mutually compensatory unit circuits in parallel. It has been shown by simulation results that the output current of the new converter can be increased by at least one order of magnitude although the duty ratio and the operation frequency are still 0.5 and 10MHz, respectively.

## 2 Circuit operation and simulation analyses

The unit circuit of the demonstrative SC DC-DC converter is schematically shown in Fig. 1 where some important component parameters are also marked.

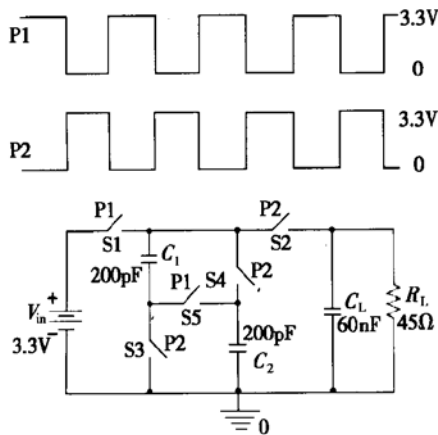


Fig. 1 Unit circuit of the SC DC-DC converter

In Fig. 1, P1 and P2 represent the controlling pulses of these five switches illustrated in this figure, and the on or off state of these switches corresponds to the high or low voltage level, respectively.

The output current ( $I_{out}$ ) of the demonstrative conversion circuit can be defined as<sup>[7]</sup>

$$I_{out} = AfC \left( \frac{1}{2} V_s - V_L - \frac{3}{2} V_d \right) \frac{(1 - e^{-\frac{1}{2frc}})}{(1 + e^{-\frac{1}{2frc}})} \quad (1)$$

where  $V_s$  is the value of the input voltage  $V_{in}$ ,  $V_L$  is the output voltage,  $V_d$  is the voltage drop across each of the switches S3, S4, and S5 in on-state, which have the same value,  $r$  is the equivalent resistance of the circuit,  $f$  is the operation frequency and  $C$  equals to a half of the capacitance of  $C_1$  or  $C_2$ , which have the same value in this circuit. According to the theory of resistance modulation (RM)<sup>[7]</sup>,  $I_{out}$  can be enhanced by decreasing the equivalent resistance  $r$  when  $f$  and  $C$  are all fixed at a constant. As the on-state resistance of CMOS switches is usually small and less affected by the voltage between the source and the drain, using CMOS as switches S1 and S2 in the converter must result in a remarkable improvement of its output characteristics.

In comparison, Figure 2 describes the plots of the simulation results of the output current versus time for different types of switching devices adopted in Fig. 2.

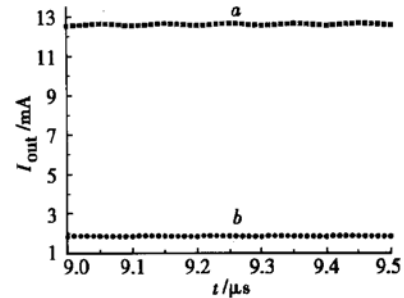


Fig. 2 Plots of the output current versus time for the SC DC-DC converters using different switching devices

In Fig. 2, curve *a* represents the  $I_{out}$  performance of the improved converter using CMOS switching devices as S1 and S2, while curve *b* represents the  $I_{out}$  characteristics of the circuit taking PMOS and NMOS switches as S1 and S2, respectively.

It can be seen from Fig. 2 that  $I_{out}$  of the converter using CMOS switches is about 12.5mA, which is almost one order higher than that of the converter using PMOS and NMOS switches.

In addition to adopting CMOS switches, the

conversion circuit structure can be improved by combining the two unit circuits in a parallel mutually compensatory manner to boost up the output current more efficiently, as shown in Fig. 3. Advantages of the mutually compensatory conversion circuit can be understood in the following. In the unit circuit shown in Fig. 1,  $C_L$  is only charged in half of a period, while in the new mutually compensatory circuit shown in Fig. 3,  $C_L$  can be charged in a full period. Consequently, the output current can be enhanced.

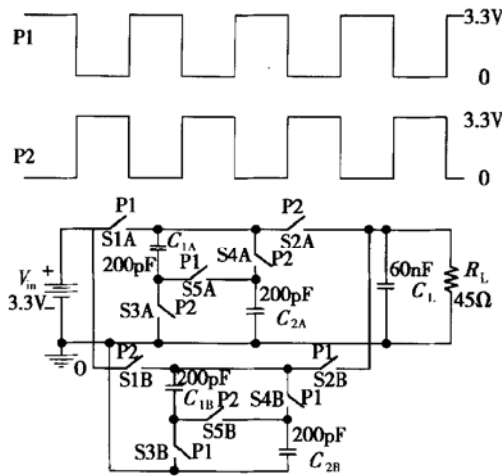


Fig. 3 Mutually compensatory circuit structure of the SC DC-DC converter

As depicted in Fig. 1, controlling pulses P1 and P2 also command these switches in Fig. 3 by means of its high or low voltage level.

From Fig. 3, it can be seen that the mutually compensatory circuit is composed of two absolutely same unit circuits. However, the two units operate always in different states, which are controlled by P1 and P2 applied to the gates of the switching devices. For example, when P1 is in high voltage level while P2 in the opposite state, S1A, S5A, S2B, S3B, and S4B are switched on, and S2A, S3A, S4A, S1B and S5B are switched off. In this state,  $C_{1B}$  and  $C_{2B}$  are charged in series by  $V_{in}$ , while  $C_{1A}$  and  $C_{2A}$  are discharged in parallel through  $C_L$ . Similarly, when P1 and P2 are in different voltage levels, S1A, S5A, S2B, S3B, and S4B are switched off and S1B, S5B, S2A, S3A, and S4A are switched on. Cor-

respondingly,  $C_{1A}$  and  $C_{2A}$  are charged in series by  $V_{in}$ , while  $C_{1B}$  and  $C_{2B}$  are discharged in parallel through  $C_L$ . It means that  $C_L$  can be charged continuously in the whole operation states, thus the output current can be improved furthermore.

The output characteristics of the demonstrative SC DC-DC converter with mutually compensatory circuit structure are simulated for its operation at room temperature. The plots of the output voltage and the output current versus time are simultaneously shown in Fig. 4.

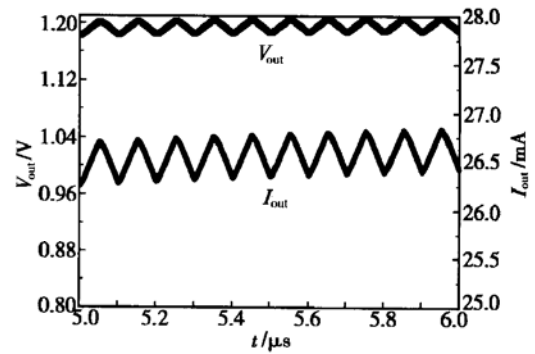


Fig. 4 Plots of  $V_{out}$  and  $I_{out}$  versus time for the mutually compensatory circuit structure

The simulation results indicate that the output current of the SC DC-DC converter with mutually compensatory circuit structure can reach up to about 26mA and the maximum ripple is only 1.5% when the output voltage is stable.

### 3 Experimental results

The demonstrative DC-DC converter was fabricated in a standard Rohm 0.35μm CMOS technology with p-substrate n-well 3-metal 2-polysilicon process in Tokyo University of Japan. The converter delivered about a 1.2V output from a 3.3V input at a 10MHz switching frequency. As far as the converter switched by NMOS and PMOS switching devices is concerned, by using an Ampere meter, the output current amounts to 1.3mA and the characteristic of the  $V_{out}$  of 1.13V are similar to that of a single unit circuit of the converter using CMOS switches.

For a single unit circuit of the converter using CMOS switching devices, the test result of the  $V_{out}$  of 1.16V is displayed in Fig. 5 with the  $I_{out}$  of 9.8mA also tested by an Ampere meter.

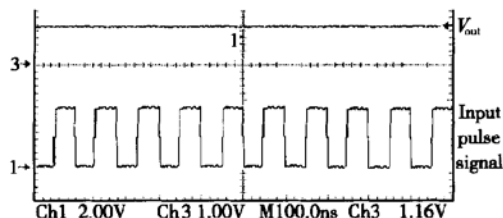


Fig. 5 Experimental result of  $V_{out}$  of a single unit circuit of the converter using CMOS switching devices as S1 and S2

By analyzing the experimental results, it can be concluded that the use of CMOS switches can effectively raise the  $I_{out}$  of a single unit circuit to 9.8mA, which is almost in accordance with the simulation result signified by curve *a* in Fig. 2.

## 4 Conclusion

An integrated SC DC-DC converter has been described, designed, analyzed, and tested. Using CMOS instead of NMOS and PMOS switching devices, the converter demonstrated more suitable characteristics indicating that the  $I_{out}$  of a single unit circuit can come up to 9.8mA with the  $V_{out}$  of 1.16V. Also the simulation results show that double  $I_{out}$  can be obtained by designing the mutually compensatory conversion circuit with a power con-

version efficiency of 73% and an output voltage ripple under 1.5%. In general, as for the demonstrative 3.3V/1.2V SC DC-DC converter, the improvements presented in this paper directly result in the advancement of the output current.

**Acknowledgment** The authors would like to acknowledge Professor Tadashi Shibada and his group at Tokyo University for their kind help in this work.

## References

- [1] Hara N, Oota I, Ueno F. Mathematical analysis of 1/2 step-down switched-capacitor DC-DC converter with low ripple. Elsevier Physica B, 1997, 239: 181
- [2] Stratakos A J, Brodersen R W. A low-voltage CMOS DC-DC converter for a portable battery-operated system. In: Proc IEEE PESC, 1994: 619
- [3] Geng Li, Chen Zhiming, Liu Jian. Design of a hybrid monolithic integrated switched capacitor DC-DC step-up converter. In: Proc IPEMC, 2000, 1: 263
- [4] Hiraki M, Ito T, Fujiwara A, et al. A 63-μW standby power microcontroller with on-chip hybrid regulator scheme. IEEE J of Solid-State Circuits, 2002, 37(5): 605
- [5] Wu J T, Chang Y H, Chang K L. 1.2V CMOS switched-capacitor circuits. In: Proc IEEE International Solid-State Circuits Conference, 1996: 388
- [6] Geng Li, Chen Zhiming, Liu Xianfeng. A monolithically integrated 12V/5V switched capacitor DC-DC converter. Chinese Journal of Semiconductors, 2000, 21(6): 529
- [7] Geng Li. Monolithically integrated switched capacitor DC-DC converters. Thesis for Doctor Degree, Xi'an University of Technology, 2001[耿莉. 单片集成开关电容 DC-DC 变换器. 西安理工大学博士论文, 2001]

## 用 CMOS 工艺改善集成开关电容 DC-DC 变换器的特性\*

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**摘要:** 介绍了一种具有改进电路结构和改进工艺的单片集成 3.3V/1.2V 开关电容 DC-DC 变换器, 其控制脉冲频率和固定导通比分别为 10MHz 和 0.5. 为了提高变换器的输出电流, 采用 CMOS 工艺来制造电路中的开关器件和改进的互补型电路结构. 使用 Hspice 电路仿真软件得到的仿真结果表明改进变换器的单个单元电路和互补型电路可使输出电流分别达到 12.5mA 和 26mA, 且后者的功率转换效率为 73%, 输出电压纹波小于 1.5%. 变换器在日本东京大学的标准 Rohm 0.35 $\mu$ m CMOS 工艺线上投片试制, 测试结果显示, 使用 CMOS 开关的变换器单元电路的输出电流为 9.8mA.

**关键词:** DC-DC 变换器; CMOS 工艺; 单片集成

**PACC:** 7420; 0660E

**中图分类号:** TN401

**文献标识码:** A

**文章编号:** 0253-4177(2003)12-1239-05

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\* 国家自然科学基金资助项目(批准号: 50177027)

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2003-05-09 收到, 2003-06-26 定稿

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