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A 900MHz CMOS PLL/Frequency Synthesizer Initialization Circuit*

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Abstract: A 900MHz CMOS PLL/frequency synthesizer using current-adjustable charge-pump circuit and on-chip loop filter with initialization circuit is presented. The charge-pump current is insensitive to the changes of temperature and power supply. The value of the charge-pump current can be changed by switches, which are controlled by external signals. Thus the performance of the PLL, such as loop bandwidth, can be changed with the change of the charge-pump current. The loop filter initialization circuit can speed up the PLL when the power is on. A multi-modulus prescaler is used to fulfill the frequency synthesis. The circuit is designed using 0.18μm, 1.8V, 1P6M standard digital CMOS process.

Key words: PLL; charge-pump; loop filter; multi-modulus prescaler
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1 Introduction

Phase-locked loops (PLLs) are widely used in communication applications. They can recover clock from received data signals, perform frequency and phase modulation/demodulation, and frequency synthesis. Nowadays, especially in wireless communication systems, frequency synthesizers mainly take the PLL-based structure, and charge-pump PLL[1] (CPPLL) is the most popular architecture.

In this work, we present a PLL/frequency synthesizer circuit whose charge-pump current can be adjusted, and the output pump current is insensitive to the changes of power supply and temperature; also in the on-chip filter, an initialization circuit is added in to speed up the PLL when power is on.

2 Charge-pump PLL

A charge-pump PLL[1] consists of several major blocks including a phase-frequency detector, a charge-pump and a loop filter, a voltage-controlled oscillator, and a prescaler, which is optional, in the feedback loop.

Within a limited ranges, a PLL can be modeled as a linear transfer function. Figure 1 shows a generic linear model of a PLL[2,3].

In above model, the VCO acts as an ideal inte-

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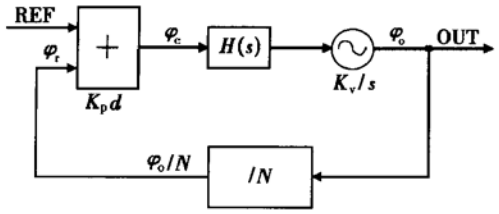

Fig. 1　A generic linear model for PLL

grator of phase and the output phase can expressed as

$$\phi_o(t) = \omega_c(t) + \int_0^t K_v K_c(t)\,dt + \phi_o(0), t \geqslant 0 \quad (1)$$

where ω_c represents the nominal VCO frequency in radians per second, and K_v represents the VCO gain in radians per second per volt. The phase detector output is given by

$$V_d = K_{pd} f(\phi_e) \quad (2)$$

where

$$\phi_e = \phi_r - \phi_o/N \quad (3)$$

which is the loop phase error, and N is the feedback divider ratio.

As for a charge-pump PLL, the output current of the charge-pump can be expressed as[1,4]

$$i_p = I_p \mathrm{sgn}(\tau) \quad (4)$$

where I_p is the reference current of the charge-pump, τ is the time interval of UP/DOWN signals, whose value is determined by ϕ_e, and sgn(•) is the sign function.

Then the PFD gain K_{pd} is proportional to the charge-pump output current and the time interval of the UP/DOWN signals and can be expressed as

$$K_{pd} = V_d/f(\phi_e) = i_p Z(s)/f(\phi_e) \quad (5)$$

where $Z(s)$ is the load looking at the output of the charge pump circuit. Then the control voltage of the VCO is given by

$$V_c = V_d H(s) = i_p Z(s) H(s) = i_p H'(s) \quad (6)$$

where $H(s)$ represents the transfer function of the loop filter.

From Fig. 1, we can write the closed loop transfer function as

$$H_L(s) = \frac{\phi_o}{\phi_r} = \frac{K_{pd} H(s) K_v/s}{1 + \frac{1}{N} K_{pd} H(s) K_v/s} \quad (7)$$

Taking the absolute value of the open loop gain $H_o(s) = K_{pd} H(s) K_v/(Ns)$ with $s = j\omega$, one can find out what the bandwidth of the system ω_b is when $|H_o(j\omega)|$ equals to 1. The result is that the bandwidth of the system is proportional to the charge pump output current. And the settling time approximates to $-\ln\epsilon/\omega_b$[5], where ϵ represents the settling accuracy. Thus, if the charge-pump current can be changed during operation, then the performances of the PLL can be changed also.

3　CPPLL circuit design

As mentioned in section 2, the charge-pump current is a key factor influencing the performances of the CPPLL such as the bandwidth, the tracking speed, and the noise performances of the PLL.

The architecture of the designed charge-pump PLL circuit is shown in Fig. 2.

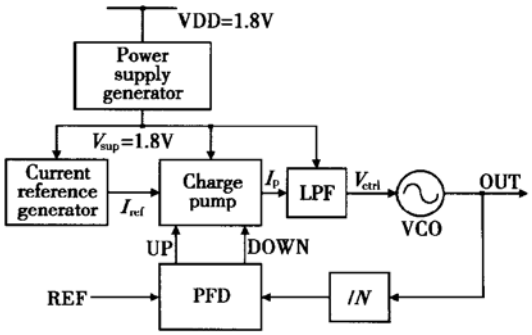

Fig. 2　Block diagram of the designed CPPLL

3.1　Power supply generator

Because the charge-pump current is a key parameter in the design of PLLs or frequency synthesizers, it should be insensitive not only to the changes of power supply and temperature, but also to the power supply noise. The power supply generator is used here to generate a supply voltage with 1.8V for analog part[6].

3.2　Charge-pump circuit

The charge-pump circuit consists of a current reference circuit and a current output circuit[6]. The design in Ref. [6] is shown in Fig. 3(a), the current generated by current reference circuit is mir-

rored to the current output circuit and sources current to or sinks current from the loop filter according to the signals UP and DOWN. The current mirrored to the current output circuit can be adjusted through the branches MN2, MN3, and MN4 controlled by switches. The switch under MN1 is always on in order to match the other switches.

But there is a drawback in the above structure, that is whether MN2, MN3 and/or MN4 sink current or not, the total current draw from the power supply through MP1 is fixed with the maximum value. Thus some extra power is dissipated when switches S2, S3, or S4 are on.

The improved structure is shown in Fig. 3(b). When switches S2, S3, and S4 are off, there is no more extra current drawn from power supply, and then no more power is dissipated.

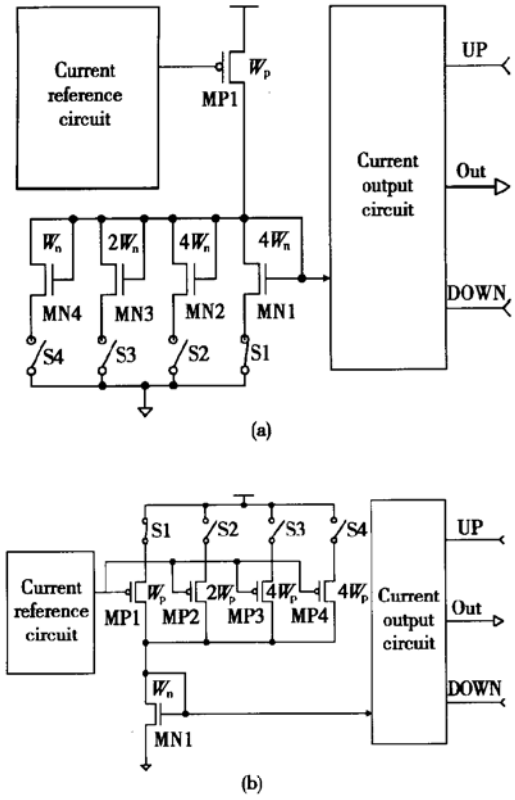

Fig. 3 Charge pump circuit structure (a) Charge pump circuit structure in Ref. [6]; (b) Improved charge pump circuit structure

3.3 Loop filter with initialization circuit

When the power is off, the output control voltage of the loop filter is zero. If a down signal of PFD is first generated after the power on, the output control voltage of the loop filter should decrease, but the voltage value cannot go down below zero. So an initialization circuit is added to the loop filter (see Fig. 4). A Schmitt flip-flop with two threshold voltages of 0.5V and 0.95V is used to sense the control voltage on the loop filter. When the power on, a pulse signal RESET is generated, INIT signal is active, loop filter is initialized by MN1, MN2, and MP1. When the control voltage reaches 0.95V (about half of the power supply), Schmitt flip-flop toggles, then the output of Schmitt flip-flop disables the initialization operation even though RESET is high. This configuration can speed up the PLL system.

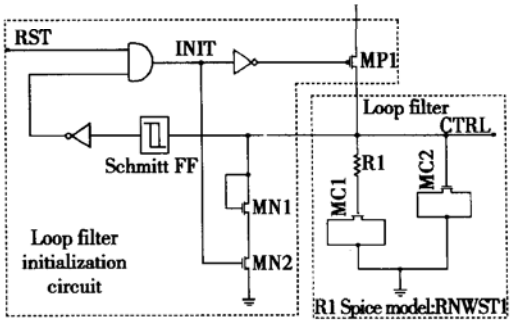

Fig. 4 Loop filter with initialization circuit

3.4 Multi-modulus prescaler

To achieve high-speed and low-power design, it is desirable to minimize the amount of circuitry operating at high frequency. Based on traditional dual-modulus prescaler[7~9], a multi-modulus prescaler is designed as shown in Fig. 5(a), which consists of a synchronous divide-by-2/3 counter as the first stage, an asynchronous divide-by-32 counter as the second stage, and a controlled logic stage.

The operation of the controlled logic is explained as follow. When D_3~ D_0 are zeros and then MC is one, the first stage does divide-by-2 only, and the total division ratio is 64. The signal Y_i is determined by the outputs of F3, F4, F5, and F6 (the timing diagram is shown in Fig. 5(b)). The

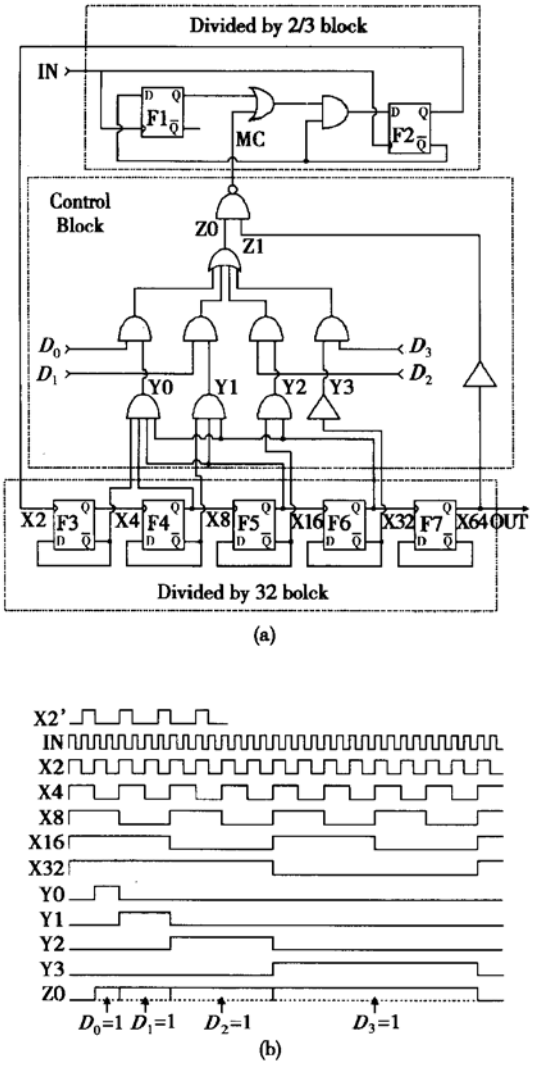

Fig. 5　Multi-modulus prescaler　(a) Multi-modulus prescaler block diagram; (b) Timing diagram of the prescaler

signal Y_i generates a signal pulse with 2^i-clock cycle in 16 clock cycles of X2, which is the output of the first division stage, and is non-overlapped each other. Z_0 is the combined cycle of n clocks according to D_i, where $n = D_3 \times 2^3 + D_2 \times 2^2 + D_1 \times 2 + D_0$. Combined with the signal Z_1, which is one-fourth of 32-clock cycle of X2, MC generates a zero signal pulse of n clocks in this 32-clock cycle and a single clock period of IN is swallowed. This makes the first stage as a divide-by-3 divider (see X2′ in Fig. 5(b)), thus the prescaler functions as a divide-by-(64+ n) divider. Afterward the divide-by-2 action is resumed. Therefore, the prescaler's division ratio is given by

$$N = 64 + D_3 \times 2^3 + D_2 \times 2^2 + D_1 \times 2^1 + D_0 \times 2^0 \quad (8)$$

3.5　Other circuits of the CPPLL

The VCO is a ring oscillator, which is made up of a four-stage cross-coupled differential delay cells, buffers, and D2S (differential to single) circuit. The PFD used in this work takes the form described in Ref. [10].

4　Experimental results

The whole charge-pump PLL circuit was designed using SMIC 0.18μm 1.8V standard digital CMOS process. The circuit was simulated using typical, fast, and slow models. The simulation tool is Hspice.

The power supply generator was simulated with the temperature swept from 0℃ to 100℃, and the power supply voltage swept from 1.44V to 2.16V (20% changes in VDD) during simulation. The output voltage is about 1.8V and changes little[6].

The current of the charge-pump reference circuit was simulated swept from 0℃ to 100℃ with switches on or off, the output current can be changed from 7.5μA to 82μA, and the temperature coefficient of the output current at 25℃ is about + 0.02% change/℃ or + 200ppm/℃.

The VCO can be tuned from 800MHz to 980MHz, the control voltage is from 0.75V to 1.45V.

Then, the whole PLL is simulated. The output control voltage of the loop filter is shown in Fig. 6. There are two results for charge pump current with the value of 82μA, one is for 827MHz output frequency and the other is for 961MHz output frequency of the VCO. Also shown in the figure is another analysis with the charge pump current value of 47μA. The FFT analysis is shown in Fig. 7.

According to the analysis in section 2, the bandwidth of the PLL system is one of the most

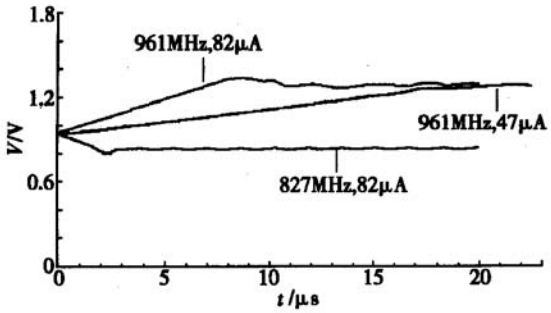

Fig. 6 Transient analysis of the control voltage for VCO of PLL

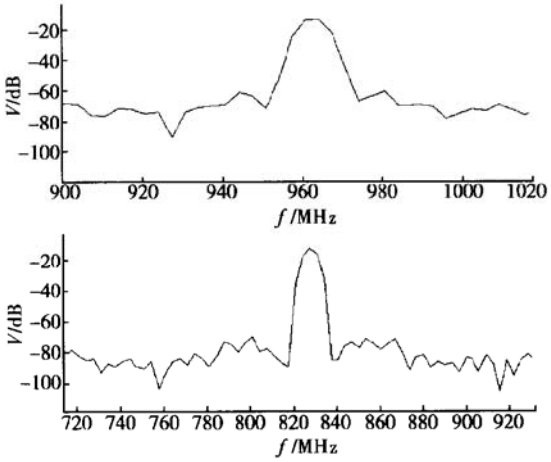

Fig. 7 FFT analysis of the PLL

important performance and its value is proportional to the charge-pump current, and the transient characteristics of the PLL such as settling time is a function of the bandwidth, that is with the larger bandwidth, the settling time is shorter. From the simulation result, it can be seen that the design verifies the analysis in section 2, and the design idea using the current-adjustable charge-pump circuit to change the performance of the PLL is applicable.

Figure 8 shows the chip photo of the designed PLL.

5 Conclusion

In this work, a 900MHz charge-pump PLL with adjustable pump current and on-chip loop filter is presented. The output reference pump current is designed to be insensitive to the changes of the temperature. A power supply generator is used to generate the supply voltage for the analog circuits; this generated voltage is insensitive to the changes of the temperature and power supply. And thus the output pump current of the charge-pump circuit is also insensitive to the changes of power supply. An initialization circuit is added to the on-chip loop filter to speed up the PLL when power is on. The whole circuit was designed using 0.18μm 1.8V standard digital CMOS process, and the simulation results show that the performance of the circuit is satisfied.

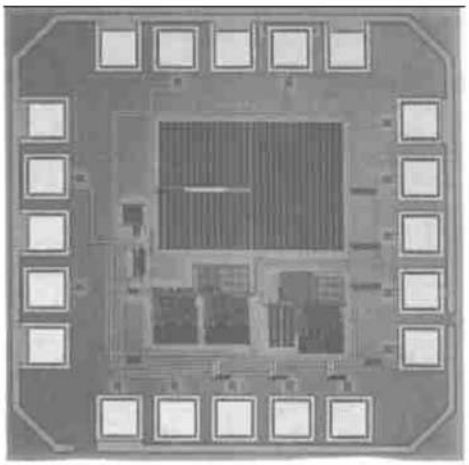

Fig. 8 Chip photo of the designed PLL

References

[1] Gardner F M. Charge-pump phase-lock loops. IEEE Trans Commun, 1980, 28(11): 1849

[2] Wolaver D H. Phase-locked loop circuit design. Prentice-Hall, Inc, 1991

[3] Crawford J A. Frequency synthesizer design handbook. Artech House, Inc, 1994

[4] Van Paemel M. Analysis of a charge-pump PLL: a new model. IEEE Trans Commun, 1994, 42(7): 2490

[5] Craninckx J, Steyaert M S J. Wireless CMOS frequency synthesizer design. Kluwer Academic Publishers, 1998

[6] Zhao Hui, Xu Donglin, Pan Sha, et al. The design of a CMOS current-adjustable charge-pump circuit insensitive to power supply and temperature. Chinese Journal of Semiconductors, 2003, 24(3): 260

[7] Foroudi N, Kwasniewski T A. CMOS high-speed dual-modulus frequency divider for RF frequency synthesis. IEEE J Solid-State Circuits, 1995, 30(2): 93

[8] Larsson P. High-speed architecture for a programmable frequency divider and a dual-modulus prescaler. IEEE J Solid-State Circuits, 1996, 31(5): 744

[9] Craninckx J, Steyaert M. A 1.75GHz/3V dual-modulus divide-by-128/129 prescaler in 0.7μm CMOS. IEEE J Solid-State Circuits, 1996, 31(7): 890

[10] Von Kaenel V, Aebischer D, Piguet C, et al. A 320MHz, 1.5mW@1.35V CMOS PLL for microprocessor clock generation. IEEE J Solid-State Circuits, 1996, 31(11): 1715

900MHz CMOS 锁相环/频率综合器*

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摘要: 给出了一个 900MHz CMOS 锁相环/频率综合器的设计, 设计中采用了电流可变电荷泵及具有初始化电路的环路滤波器. 电荷泵电流对温度与电源电压变化的影响不敏感, 同时电流的大小可通过外部控制信号进行切换控制而改变. 因此, 锁相环的特性, 诸如环路带宽等, 也可通过电流的改变而改变. 采用具有初始化电路的环路滤波器可提高锁相环的启动速度. 另外采用了多模频率除法器以实现频率合成的功能. 该电路采用 0.18μm、1.8V、1P6M 标准数字 CMOS 工艺实现.

关键词: 锁相环; 电荷泵; 滤波器; 多模频率除法器

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