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5Gb/s 0.25 m CMOS Limiting Amplifier*

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Abstract: A limiting amplifier (LA) IC implemented in TSMC standard 0.25μm CMOS technology is described. Active inductor loads and direct-coupled technology are employed to increase the gain, broaden the bandwidth, reduce the power dissipation, and keep a tolerable noise performance. Under a 3.3V supply voltage, the LA core achieves a gain of 50-dB with a power consumption below 40mW. The measured input sensitivity of the amplifier is better than 5mV_{pp}. It can operate at bit rates up to 7Gb/s with an rms jitter of 0.03 UI or less. The chip area is only 0.70mm × 0.70mm. According to the measurement results, this IC is expected to work at the standard bit rate levels of 2.5, 3.125, and 5Gb/s.

Key words: limiting amplifier; active inductor; shunt peaking technique; CMOS
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1 Introduction

Wide-band, high-speed limiting amplifiers (LAs) are widely used in fiber-optical communications, space communications, and radar systems. In fiber-optical links, a LA has several possible applications such as the main amplifier of an optical receiver, the input and output buffer for data and clock signal reforming. The design of a high-speed LA with a high gain and a wide dynamic range is therefore an essential task for the realization of high-speed data systems[1].

Most ICs operating at Gb/s data rates used to be realized in GaAs and Si bipolar technologies with higher DC power and cost. As the feature size gradually scaled down, deep submicron CMOS technologies can be used to realize high-performance and high-speed ICs. In this work, the TSMC 0.25μm CMOS technology was used to design a LA for the use of SDH/SONET systems.

In the past, much work has been done to improve the performance of CMOS LAs. Compared with the preceding works[2~4], the CMOS LA presented in this paper achieves higher bit rates and consumes a lower DC power. The structure examined in this paper introduces active inductor loads that make it possible for the LA to get large gain-bandwidth product and employs direct-coupled gain stages without source followers that reduce the power consumption nearly 50 percent. In following sections, the circuit architecture will be analyzed in detail, the fabrication aspects will be given briefly and the measurement results will be dis-

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cussed.

2 Circuit design

As shown in Fig. 1, the fully differential circuit consists of an input buffer for 50Ω impedance match and level-shifting. The LA core includes several similar cascaded gain stages. An output buffer is used for driving 50Ω transmission lines. A pair of networks of total feedback is inserted for DC offset canceling.

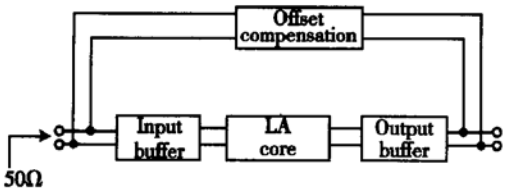

Fig. 1 Block diagram of the limiting amplifier

Direct-coupled gain stages are utilized to achieve high gain and low power. As illustrated in Fig. 2, the typical gain stage with NMOS loads is difficult to operate at high bit rates due to its large load capacitance.

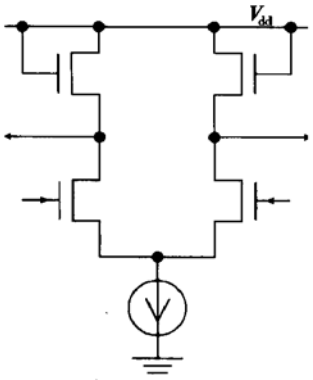

Fig. 2 Conventional gain stage schematic

An effective way to increase the gain-bandwidth product is to introduce an inductive component into the loads of the NMOS differential pairs, which is known as the shunt peaking technique. By partly tuning out the capacitive loading, the pole of each stage can be moved to a higher frequency. With suitable choice of inductors, both a maximal flat response and a substantial bandwidth extension can be obtained simultaneously.

An inductive load can be implemented with a spiral inductor or an active inductor (see Fig. 3). It is difficult to design a spiral inductor with high inductance but keeping the self-resonance outside the pass-band. Furthermore, a spiral inductor is not compact. In contrast, an active inductor is able to work at higher frequencies with an acceptable chip-area. For the application in a broadband amplifier, a high Q-factor is not necessary. The schematic of each gain stage with active inductor loads is illustrated in Fig. 3. The small-signal model of an active inductor is shown in Fig. 4 (a).

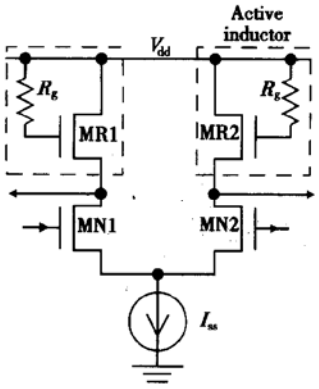

Fig. 3 Gain stage with active inductors

To simplify the calculation, C_{gd}, C_{ds}, g_{ds} can be neglected under the conditions of $C_{gs} \gg C_{gd}$, $C_{gs} \gg C_{ds}$, and $g_m \gg g_{ds}$. The simplified model is illustrated in Fig. 4(b).

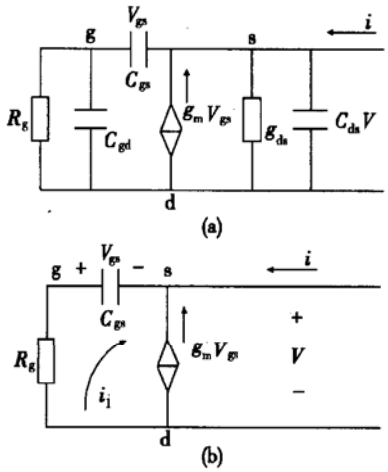

Fig. 4 (a) Small-signal model of an active inductor; (b) Simplified small-signal model of an active inductor

Therefore, the equivalent impedance of an active inductor can be written as

$$Z_{in} = \frac{1 + R_g s C_{gs}}{g_m + s C_{gs}} \tag{1}$$

Thus, the equivalent inductance L and serial resistance R are obtained as

$$L = \frac{\frac{R_g}{\omega_T} - \frac{1}{g_m \omega_T}}{1 + (\frac{\omega}{\omega_T})^2} \tag{2}$$

$$R = \frac{\frac{1}{g_m} + R_g(\frac{\omega}{\omega_T})^2}{1 + (\frac{\omega}{\omega_T})^2} \tag{3}$$

where ω_T is the unity current-gain angular frequency. To stabilize the operation of the LA, the DC operating points of each stage are often kept unchanged for both input and output, and they are determined by g_m of NMOS load with fixed current source I_{ss}. As a result, the adjustment of an active inductor is mainly realized by altering the value of R_g. Equation (2) suggests that the equivalent inductance increases with the resistance R_g. But this increase is restricted. To avoid undesirable peaking in the frequency response, the optimum inductance should be

$$L_{opt} = \frac{1}{1 + \sqrt{2}} R^2 C \tag{4}$$

where the equivalent serial resistor $R \approx 1/g_m$ if $\omega \ll \omega_T$. In this case, the bandwidth of the stage is about 1.72 times as large as that of the same stage without peaking. If the optimum value is exceeded much more, a "phase distortion" will occur, which is responsible for the bit errors. In addition, the self-resonance frequency will decrease, which constrains the working speed of the LA. Hence, the resistance R_g should be chosen carefully according to the capacitive loads of each gain stage and trans-conductance of NMOS loads.

The DC gain of each stage with active inductors is primarily determined by the geometrical ratio of two NMOS transistors: MN1 and MR1 or MN2 and MR2 in Fig. 3, namely,

$$A_{dc} = \frac{g_{MN1}}{g_{MR1}} = \sqrt{\frac{W_{MN1}}{W_{MR1}}} \tag{5}$$

for $L_{MN1} = L_{MR1}$. The DC gain is insensitive to process, temperature, and bias. Figure 5 shows the equivalent inductance of active inductors in this design. The self-resonance frequency is around 9GHz, much higher than bandwidth required, and the equivalent inductance is over 10nH from low frequency to 5GHz, which ensures the working speed of the LA up to 5Gb/s.

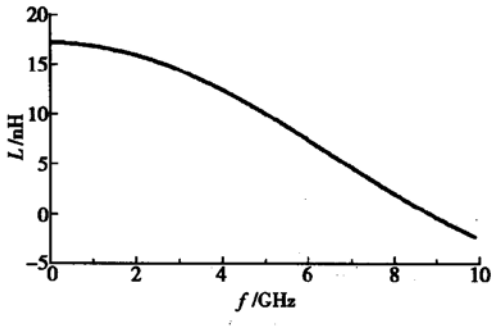

Fig. 5 Equivalent inductance of an active inductor

3 Fabrication aspects

The limiting amplifier was realized in TSMC 0.25μm CMOS technology through the MOSIS program of the University of South California, USA. The chip microphotograph is shown in Fig. 6. The chip area is only 0.70mm×0.70mm.

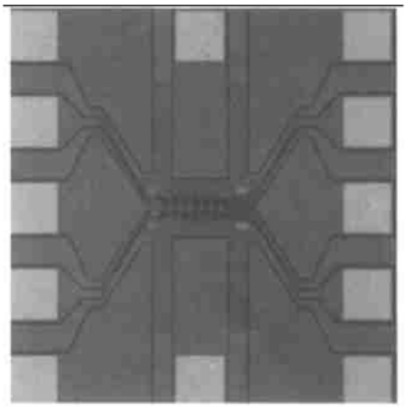

Fig. 6 Chip photograph of the LA

4 Measurement results

The performance of the IC was evaluated via on-wafer probes, using differential input voltage signals at various bit rates. Figures 7 (a), (b) and

Figs. 8 (a) and (b) show the eye-diagrams of one single-ended output of the LA measured at the bit rates of 2.5Gb/s, 5Gb/s with input signals of 5mV_{pp} and 500mV_{pp}, respectively. The output voltage swing is limited at 400mV_{pp}. Figure 9 shows the eye-diagram at 7 Gb/s. Very little intersymbol interference is present in the eyes and the measured rms jitter is 0.03 UI or less (unit interval), consistent with *s*-parameter analysis of the active inductor.

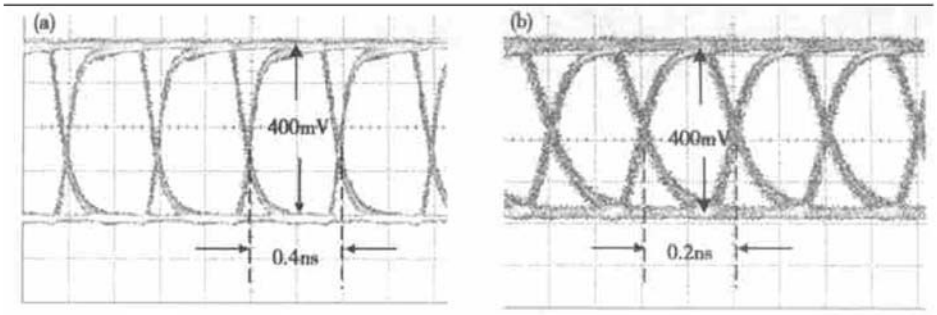

Fig. 7　Eye-diagrams of single-end output at 5mV_{pp} input at 2.5Gb/s (a) and 5 Gb/s (b)

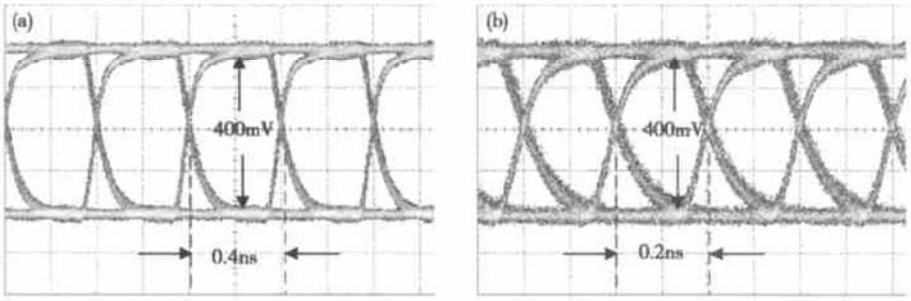

Fig. 8　Eye-diagrams of single-end output at 500mV_{pp} input at bit rates of 2.5Gb/s (a) and 5Gb/s (b)

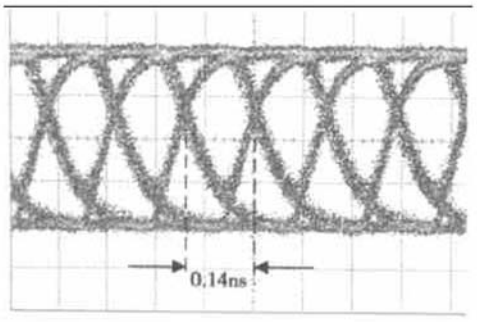

Fig. 9　Eye-diagram of single-end output at 7Gb/s

The DC current under the 3.3V supply is 28mA. The current needed for the LA core without the buffers is only 12mA, corresponding to a power consumption of less than 40mW, significantly lower than that of commercially available stand-alone LAs (165~ 500mW). Based on the measurement results above, this LA with active inductor loads can operate well at the standard bit rates of 2.5, 3.125, and 5Gb/s.

5 Conclusion

A limiting amplifier has been realized in a standard 3.3V 0.25μm CMOS technology of TSMC. Directed-coupled gain stages and active inductor loads have been used to broaden the bandwidth, reduce the power consumption, and enhance the process and temperature insensitivity of the gain. The IC has an input dynamic range of 40dB, a differential output voltage of 800mV_{pp} across a 50Ω load, a power consumption of ~ 40mW, and a time jitter of ≤0.03UI. These results meet the specifications of STS-48/STM-16 at 2.5Gb/s and STS-96 systems at 5Gb/s.

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5Gb/s 0.25 m CMOS 限幅放大器*

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摘要: 采用 TSMC 0.25μm CMOS 技术设计实现了高速低功耗光纤通信用限幅放大器. 该放大器采用有源电感负载技术和放大器直接耦合技术以提高增益, 拓展带宽, 降低功耗并保持了良好的噪声性能. 电路采用 3.3V 单电源供电, 电路增益可达 50dB, 输入动态范围小于 $5mV_{pp}$, 最高工作速率可达 7Gb/s, 均方根抖动小于 0.03UI. 此外核心电路功耗小于 40mW, 芯片面积仅为 0.70mm×0.70mm. 可满足 2.5, 3.125 和 5Gb/s 三个速率级的光纤通信系统的要求.

关键词: 限幅放大器; 有源电感; 并联峰化技术; CMOS

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