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Influence of Device Narrowing on HALO-pMOSFETs' Degradation Under $V_g = V_d/2$ Stress Mode*

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Abstract: The degradation characteristics of both wide and narrow devices under $V_g = V_d/2$ stress mode is investigated. The width-enhanced device degradation can be seen with devices narrowing. The main degradation mechanism is interface state generation for pMOSFETs with different channel width. The cause of the width-enhanced device degradation is attributed to the combination of width-enhanced threshold voltage and series resistance.

Key words: width-enhanced degradation; pinch-off voltage; current-crowding effect
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1 Introduction

Hot carrier degradation has been recognized as a major reliability and performance concern in today's submicron complementary metal oxide semiconductor (CMOS) field effect transistor (FET) technology. As the CMOS technology was introduced into the areas of submicron and deep-submicron, the degradation caused by the pMOSFETs has become comparable with that of the nMOSFETs. It is then very important to investigate the behavior and underlying physics of pMOSFETs hot carrier degradation mechanism. Most of the effects of hot-carrier-induced degradation have concentrated on the channel length dependency on hot-carrier degradation using devices with channel widths greater than 10μm[1~3]. As MOSFETs dimensions shrink, the channel width effect plays an increasingly important role in hot-carrier degradation, particularly in multi-megabit devices where the device width is less than 1μm. Previous studies[4~6] based on devices fabricated with the conventional LOCOS have reported that narrow channel devices exhibited enhanced hot-carrier degradation compared to the wide channel devices. This is attributed to the reported different degradation mechanism in the two types of devices, as the wide channel devices degrade via interface state generation, while the narrow devices degrade via charge trapping in the gate oxide due to the high mechanical stress[1,3]. As the gate width is shrinking towards the 0.25μm generation and beyond, shallow-trench-isolation (STI) has evolved as the mainstream in the present deep-submicron ULSI devices. From the experimental measurements, it was

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observed that the degradation in narrow p-MOSFETs is resulting from the mechanical stress, which is responsible for the enhanced electron trapping efficiency[3].

In this paper, we compare the degradation behavior of both wide (W_{mask} = 10μm) and narrow (W_{mask} = 0.3 and 0.19μm) devices under $V_g = V_d/2$ stress mode, and investigate the cause for the difference in the degradation behavior. Finally, the cause for the width-enhanced degradation is discussed.

2 Results and discussions

The results of the stress on pMOFETs with different channel width show that narrow devices exhibit larger degree of hot-carrier degradation compared to wide devices having the same channel length, at the same stress voltage and $V_g = V_d/2$ stress mode. HALO structure is introduced to improve the short channel effect and threshold voltage. The devices used in this study were fabricated using 0.13μm CMOS technology with shallow-trench-isolation (STI) structure. The gate oxide thickness is 2.5nm and the device has HALO structure. Saturation drain currents (I_{dsat}) of fresh and stressed devices are used to monitor the hot carrier drain current degradation.

The stress time dependence plot of dI_{dsat} (= $(I_{dsat} - I_{dsat}(0))/I_{dsat}(0)$) degradation is shown in Fig. 1. By assuming 10% degradation of saturation drain current as a device lifetime (τ), the device lifetime of the narrowest device is approximately 7 times shorter than that of wide width devices. This shows that the degradation rate was significantly enhanced with scaling down of the device width. In Fig. 1, it is observed that both wide and narrow channel devices exhibit slopes, which are nearly parallel to each other. This suggests the degradation mechanism is the same for both wide and narrow channel devices.

To find the relationship between device degradation and interface state generation, dI_{dsat}-ΔN_{it} is

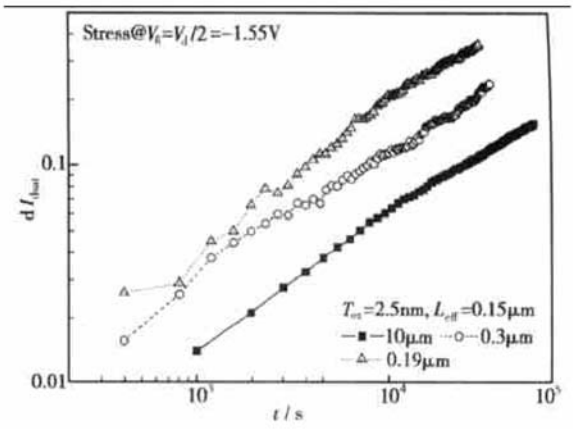

Fig. 1 Relationship of I_{dsat} degradation and stress time for pMOSFETs with different ration of channel width to length Wide devices exhibited longer time taken to reach 10% dI_{dsat} compared to narrow devices.

plotted in Fig. 2 for pMOSFETs with different channel width. ΔN_{it} is measured by CP method. A unified curve of dI_{dsat} vs interface state generation (ΔN_{it}) can be found. All data under different stress voltages align themselves on a unified curve, regardless of the channel width. The degradation of other characteristic parameters, such as maximum

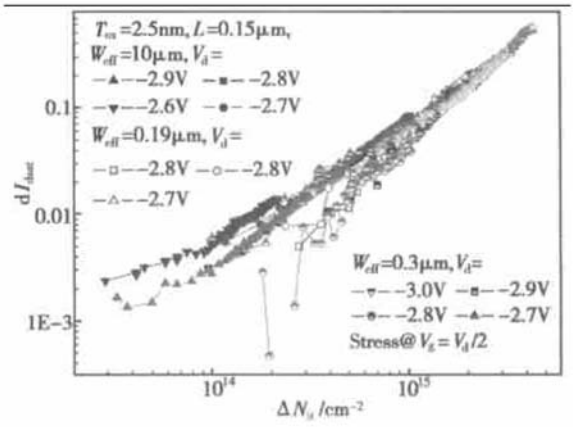

Fig. 2 Unified curve of dI_{dsat} versus interface state generation (ΔN_{it}) for pMOSFETs with different channel widths

conductance (g_m), linear current ($I_{d,line}$) and threshold voltage (V_t) has the same unified curves as I_{dsat}. This shows that the main degradation mechanism is interface state generation for pMOSFETs with different channel width under $V_g = V_d/2$

when the device gate oxide thickness decreases to a certain value. This unified curve suggests a lifetime prediction model can be made on the basis of interface state density for pMOSFETs with different channel widths.

To explain the above results, various measurements have been carried out for pMOSFETs with different gate widths. The relationship of $\tau I_d/W$ versus I_b/I_d, for different channel gate widths are plotted in Fig. 3, where I_b and I_d are substrate and drain current and W is channel width. The model has been generally accepted in nMOSFETs lifetime prediction under the condition that the main degradation mechanism is interface state generation[7]. All data points aligned themselves on a straight

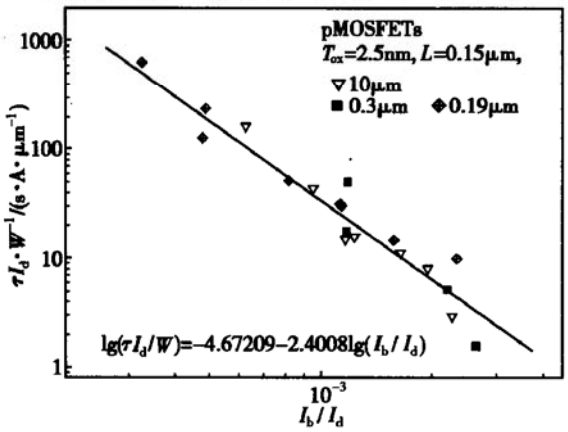

Fig. 3　pMOSFETs lifetime data and simulations using the proposed model plotted on $\tau I_d/W$ versus I_b/I_d A unified line can be found for pMOSFETs with different channel width.

line in lg-lg scale; and the exponential value is identical. This indicates the main degradation mechanism is the same for devices with different channel width, which is consistent with the claimal before. The same value of impact on the ionization rate results in the same degradation, which shows the electric field in the channel is universally distributed and not focused on the certain region. Although it was reported that the narrow channel width device had the smaller vertical field[1] and resulted in the lower degradation under the same impact ionization rate, the device degradation does not show corresponding degradation characteristics[1]. So the conclusion can be made that the device degradation is mainly caused by lateral electric field and basically independent on the distribution of vertical field. The width-enhanced device degradation phenomena can be explained by the width-enhanced impact ionization rate.

The relationship of the degradation of impact ionization rate (I_b/I_d) and stress time for different channel gate widths is plotted in Fig. 4. Obviously, the impact ionization rate decreases at initial stage and then increases after stress due to the combina-

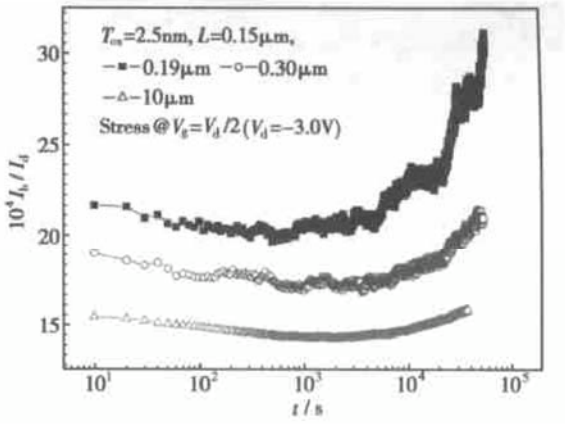

Fig. 4　Impact ionization rate increases with reducing gate width for pMOSFETs under $V_g = V_d/2$ stress mode

tion of oxide traps and interface states generation, which change the lateral field in devices. The inflection point is almost the same under the same stress voltage, which suggests the same degradation mechanism during degradation process. Moreover, it can also be seen that the narrow-width device has larger impact on the ionization rate. For example, the impact ionization rate for pMSOFETs with 0.19μm channel width is about 1.4 times larger than that with 10μm channel width. The impact ionization rate is generally used to characterize the lateral electric field. The increase of impact ionization rate indicates the increase of lateral electric field with device narrowing, which can be attributed to the current-crowding effect, width-enhanced threshold voltage, the change of characteristic saturated length or the influence of series resistance[8, 11].

Figure 5 shows the substrate and drain current versus gate bias for pMOSFETs with the gate width of 0.19, 0.30, and 10μm. It can be seen that I_{bmax}/W (I_{bmax} is the maximum substrate current) increases with the decreasing channel width, while I_d/W almost remain unchanged. This suggests that the impact on ionization increases sharply with the decrease of channel width. The difference of substrate current at peak substrate current condition was significant for various device widths, but the substrate current of narrow width was not significantly higher for high gate bias conditions. So, the current-crowing effect can be excluded from the cause for width-enhanced impact ionization rate[8]. The abnormal substrate current can only be explained by the larger lateral electric field in the narrow channel device with the decreasing channel width.

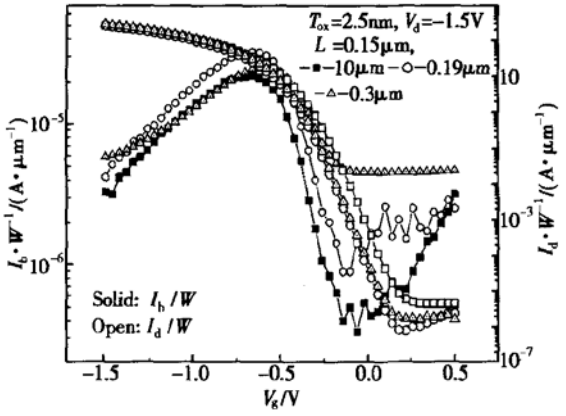

Fig. 5 I_b/W and I_d/W increase with reducing gate width for pMOSFETs

The impact ionization rate I_b/I_d generally can be written as[9]:

$$\frac{I_b}{I_d(V_d - V_{dsat})} = A_i \exp\left(\frac{-B_i l_d}{V_d - V_{dsat}}\right) \quad (1)$$

where A_i and B_i are technology-dependent constants, V_d is drain voltage, l_d is the characteristic length of the velocity saturation region, which is dependent on the gate oxide thickness and junction depth.

The experimental V_{dsat} are found to fit a physical expression if $E_{sat} = 2\times10^5$V/cm was used, V_{dsat} is the pinch-off voltage, which can be expressed as[4]:

$$V_{dsat} = \frac{L_{eff}E_{sat}(V_g - V_t)}{L_{eff}E_{sat} + (V_g - V_t)} \quad (2)$$

where E_{sat} is the critical electric field for velocity saturation, V_g is the gate voltage, L_{eff} is the effective channel length. Plotting $I_b/I_d/(V_d - V_{dsat})$ vs $1/(V_d - V_{dsat})$, A_i and $B_i l_d$ can be derived. It can be seen from Eq. (1) that the impact ionization rate is dependent on $V_d - V_{dsat}$ and l_d.

A plot of threshold voltage, V_t, against the effective channel width, is shown in Fig. 6. There is an observed increase in threshold voltage as channel width decreases. This implies a larger lateral

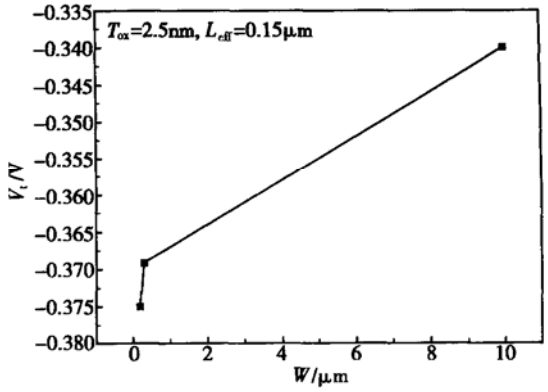

Fig. 6 Plot of threshold voltage versus effective channel width

electric field in the narrow channel device, as compared to the wide channel device, from Eq. (1) above. If the change of threshold voltage is the cause for the abrupt increase of impact ionization rate, the same $V_d - V_{dsat}$ should produce the same impact ionization rate. The plots of $I_b/I_d/(V_d - V_{dsat})$ versus $1/(V_d - V_{dsat})$ for W_{eff}= 10, 0.3, and 0.19μm are shown in Fig. 7 and the same $V_d - V_{dsat}$ leads to the different impact ionization rate I_b/I_d. The slope of $\lg(I_b/I_d/(V_d - V_{dsat}))$ versus $1/(V_d - V_{dsat})$ corresponds to $B_i l_d$. In addition, l_d is thought to be irrespective of channel width. Therefore, the conclusion can be made that such a slight increase in threshold voltage cannot explain the degradation behavior of the narrow channel devices as compared to the wide channel devices and the only reason lies in the influence of increased series resis-

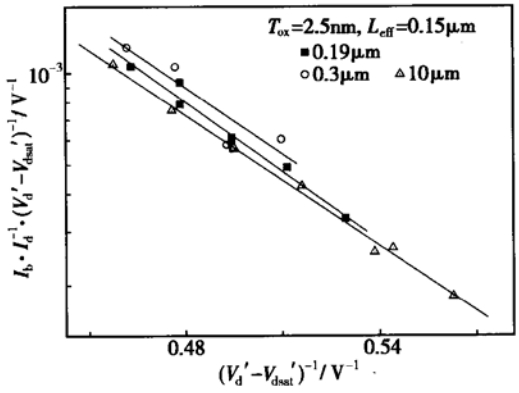

Fig. 7　Plot of $I_b/I_d/(V_d - V_{dsat})$ versus $1/(V_d - V_{dsat})$ for W_{eff} = 10, 0.3, and 0.19μm　The oxide thickness is 2.5nm and channel length is 0.15μm.

tance by the introduction of HALO structure.

The introduction of HALO structure increases the total series resistance of devices. For wide-channel devices, S&R method is taken to extract total series resistance to be 52Ω, and the corresponding total resistance (V_g = − 1.5V) is about 300Ω. The influence of series resistance cannot be neglected and V_d and V_{dsat} should be corrected as follows:

$$V'_d = V_d - I_d(V_d) R_d \quad (3)$$

$$V'_{dsat} = V_{dsat} - I_{dsat}(V_{dsat}) R_d \quad (4)$$

where R_d is the drain parasitic resistance.

The plot of $I_b/I_d/(V'_d - V'_{dsat})$ versus $1/(V'_d - V'_{dsat})$ for W_{eff}= 10, 0.3, and 0.19μm is shown in Fig. 8 and the same $V'_d - V'_{dsat}$ leads to the different

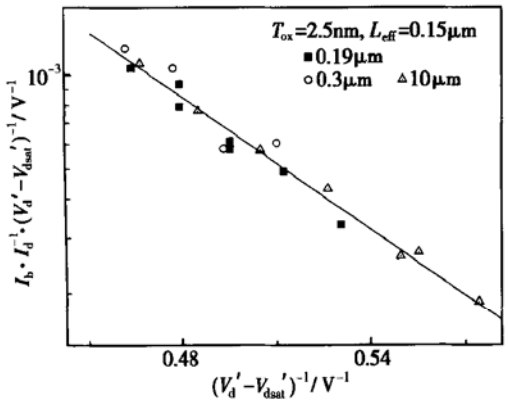

Fig. 8　Plot of $I_b/I_d/(V'_d - V'_{dsat})$ versus $1/(V'_d - V'_{dsat})$ for W_{eff}= 10, 0.3 and 0.19μm　The same $V'_d - V'_{dsat}$ leads to the different impact ionization rate I_b/I_d.

impact ionization rate I_b/I_d. So the conclusion can be made that the width-enhanced device degradation is caused by the combination of width-enhanced threshold voltage and series resistance.

3 Conclusion

In this paper, the degradation characteristics of both wide and narrow devices under $V_g = V_d/2$ stress mode is investigated. The width-enhanced device degradation can be seen with devices narrowing. The main degradation mechanism is interface state generation for pMOSFETs with different channel widths. The width-enhanced device degradation is caused by width-enhanced impact ionization rate. Through the investigation of many possible causes such a current-crowding effect, slight increase of threshold voltage with the decrease of channel width, the change of characteristic length of the velocity saturation region and the influence of series resistance, the cause of the width-enhanced device degradation is attributed to the combination of width-enhanced threshold voltage and series resistance.

References

[1] Yue J M P, Chim W K, Chao B J, et al. Channel width effect on hot-carrier degradation in NMOSFETs with recessed-LOCOS isolation structures. IEEE Proceedings of 7th IPFA'99, Singapore, 1999: 94

[2] Chin D, Pan S, Wu K. Geometry effect on CMOS transistor stability under DC gate stress. In: IEEE Preceeding of International Reliability Physics Symposium, 1993: 66

[3] Chung S S, Chen S J, Yang W J, et al. A new physical and quantitative width dependent hot carrier mode for shallow-trench-isolated CMOS devices. In: IEEE Preceeding of International Reliability Physics Symposium, 2001: 419

[4] Chung J, Jeng M C, May G, et al. Hot-electron currents in deep-submicrometer MOSFETs. In: IEEE, IEDM Tech Digest, 1988: 200

[5] Lee W, Lee S, Ahn T, et al. Degradation of hot carrier lifetime for narrow width MOSFET with shallow trench isolation. In: IEEE Preceeding of International Reliability Physics Symposium, 1999: 259

[6] Chen J F, Ishimaru K, Hu C. Enhanced hot-carrier induced

degradation in shallow trench isolation narrow channel PMOSFEs. IEEE Electron Device Lett, 1994, 15: 427

[7] Hu C M, Tam S C, Hsu F C, et al. Hot-electron induced MOSFET degradation-model, monitor, and improvement. IEEE Trans Electron Devices, 1985, 32(2): 375

[8] Chung J, Jeng M C, May G, et al. Hot-electron currents in deep-submicrometer MOSFETs. IEEE IEDM, 1988: 200

[9] Ong T C, Ko P K, Hu C. Hot-carrier current and device degradation in surface-channel pMOSFE′s. IEEE Trans Electron Device, 1990, 37: 1658

[10] Mizuno T, Toriumi A, Iwase M, et al. Hot carrier effect in 0.1μm gate length CMOS devices. IEEE IEDM, 1992: 695

$V_g = V_d/2$ 应力模式下宽度变窄对 HALO-pMOSFETs 退化的影响*

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摘要: 讨论了最差应力模式下($V_g = V_d/2$)宽沟和窄沟器件的退化特性. 随着器件沟道宽度降低可以观察到宽度增强的器件退化. 不同沟道宽度 pMOSFETs 的主要退化机制是界面态产生. 沟道增强的器件退化是由于沟道宽度增强的碰撞电离率. 通过分析电流拥挤效应, 阈值电压随沟道宽度的变化, 速度饱和区特征长度的变化和 HALO 结构串联阻抗这些可能原因, 得出沟道宽度增强的热载流子退化是由宽度降低导致器件阈值电压和串联阻抗降低的共同作用引起的.

关键词: 宽度增强退化; 尖断电压; 电流拥挤效应

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