

Development of Novel Thin-Film SOI High Voltage MOSFET

Li Wenhong¹ and Luo Jinsheng²

(1 ASIC & System State Key Laboratory, Fudan University, Shanghai 200433, China)

(2 Xi'an Jiaotong University, Xi'an 710049, China)

Abstract: Two kinds of thin-film SOI high voltage MOSFETs are developed. One is general structure, the other is novel two-drift-region structure. The gate width is $760\mu\text{m}$, and the active area is $8.58 \times 10^{-2}\text{mm}^2$. The experiments show that the breakdown voltages of the two-drift-region and general structures are 26V and 17V, respectively, and the on resistances are 65Ω and 80Ω , respectively.

Key words: SOI; MOSFET; high voltage device

EEACC: 2560; 2560B

CLC number: TN386

Document code: A

Article ID: 0253-4177(2003)12-1261-05

1 Introduction

SOI technology is the important research area^[1,2], which offers nearly ideal dielectric-isolation (DI) and relatively simple isolation process. DI has more advantages than junction-isolation (JI), which realizes the completely electric isolation of low-voltage circuit from high-voltage devices. So the study of SOI smart power IC has received much attention, and the design of SOI high-voltage devices is one of the major issues in the area of SOI smart power IC^[3].

Two methods have been proposed for achieving high-voltage devices on SOI substrates. One uses relatively thick top layer of silicon, which is called thick-film SOI technology, the other is thin film SOI (TFSOI) technology. The former makes it more difficult to realize lateral isolation structures, the latter avoids the problem of the lateral isolation structure. So TFSOI technology has caught the attention of many researchers, and several high-voltage structures have been given^[4,5].

In this paper, two kinds of TFSOI high voltage MOSFETs are presented. One is general struc-

ture and the other is novel two-drift-region structure. The experiments show that the breakdown voltages are 17V and 26V, respectively.

2 Device structure and process

The cross sections of the general TFSOI high voltage MOSFET and two-drift-region TFSOI high voltage MOSFET are given in Fig. 1. The devices in Fig. 1 are analyzed with MEDICI and analytical model^[6].

Figure 2 gives the results for surface potential distributions of drift region, in which Figure 2(a) is the general structure and Figure 2(b) is two-drift-region structure. In Fig. 2(a), along x direction the curves of potential distribution are similar to a ladder, which is only related to y -variable in the ladder area. Meanwhile the analytical model and simulation show that the potential distribution is relative to the drift region length. If the drift length is shorter than a certain value, the potential distribution does not resemble a ladder at all, which rises monotonously.

Along x direction there are two electric field peak values at the interfaces of the pn and n^+n

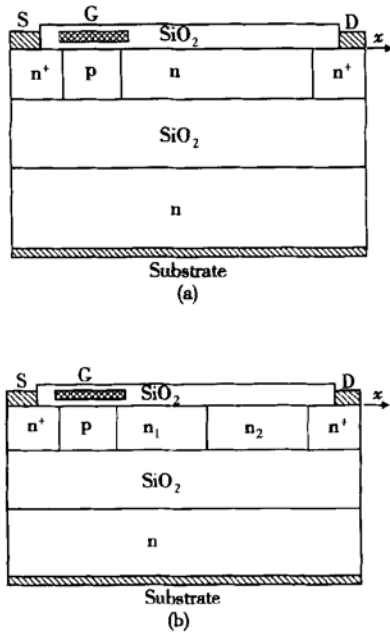


Fig. 1 Schematic diagram of device structure (a) General TFSOI high voltage MOSFET; (b) Two-drift-region TFSOI high voltage MOSFET

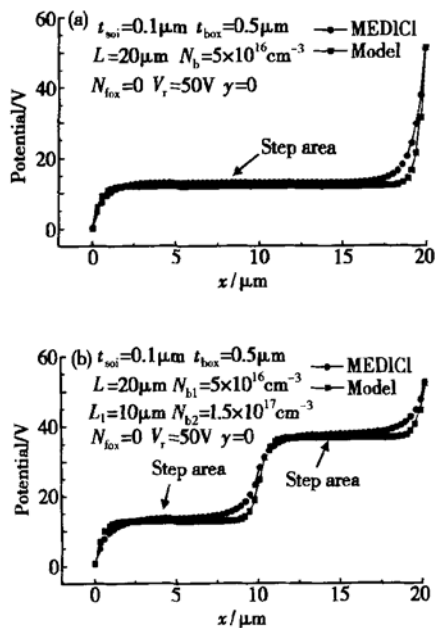


Fig. 2 Surface potential distribution (a) General structure; (b) Two-drift-region structure

junctions, and the electric field is small between two peak values. When the doping concentration N_b of the drift region is small, the highest peak value is at the interface of the n^+ n junction, and the highest peak value moves from the interface of the

n^+ n junction to the interface of the pn junction with the increase of the doping concentration N_b . In fact this means that the breakdown point moves from the interface of the n^+ n junction to the interface of the pn junction with the increase of the doping concentration.

It is easily known that the surface potential and electric field distributions of the general structure are similar to that of the single FR (field ring) termination. The difference is that the former varies with the doping concentration of the drift region and the later does with the ring spacing.

Figure 2(b) is the potential distribution of two-drift-region structure. Along x direction the curves of potential distribution are similar to the two-level-ladder in SOI layer, which shows that the potential is only related to y -variable in the ladder areas of two drift regions. So along x direction there are three electric field peak values at the interfaces of the pn_1 , n_1n_2 and n^+n_2 junctions, and the electric field is smaller between two peak values. As compared with Fig. 2(a), two-drift-region structure improves the distribution of the potential clearly, the applied bias is supported by the pn_1 , n_1n_2 and n^+n_2 junctions, not only pn and n^+n junctions in Fig. 2(a). This means that the breakdown voltage increases, and the more the number of the drift regions is, the higher the breakdown voltage is, but the process is more difficult too. In practice the number of the drift regions is determined by the compromise of the breakdown voltage and the process difficulty^[6].

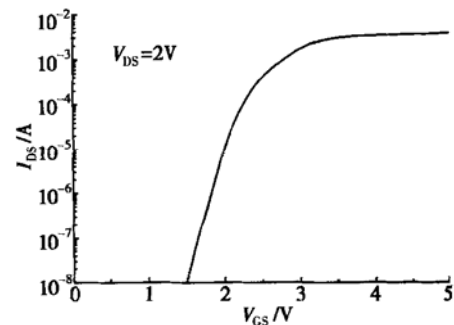


Fig. 3 Threshold test curve

As compared to general TFSOI structure, the potential and electric field distributions of the two-drift-region structure resemble that of the two-FR termination. This contributes to understand the physical meaning of two-drift-region structure supporting higher breakdown voltage.

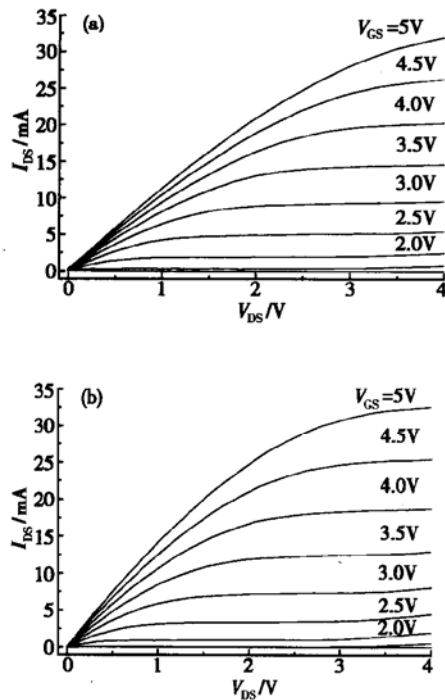


Fig. 4 Output characteristics (a) General TFSOI high voltage MOSFET, Drift region length $5\mu\text{m}$; (b) Two-drift-region TFSOI high voltage MOSFET, Two drift region length $2.5\mu\text{m}/2.5\mu\text{m}$

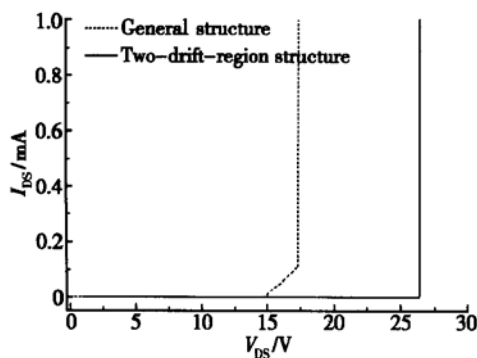


Fig. 5 Breakdown voltage test results

The general and two-drift-region thin-film SOI high voltage MOSFETs are designed, which adopt the enclosed gate structures. The gate length is about $2\mu\text{m}$ and the gate width is $760\mu\text{m}$. Mean-

while the bulk contact area connected with p-type channel is designed to avoid the parasitic bipolar transistor.

The substrate is SIMOX made by IBIS. The top Si is 180nm and the buried oxide layer is 380nm . After isolation boron is implanted and the p-type channel region is formed. The implant conditions are 40keV and $3 \times 10^{12}\text{cm}^{-2}$. Then the gate oxide and polysilicon are deposited. The gate oxide thickness is about 46nm . Finally, the drift region and bulk contact region and source/drain region are implanted and annealed.

The final device parameters are given in Table 1. The device micrograph is presented in Fig. 6.

Table 1 Device parameters

Thickness of top Si	180nm
Thickness of buried SiO_2	380nm
Gate SiO_2 thickness	46nm
Gate length	$2\mu\text{m}$
Drift region length for general TFSOI high voltage MOSFET	$5\mu\text{m}$ and $10\mu\text{m}$
Drift region length for two-drift-region TFSOI high voltage MOSFET	$2.5\mu\text{m}/2.5\mu\text{m}$ and $5\mu\text{m}/5\mu\text{m}$
Width of gate	$760\mu\text{m}$
Active area	$8.58 \times 10^{-2}\text{mm}^2$

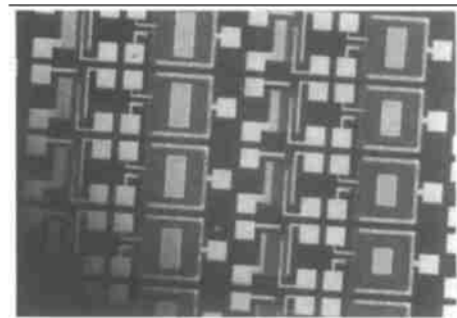


Fig. 6 Device micrograph

3 Device characteristic and analysis

The analytical model and simulation show the two-drift-region TFSOI MOSFETs have higher breakdown voltage, lower on-resistance and higher performance. The cause is that the two-drift-region not only improves the potential and electric field distributions of drift region but also increases the density of drift region.

HP4156 is used to measure the characteristics.

3.1 Threshold voltage and subthreshold characteristics

Figure 3 is the test results of threshold voltages, which is 1.7V when I_{DS} equals $1\mu A$. Meanwhile the slope of subthreshold is 150mV/dec.

3.2 Breakdown voltage

The test breakdown voltages of general structure and two-drift-region structure TFSOI MOSFET are 17V and 26V respectively, which are shown in Fig. 5. It is apparent that the breakdown voltage of two-drift-region structure increases by 53% than that of general structure. The test results prove the analysis of section 2.

Meanwhile the results show that the length of drift region does not affect the breakdown voltage. The analytical model and MEDICI simulation show that the length of drift region does not affect the breakdown voltage when the length is longer than a value. On the conditions of assuring the breakdown voltage the length of drift region should be as short as possible.

3.3 Output characteristics and transconductance

Figure 4 contains the test curves of output characteristics for two kinds of devices. When the gate voltage equals 5V, the saturated drain current of general TFSOI high voltage MOSFET is 31.9mA, the on-resistance is 80Ω and the transconductance is 11.3mA/V. At the same conditions the saturated drain current of two-drift-region TFSOI high voltage MOSFET is 32.6mA and the on-resistance is 65Ω and the transconductance is 14.3mA/V. So the on-resistance decreases by 18% and the transconductance increases by 26.5%.

In sum, the two-drift-region TFSOI high voltage MOSFET has more advantages comparing to

general TFSOI high voltage MOSFET. The breakdown voltage increases by 53% and the on-resistance decreases by 18%. The analysis and the experiments show that multiple-drift-region TFSOI high voltage MOSFET has higher breakdown voltage and less on-resistance, which is different with Si high voltage MOSFET. The on-resistance of Si high voltage MOSFET increases by 2.5-power with breakdown voltage. The more the number of drift region is, the better the effect is, but the more complex the process is. So the trade-off is necessary in the design of multiple-drift-region structure TFSOI high voltage MOSFET.

4 Conclusion

The novel two-drift-region and general TFSOI high voltage MOSFETs are developed. The analytical model and simulations and experiments show that the former has more advantages comparing with the latter. The breakdown voltage increases by 53% and the on-resistance decreases by 18%.

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新型薄膜 SOI 高压 MOSFET 的研制

李文宏¹ 罗晋生²

(1 复旦大学专用集成电路与系统国家重点实验室, 上海 200433)

(2 西安交通大学, 西安 710049)

摘要: 研制了两种薄膜 SOI 高压 MOSFET, 一种是一般结构, 另一种是新的双漂移区结构. 两者的栅宽均为 $760\mu\text{m}$, 有源区面积为 $8.58 \times 10^{-2} \text{mm}^2$, 测试表明其击穿电压分别为 17V 和 26V, 导通电阻分别为 80Ω 和 65Ω .

关键词: 绝缘体上硅; 金属氧化物半导体场效应晶体管; 高压器件

EEACC: 2560; 2560B

中图分类号: TN386

文献标识码: A

文章编号: 0253-4177(2003)12-1261-05