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Design and Fabrication of Power $Si_{1-x}Ge_x$/Si Heterojunction Bipolar Transistor for Wireless Power Amplifier Applications*

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Abstract: A multi-finger structure power SiGe HBT device (with an emitter area of about 166μm^2) is fabricated with very simple 2μm double-mesa technology. The DC current gain β is 144.25. The B-C junction breakdown voltage reaches 9V with a collector doping concentration of $1\times10^{17}cm^{-3}$ and a collector thickness of 400nm. Though our data are influenced by large additional RF probe pads, the device exhibits a maximum oscillation frequency f_{max} of 10.1GHz and a cut-off frequency f_T of 1.8GHz at a DC bias point of $I_C=10mA$ and $V_{CE}=2.5V$.

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1 Introduction

Power amplifiers (PA) are key components in the wireless communications industry. Historically, gated field-effect structures such as the MESFET structure have been widely used in the PA field. Now, due to higher gain and current density at the frequencies employed, bipolar transistors have become as the preferred choice. Unfortunately, the conventional low-cost silicon BJTs (bipolar junction transistors), in which the frequency response is limited by intrinsic Si material properties, are not suitable for microwave and RF applications. GaAs HBTs have dominated in such applications. However, the high-cost, low thermal conductivity, and poor mechanical strength of these materials make them unsuitable for high-level integration. A bandgap-engineered SiGe HBT is an emerging alternative, due to the advantages of low cost, superior thermal conductivity, and compatibility with Si CMOS technology.

The implementation of microwave monolithic integrated circuit (MMIC) power amplifiers is useful and necessary for system-on-a-chip scenarios. The demonstration of a MMIC power amplifier is still lacking. With more advantages compared to III-V group material, the SiGe HBT MMIC power amplifier has received more great attention as a potential candidate for wireless communication applications. Some efforts on the microwave power application of SiGe-based HBTs have been reported[1~6]. The challenge faced by SiGe-based MMIC PA technologies is to provide power HBTs with sufficient high-voltage immunity without compromising device performance[7]. In this paper we describe a very simple fabrication technology for SiGe HBT, in which only 5 patterns are needed. With 2μm double-mesa technology, multi-finger (2 cells, 4 fingers) structure power SiGe HBTs are fabricated. We also discuss and illustrate key device design issues for power $Si_{1-x}Ge_x$/Si HBTs suitable for wireless PA applications.

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2 Device structure design and fabrication process

The heterostructure, as shown in Fig. 1, was grown on a low-resistivity ($\rho = 2.4 \times 10^{-3} \Omega \cdot cm$) 50mm Si wafer in one step by UHV/CVD. The maximum boron concentration of $2 \times 10^{19} cm^{-3}$ in the base layer ensures a low base access/spreading resistance. The high doping substrate is directly used as a sub-collector to achieve a smaller collector access/spreading resistance. The doping concentration in the emitter cap layer is also $2 \times 10^{19} cm^{-3}$ so as to reduce emitter contact resistance.

Emitter cap	Si	n^+	P $2 \times 10^{19} cm^{-3}$	100nm
Emitter	Si	n	P $1 \times 10^{18} cm^{-3}$	100nm
Spacer	$Si_{1-x}Ge_x$ ($0.22 \leq x \leq 0.25$)	i		10nm
Base	$Si_{1-x}Ge_x$ ($0.22 \leq x \leq 0.25$)	p	B $2 \times 10^{19} cm^{-3}$	25nm
Spacer	$Si_{1-x}Ge_x$ ($0.22 \leq x \leq 0.25$)	i		10nm
Collector	Si	n^-	P $1 \times 10^{17} cm^{-3}$	400nm
Substrate	Si(110)	n^+	$5 \times 10^{18} cm^{-3}$	400μm

Fig. 1 SiGe/Si double-heterostructure bipolar transistor

In order to obtain a large current handling capability, a multiple finger structure design for the emitter and base contacts is often chosen. But a configuration, in which all emitter and base fingers are bound together with a narrow finger spacing, will be disadvantageous for reducing thermal effects. All the emitter fingers can be divided into several subcells, in each of which several fingers are bound together with a narrow finger spacing. This configuration can not only reduce thermal effects without increasing C_{BC} (B-C junction capacitance), but also decrease collector spreading resistance.

Double mesa-type HBTs were fabricated with standard liftoff and etching techniques. The fabrication process was initiated by ICP etching with photoresist protection to form a base mesa. The etching depth was about 500nm. Then the Cr/Au (50nm/100nm) films were evaporated on top of the wafers. The emitter electrode was formed with standard lithography and liftoff techniques. The patterned emitter electrode served as the mask for base exposure. Then wet etching with KOH-based solution ($KOH : K_2Cr_2O_7$: propanol : H_2O = 100g : 4g : 100mL : 400mL) was used to expose the SiGe base layer and form the emitter mesa. Then base electrode metal and collector electrode metal Cr/Au (40nm/60nm) deposition was performed simultaneously with standard lithography and liftoff techniques. Device passivation was achieved by the PECVD deposition of 650nm SiO_2 at 300 ℃. This layer also was served as the dielectric layer for the metal layer structure during interconnection deposition. Via-holes were then opened using wet etching, and 600nm Al was evaporated. Wet etching was used to form a metal layer structure for interconnection. Figure 2 shows the micrograph of a finished two-cell four-finger common-emitter HBT. The emitter finger width is 2μm, and the length is 26μm. The space between the fingers is 2μm. Figure 3 shows the schematic cross-section of a cell of SiGe/Si DHBT. The space between the base mesa and the collector metal is 3μm. The space between the emitter mesa and the base metal is 2μm.

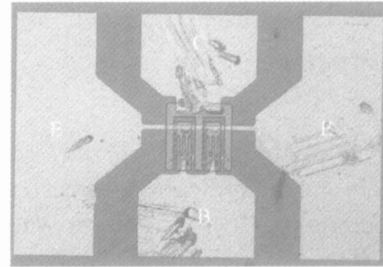

Fig. 2 Micrograph of a two-cell four-finger DHBT

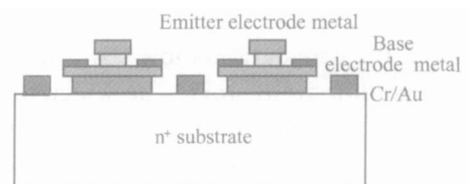

Fig. 3 Schematic cross-section of a cell of SiGe/Si DHBT

3 Results and discussion

The DC characteristics of the devices have been measured with an HP4155A semiconductor parameter analyzer. The I-V curves of a 4 finger HBT are shown in Fig. 5. It exhibits a maximum DC current gain β of 144.25. The measured B-C junction breakdown voltage is over 9V with a collector thickness of 400nm. The offset voltage of the common emitter configuration is about 0.1V. The offset voltage is small, which is an advantage in terms of the power added efficiency (PAE). The knee (saturation) voltage of the CE configuration is only 1.2V, which is attributed to the reduced collector

access resistance from the vertical heterostructure design (much thicker subcollector layer) and layout design (3μm separation between the base mesa and collector metal). With the increasing of the collector current, no notable current gain fall-off is found. No thermal effects are observed in the *I-V* curves, mainly because of the novel distributed layout.

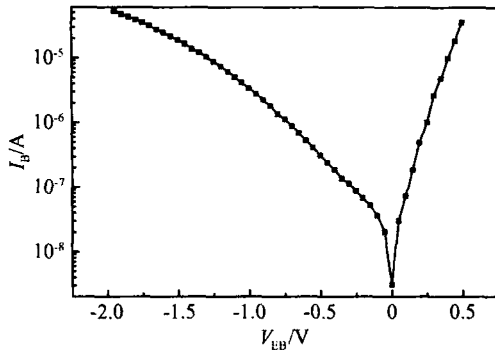

Fig. 4 *I-V* curves of BE junction SiGe/ Si DHBT

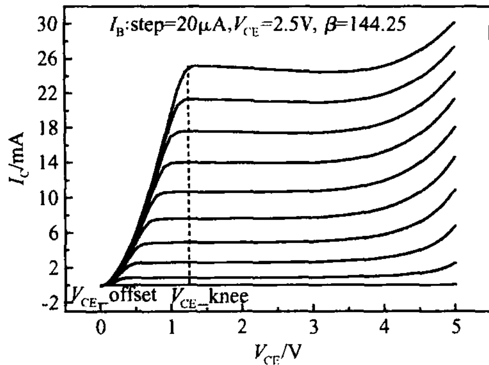

Fig. 5 *I-V* characteristics of a 4 finger HBT

The high base leakage current is commonly observed in double-mesa Si/ SiGe HBT, which mainly arises from the insufficiently passivated surface states and the noncoincidence between the BE pn junction and the Si/ SiGe heterojunction. The BE junction *I-V* curves are shown in Fig. 4. The BE junction saturation leakage current is only 3.1×10^{-9} A, which indicates excellent interface quality and sufficiently passivated surface states.

For small signal RF characteristic, on-wafer probing *S*-parameter measurement was performed using an HP8510C network analyzer. Figure 6 shows the current gain $|h_{21}|$, the unilateral power gain *U*, and maximum stable gain of the device at a DC bias point of I_C = 10mA and V_{CE} = 2.5V. Though the measured results are influenced by the large additional RF probe pads, the device exhibits a maximum oscillation frequency f_{max} of 10.1GHz and a cut-off frequency f_T of 1.8GHz. In order to make the HBT testable, additional RF probe pads must be connected to it, and they can have a significant influence on the measurement results [7]. If their influence on the data is removed, f_T and f_{max} will be much larger. The maximum power gain is MSG(maximum stable gain) = 24.9dB and U (Mason unilateral gain) = 25.6dB.

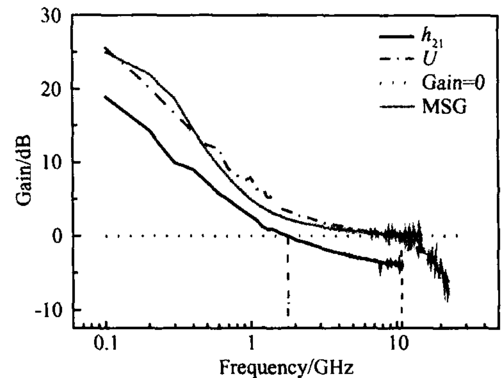

Fig. 6 Measured small signal frequency response of the device

The design goal for a power HBT is to achieve high-frequency operation while maintaining high breakdown voltages and high current density for high output power operation. These requirements are interrelated, and an optimal design has to be performed. For wireless PA applications, SiGe HBT device design is constrained by the performance tradeoff defined by the well known Johnson Limit[8]. It states that due to material limitations in carrier transient velocity and avalanche generation, the product of current-gain cutoff frequency and open-base breakdown voltage should be kept relatively constant. Thus, it is challenging to achieve high BV_{CBO} and high f_T simultaneously.

The design of the collector region has a more profound effect on the overall performance of a power HBT[9]. Device performance such as collector-base avalanche breakdown voltage, maximum collector current density, carrier total transit delay time from emitter to collector, and base-collector junction capacitance are mainly determined by collector thickness and doping concentration. A p^+ ($Si_{0.75}Ge_{0.25}$, doping concentration $2 \times 10^{19} cm^{-3}$)-n^- (Si, as collector)-n^+ (Si) junction avalanche

breakdown voltage and maximum collector current density(J_{max}) as functions of collector thickness at various doping concentrations were simulated by commercial software MATLAB. The simulated results are shown in Figs. 7 and 8, which show that the design of the collector region is critical for achieving high performance.

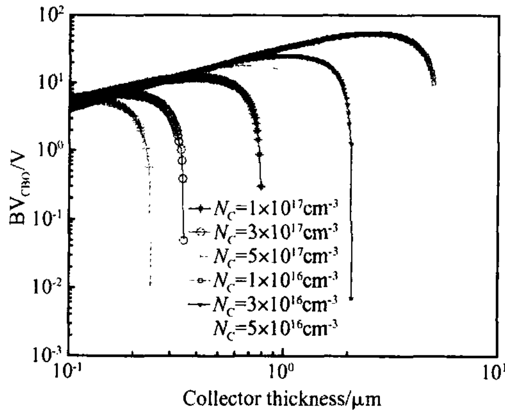

Fig. 7 Breakdown voltage as a function of collector thickness at various doping concentrations

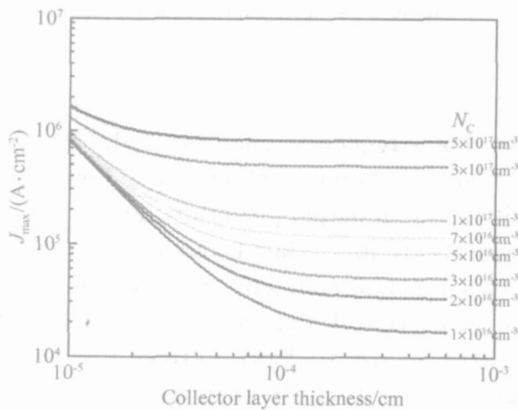

Fig. 8 J_{max} as a function of collector thickness at various doping concentrations

In Fig. 7, it can be seen that generally, lighter collector layer doping concentration and larger layer thickness can result in higher breakdown voltage and lower maximum collector current density and vice versa. However, the maximum collector thickness should not exceed the collector-side depletion width of the base-collector junction under normal operating conditions (the B-C junction maximum depletion width $\frac{\varepsilon_{Si} E_C}{qN_C}$ (E_C is the critical electrical field, ε_{Si} is the Si dielectric constant, N_C is the collector doping concentration), as the undepleted portion of the collector layer will lead to parasitic collector resistance, which can cause a dramatic decrease in the maximum breakdown voltage. With respect to the frequency response, a thicker collector layer will also result in a larger delay time when carriers are moving at their saturation velocity in the fully depleted collector layer.

In Fig. 8, it can be seen that the maximum current density that the device can handle is very sensitive to the collector doping concentration, which is restricted by the Kirk effect. If the collector doping concentration is especially low, J_{max} will notably decrease with the increase of the collector thickness. Increased collector doping raises the collector capacitance, which degrades f_{max} and U_{max}. Therefore, the doping concentration must be properly selected and well-controlled during the growth the of material structure.

The simulation shows the B-C junction breakdown voltage reaches 11V, and the measured result is 9V. The measured result is in good agreement with the simulation. The simulation shows that the maximum collector current density is about $1.2\times10^5 A/cm^2$. Because the maximum current and maximum voltage are limited to avoid a possible breakdown when the device is measured, the maximum collector current in Fig. 5 is not the actual maximum collector current that the device can handle. In Fig. 5, I_{Cmax} is 26mA, so we know that the actual maximum collector current density is larger than $1.6\times10^4 A/cm^2$.

The simulated results show that device performance, including collector-base avalanche breakdown voltage and maximum collector current density, is mainly determined by collector thickness and doping concentration. The design goal for a power HBT is to achieve high-frequency operation while maintaining high breakdown voltages and high current density for high output power operation. A high output power can be realized in two ways: employing a higher breakdown voltage with a lower current density or a lower breakdown voltage with a higher current density. The former also offers the advantage of better output linearity. The latter, in its extreme, can result in excessive heat generation across the device with a very high and nonuniformly distributed junction temperature. The nonuniform temperature distribution deteriorates the power performance by rendering the center part of the device useless for high-power opera-

tion[12]. As a consequence, a high breakdown voltage with low current density, which can be obtained by designing a thick and lightly doped collector layer (limited by the Kirk effect), is preferred for power HBT design. The doping concentration is usually selected from 1×10^{16} to 1×10^{17} cm^{-3} for the collector design of power $Si_{1-x}Ge_x$/ Si HBT for wireless power amplifier applications. An appropriate maximum collector thickness can be selected from Fig. 7. It is usually from 400nm to 2μm. If the thickness is much larger, it can increase the carrier total transit delay time from the emitter to the collector and base-collector junction capacitance.

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用于无线 PA 的高频大功率 $Si_{1-x}Ge_x$/ Si HBT 的设计和制作 *

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摘要: 采用简单的双台面工艺制作了完全平面结构的 2 个单元 4 个发射极指的 SiGe HBT. 在没有扣除测试结构的影响下, 当直流偏置 $I_C = 10mA$, $V_{CE} = 2.5V$ 时, f_T 和 f_{max} 分别为 1.8 和 10.1GHz. 增益 β 为 144.25, BV_{CBO} 为 9V.

关键词: $Si_{1-x}Ge_x$/ Si HBT; 高频; 大功率; 无线功率放大器

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