An Ultra Wideband VHF CMOS LC VCO *

Ning Yanqing†, Wang Zhihua, and Chen Hongyi

(*Institute of Microelectronics, Tsinghua University, Beijing* 100084, *China*)

Abstract: This paper presents a VHF CMOS VCO. The most significant improvement on the VCO is that the cross-coupled MOSFET pairs are divided into several switchable parts so the characteristics can compensate the state change that results from the frequency tuning of the oscillator. This VCO is implemented in 0.18μm CMOS with a core area of about 550μm ×700μm. The test results show that the tuning range covers 31～111MHz with a power consumption between 0.3～6.9mW and a phase noise at a 100kHz offset of about - 110dBc/ Hz.

Key words: wideband; VCO; CMOS
EEACC: 1230B; 7150E
CLC number: TN432 **Document code:** A **Article ID:** 0253-4177(2006)01-0014-05

1 Introduction

CMOS LC VCO has been widely used in communication systems for its outstanding phase noise performance. But the tuning range of a signal VCO has never exceeded 73 %[1]. In wideband systems, a multi-oscillator or down-convert scheme has been applied. There has been much theoretical analysis and optimization of VCOs oscillating at a fixed frequency. Most such work was concerned with elevating the oscillator's FOM, which involves phase noise, power consumption, the quality factor of the LC tank, and the tuning range[2,3]. But analysis related to the tuning situation has been sparse. The tuning range has been assumed to be proportional to the square root of the LC production change in the tank. The active circuit, which was made up of a cross-coupled MOSFET pair and a bias circuit, compensated the energy loss in the LC tank. Before 2004[4], the active circuit's nonlinear characteristic and its interactive relation with the LC tank were omitted. On the other hand, Tang *et al*.[5] provided a detailed analysis of the tuning curve affected by the varactor's nonlinear characteristic in the time-domain.

As described in Ref. [6], CMOS LC VCO can be implemented in an np- p- or n-core. In the updated literature, the widest tuning range acquired with an n-core and np-core were 42 % and 23 % respectively[7,8]. By modifying the bias MOSFET of the n-core, a 73 % tuning range was achieved[1]. A new topology to enlarge the tuning range is illustrated based on a simple analysis in this paper.

2 Analysis of a tuned VCO

Figure 1(a) is the schematic of a common n-core CMOS LC VCO, and Figure 1(b) is the simplified circuit obtained by regarding the cross-coupled MOSFET pair as a negative resistor. The differential equation of Fig. 1(b) is

$$\frac{d^2v}{d\tau^2} + \left[\frac{1}{Q} + \sqrt{\frac{L}{C}}\, i'(v)\right]\frac{dv}{d\tau} + v = 0 \qquad (1)$$

where $\tau = t/\sqrt{LC}$, $Q = (1/R_Q)\sqrt{L/C}$.

Since the quality factor Q of the LC tank was treated as a constant, Equation (1) is reasonable. According to Eq. (1), under frequency tuning by an input voltage, the effective capacitance of the varactor alters both the time-normalized relation and the coefficient of $i'(v)$. The most obvious effect was the change in output amplitude. In previous works, the tail current I_0 was adjusted to compensate the change. As in the design example of Ref. [4], Table

* Project supported by the National Natural Science Foundation of China (Nos. 60475018 and 60372021) and the State Key Development Program for Basic Research of China (No. G2000036508)

† Corresponding author. Email: nyq02@mails.tsinghua.edu.cn

Received 21 July 2005, revised manuscript received 10 October 2005

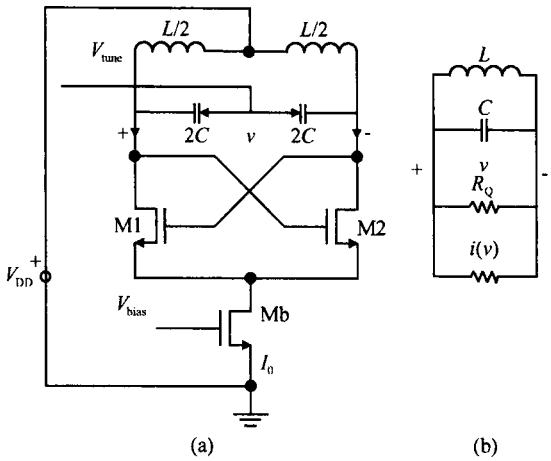

Fig. 1 CMOS LC VCO and its simplified circuit

1 illustrates the relative capacitance change, the amplitude variety and the changed tail current to compensate it, and the parameters V_n, V_s of the characteristic of the cross-coupled MOSFET pair, where $V_s = V_n^2/4V_T + V_T/2$.

Table 1 Capacitance change and bias current compensation

Relative capacitance	Amplitude change/ V	Compensated bias current/ mA	V_n/ V	V_s/ V
0.25	2.47	5.3	1.47	1.35
0.64	2.16	6.8	1.68	1.67
1	1.92	8	1.83	1.92
1.96	1.31	10.9	2.13	2.52
2.96	0.40	13.7	2.39	3.10

According to Table 1, at the original capacitance, the output amplitude is equal to V_s, which is the optimal working state. Before compensation, the working state changes in the "voltage-limited regime", in which the capacitance is reduced since the output amplitude increases. After compensation, the working state is in the "current-limited regime", in which the capacitance is reduced since the output amplitude keeps to the original value while the cross-coupled MOS pair is biased with a lower V_s. This coefficient change was overlooked in previous works but it indeed alters the state of the oscillator. As described above, although the fixed size cross-coupled MOSFET pair schematic can work well in a tuning range of less than 50 %, the work state is shifted away from the optimal point.

To sum up the analysis, besides the tuning of capacitance, another prerequisite for wideband CMOS LC VCO is the proper characteristic of the cross-coupled MOSFET pair to compensate the coefficient shift in Eq. (1), in other words, to keep the VCO in the optimal working state.

3 New topology

In theory, seamless frequency coverage of the VCO requires a continuous change of the transistor size in the active circuit to keep the optimal state along the frequency change. But a MOSFET with a continuous width/ length ratio is impossible in a real circuit. Since changing the bias current can work in a narrow tuning range, one practical solution is to divied the active circuit into switchable parts geared for the coarse-tuning and to adjust the bias current for fine-tuning.

According to Ref. [4], if the bias current I_0 is proportional to the width/ length ratio of the cross-coupled MOSFET pair, then $i(v)$ is proportional to the bias current, or to the MOSFET's size. If two or more cross-coupled MOSFET pairs are connected in parallel, the total characteristic is proportional to the sum of the MOSFET's sizes. The bias MOSFET Mb can be used as a switch. When the gate of Mb is connected to ground, there is no current through the MOSFETs. The cross-coupled MOSFET pair is in the "off" mode, and so influences only the parasitic capacitance of the LC tank. The "on" mode can be set by connecting the gate to a special voltage. The proportional relation requires the size of Mb to be proportional to that of M1 and M2.

Figure 2 illustrates the full schematic of the design. The inductor, varactors, and active circuit are paralleled to nodes A and B. All the transistors of the active circuit are implemented in pMOS for lower flicker noise level. Unlike the former schematic, the active circuit is divided into five parallel parts, which are scaled down by two with the index 0 to 4. The "off" mode is set by connecting the gate of Mbk to V_{DD} through S_{NK}. Since the sizes of M1k and M2k are identical and proportional to that of Mbk, no matter which and how the S_{Nk} is set, the total $i(v)$ characteristic is proportional to the width/ length ratio sum of M1k in the "on" mode. The inductor uses an off-chip fixed inductor of about 726nH. Two measures are adopted in order to get the maximal C_{max}/C_{min} ratio of the varactor. The first is that all varactors employed are pMOS va-

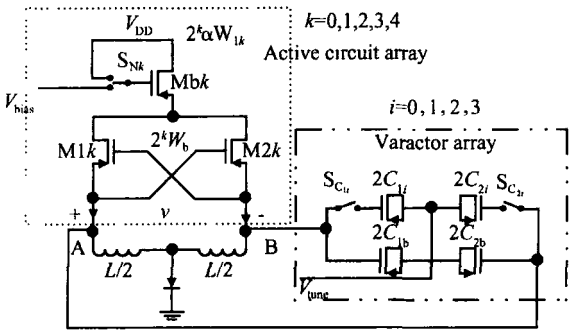

Fig. 2 Full schematic of the proposed VCO

ractors working in the inversion mode. One pair of varactors C_b is connected to nodes A and B directly, and four pairs of varactors, which are indexed 0 to 3 from the smallest to the largest, are connected to nodes A and B through the switch pair $S_{C_{1i}}$, $S_{C_{2i}}$. The switches are located at the tank sides in order to reduce the parasitic capacitance resulted from the pMOS varactors. The second measure is the use of a Si-diode to bias the DC voltage of nodes A and B to about 0.63V. This method would bias the control voltage of the pMOS varactor from the range of $0\sim V_{DD}$ to about $-0.63\sim V_{DD}-0.63$(V). In this design, the power V_{DD} is 3.3V.

4 Layout and experiment results

The proposed VCO is implemented in a 0.18μm CMOS process. The microphotograph of the VCO is shown in the left part of Fig. 3. The total die area is 1mm ×1.5mm, and the VCO core is about 550μm ×700μm. The right part is the detailed part of the active circuit described in the former paragraph. The cross-coupled MOSFET pairs are placed symmetrically in the upper right part. The bias MOSFETs Mb0～Mb4 are placed together for the sake of symmetry.

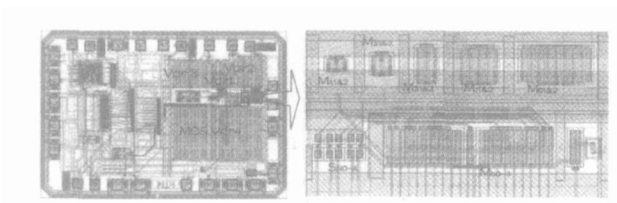

Fig. 3 Die photograph

The VCO drives a pair of on-chip voltage-followers presented in Ref. [9]. The die is bounded to the PCB directly. A transformer is used to change the differential signal to a one-end signal. The switches are set by an MPU through a 3-line interface.

An Agilent 8563EC spectrum analyzer is used for spectrum and phase noise measurement, and a HP 54845A oscilloscope is used for waveform recording and the measurement of peak-to-peak voltage and frequency. During testing, the $S_{C_{1i}}$, $S_{C_{2i}}$ states are set, and the control voltage V_{tune} is first adjusted. Second, the output amplitude is adjusted to about $0.25V_{pp}$ by switching S_{Nk} and adjusting V_{bias} by a bias current. Then the output frequency, phase noise, and current consumption of the VCO core are recorded. After the experiments, the test results are processed using Matlab. Figure 4 shows the test results of the tuning characteristics of the designed VCO. The band is indexed in the manner of $1+\sum 2^i$. Although the curves are not distributed evenly, the overlap between the adjacent bands is over 4%, and the total operating frequency is from 31 to 111MHz (112%). As shown in Fig. 5, in the full operating frequency range, the phase noise at a 100kHz offset is -105 to -117dBc/Hz, and the core power consumption is 0.3 to 6.9mW. The total size of the cross-coupled MOSFET in the "on" mode is plotted with the left Y-axis multiplied by 20. It is approximately proportional to the core current compensation. Figure 6 shows a typical phase noise spectrum at about 65MHz.

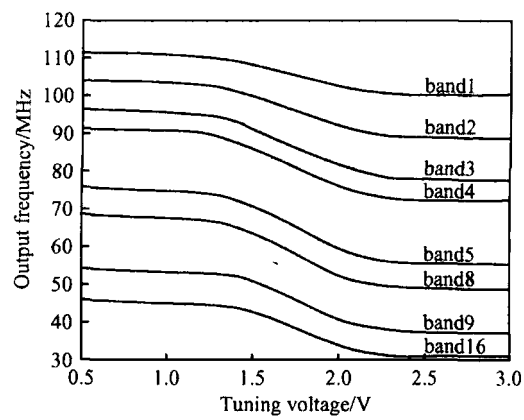

Fig. 4 Test results of tuning characteristic The band is indexed in $1+\sum 2^i$.

The measured frequency range can cover both the VHF L band of the TV system and FM band of

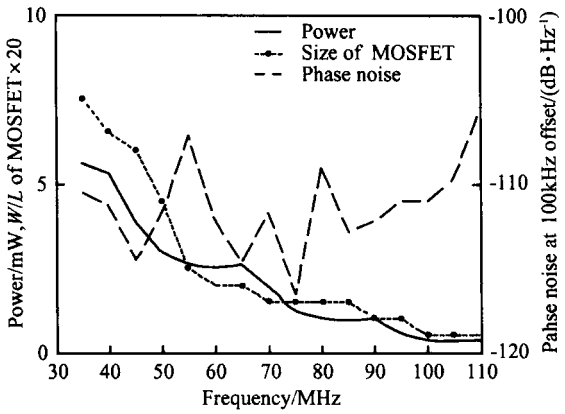

Fig. 5　Test results of phase noise at a 100kHz offset, size of cross-coupled MOSFET in "on" mode, and core bias current

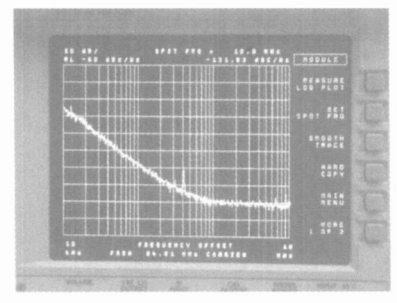

Fig. 6　Photograph of typical phase noise spectrum at about 65MHz

radio system.

5　Conclusion

This paper analyzes the CMOS LC VCO under tuning. A new topology of switchable cross-coupled MOSFET pair is provided that can compensate its characteristic widely to compensate for the work state shifting with frequency tuning. An example is illustrated which covers the frequency range of 31～111MHz. The measurements show that the power consumption and phase noise at 100kHz offset in the full band are 0.3～6.9mW with 3.3V supply and - 117～ - 105dBc/ Hz respectively. The circuitry is implemented in a 0.18μm CMOS process with a core area of about 550μm ×700μm. Although the new topology is a bit more complex than the traditional one, it can break the tuning range of the n or np-core and is much simpler than the multi-oscillator or down-convert schematic.

References

[1] Berny A D, Niknejad A M, Meyer R G. A 1.8-GHz LC VCO with 1.3-GHz tuning range and digital amplitude calibration. IEEE J Solid-State Circuits, 2005, 40(4): 909

[2] Ham D, Hajimiri A. Concepts and methods of optimization of integrated LC VCOs. IEEE J Solid-State Circuits, 2001, 36(6): 896

[3] Zanchi A, Samori C, Levantino S, et al, A 2-V 2.5-GHz-104-dBc/ Hz at 100kHz fully integrated VCO with wide-band low-noise automatic amplitude control. IEEE J Solid-State Circuits, 2001, 36(4): 611

[4] Buonomo A, Schiavo A L. Modelling and analysis of differential VCOs. Int J Circuits Theory Appl, 2004, 32: 117

[5] Tang Zhangwen, He Jie, Min Hao. A LC voltage-controlled oscillator tuned by switched step capacitors: part Ⅰ. analysis of tuning characteristics. Chines Journal of Semiconductors, 2005, 26(10): 2010(in Chinese) [唐长文, 何捷, 闵昊. 一种采用开关阶跃电容的压控振荡器(上): 调谐特性的理论分析. 半导体学报, 2005, 26(10): 2010]

[6] Park Y, Chakraborty S, Lee C H, et al. Wide-band CMOS VCO and frequency divider design for quadrature signal generation. IEEE MIT-S Digest, 2004: 1493

[7] Papalias T A, Lee T T, Hajimiri A, et al. Reprogrammable, wide tuning range 1.6GHz CMOS VCO with low phase noise variation. IEEE Radio Frequency Integrated Circuits, 2004: 479

[8] Zhang Haiqing, Zhang Qianling. Design of 2.5GHz low phase noise CMOS LC-VCO. Chinese Journal of Semiconductors, 2003, 24(11): 1154

[9] Payne R F, Alvin C J. A high speed analog 50Ω line driver in digital CMOS technology. IEEE 39th Midwest Symposium on Circuits and Systems, 1997: 29

超宽频带 VHF 频段 CMOS LC VCO *

宁彦卿† 王志华 陈弘毅

(清华大学微电子学研究所, 北京 100084)

摘要: 实现了一个宽频带 VHF 频段 CMOS VCO. 其最大的改进在于将振荡器中交叉耦合 MOS 管分为并联可开关的若干段. 这样使其特性可以在较大范围内补偿 VCO 调频过程中状态的变化. 该 VCO 使用标准 0.18μm CMOS 工艺制作, 核心版图面积约为 550μm ×700μm. 测试结果表明: 该 VCO 频率覆盖范围为 31～111MHz; 功耗为 0.3～6.9mW; 在 100kHz 频偏处相位噪声约 - 110dBc/ Hz.

关键词: 宽带; 压控振荡器; CMOS

EEACC: 1230B; 7150E

中图分类号: TN432 **文献标识码**: A **文章编号**: 0253-4177(2006)01-0014-05

* 国家自然科学基金(批准号:60372021,60475018)和国家重点基础研究发展规划(批准号:G2000036508)资助项目

† 通信作者. Email:nyq02 @mails.tsinghua.edu.cn

2005-07-21 收到, 2005-10-10 定稿