Simulation of a Double-Gate Dynamic Threshold Voltage Fully Depleted Silicon-on-Insulator nMOSFET

Bi Jinshun†, Wu Junfeng, and Hai Chaohe

(*Institute of Microelectronics, Chinese Academy of Sciences, Beijing* 100029, *China*)

Abstract: A novel planar DGDT FDSOI nMOSFET is presented, and the operation mechanism is discussed. The device fabrication processes and characteristics are simulated with Tsuprem 4 and Medici. The back-gate n-well is formed by implantation of phosphorus at a dosage of $3\times10^{13}\,cm^{-2}$ and an energy of 250keV and connected directly to a front-gate n^+ polysilicon. This method is completely compatible with the conventional bulk silicon process. Simulation results show that a DGDT FDSOI nMOSFET not only retains the advantages of a conventional FDSOI nMOSFET over a partially depleted (PD) SOI nMOSFET——that is the avoidance of anomalous subthreshold slope and kink effects but also shows a better drivability than a conventional FDSOI nMOSFET.

Key words: double-gate structure; dynamic threshold; FDSOI; nMOSFET
EEACC: 2560
CLC number: TN386.1 **Document code:** A **Article ID:** 0253-4177(2006)01-0035-06

1 Introduction

With the reduction of feature size, supply voltage is scaled down to consume less power according to the equation $P = C_L V_{dd}^2 f_d$, where P is the power consumed by a single gate, C_L is the total switching capacitance of the gate, V_{dd} is the power supply voltage, and f_d is the average cooperating frequency of the gate[1]. At the same time, the threshold voltage should be scaled down in order not to degrade the speed of the circuit significantly. However, the reduction of the threshold voltage gives rise to another problem: an increase in off-state current, resulting in an increase in the consumption of standby power in a static circuit and an increase in the possibility of failure in dynamic circuits and memory arrays[2,3].

Until now, many novel device structures have been reported to improve device performance and without increasing leakage current as happens in DTMOS and DGSOI[4~8]. The DTMOS gate and body are connected to change the threshold voltage dynamically, which requires an ultra low supply voltage (below 0.6V) to avoid leakage at the source/body junction. It is hard to expand the advantages of DTMOS beyond 1V. DGSOI performs perfectly, but the process fabrication is very complicated. In this paper, a DGDT FDSOI nMOSFET, which combines the advantages of DTMOS and DGSOI without the limitation of the supply voltage, is presented.

For a DGDT FDSOI nMOSFET, the back-gate n-well is formed by the implantation of phosphorus at a dosage of $3\times10^{13}\,cm^{-2}$ and an energy of 250keV. It is then connected directly to the front-gate n^+ polysilicon. BOX layer damage by ion implantation is not considered a problem in this work[9,10]. When the gate voltage rises, the back-gate—working as the control gate—raises the body potential so that the threshold voltage is reduced and the drive current is increased. While V_{gs} is 0V, as in conventional FDSOI nMOSFETs, the leakage current is small (There is no back-gate n-well connected to the front-gate polysilicon, and the substrate is grounded.). But the back channel should be disabled the whole time to avoid back channel leakage current. This is the main difference between DGDT FDSOI nMOSFETs and other conventional double gate devices. A p substrate is fixed

† Corresponding author. Email: bravehawk@126.com
Received 25 May 2005, revised manuscript received 9 October 2005

at the most negative potential, so the leakage current between the back-gate n-well and the p substrate is negligible.

2 Device structure and fabrication description

Figure 1 shows the layout of the active island and the overall nMOSFET. The active island was composed of Part 1 and Part 2. Part 1 and the BOX layer below it were partially etched off for the connection between the front-gate polysilicon and the back-gate n-well. The device had a buried oxide and an initial silicon film with thicknesses of 150 and 100nm, respectively. The active island was formed by STI isolation deep into the substrate. The depth of the trench was 650nm. The function of the STI was to isolate the active island and the back-gate n-well. Phosphorus was implanted with an energy of 250keV and a dosage of $3\times10^{13}\,cm^{-2}$ so that it could pass into the substrate to form the back-gate n-well. The average doping concentration just under the BOX layer was about $1.3\times10^{18}\,cm^{-3}$. Before the formation of the gate oxide, B^+ and BF_2^+ ions were implanted into the channel with energies of 40 and 50keV and dosages of 10^{13} and $10^{11}\,cm^{-2}$, respectively, to adjust the threshold voltage of the front channel and avoid a leakage current in the back channel. Part 1 of the active island was etched off by RIE before the gate oxide formation. After 19nm gate oxide was grown, the BOX layer under Part1 was partially etched, followed by 410nm polysilicon depositions forming hard local front-gate and back-gate connections, as shown in Fig. 2(a).

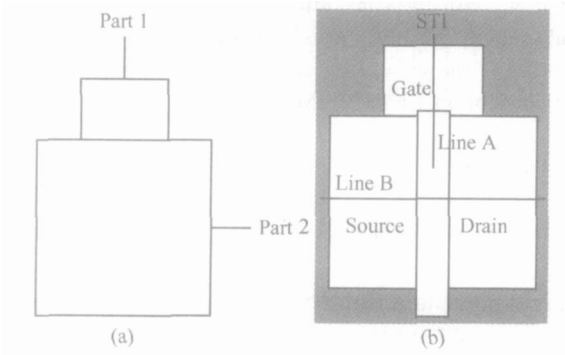

Fig. 1 (a) Layout of the active island composed of Part 1 and Part 2. Part 1 and the BOX layer below it will be partially etched off for the connection between the front-gate polysilicon and back-gate n-well; (b) Layout of the nMOSFET

By this way, the front-gate and back-gate stay at the same potential which is the basis of DGDT FDSOI. The polysilicon was patterned and etched to form the 0.8μm gate. Then phosphorus implantation with an energy of 20keV and a dosage of $5\times10^{13}\,cm^{-2}$ was performed to form an LDD/LDS structure. After a 400nm oxide spacer formation, n^+ doping was performed by the implantation of phosphorus ($1\times10^{15}\,cm^{-2}$, 70keV) and arsenic ($3\times10^{15}\,cm^{-2}$, 50keV). In order to activate the impurities implanted in the silicon film, a rapid thermal process (RTP) was performed for 5s at 1000 ℃. Germanium with an energy of 30keV and a dosage of $3\times10^{14}\,cm^{-2}$ was implanted in order to form a shallow salicide. A 25nm titanium film was deposited followed by two steps of annealing to form salicidation. The final silicon film thickness is about 75nm. The combination of silicon film thickness, doping concentration, and gate type resulted in a DGDT FDSOI nMOS device. Figure 2(b) shows the schematic cross section of the device. The impurity concentration along the channel region after process simulation with Tsuprem 4 is given in Fig. 3, and the phosphorus concentration distribution under the BOX layer is shown in Fig. 4.

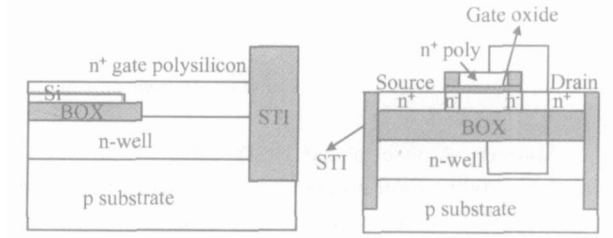

Fig. 2 (a) Cross section along line A showing the contact between the front-gate and back-gate n-well; (b) Schematic cross section of the device along line B

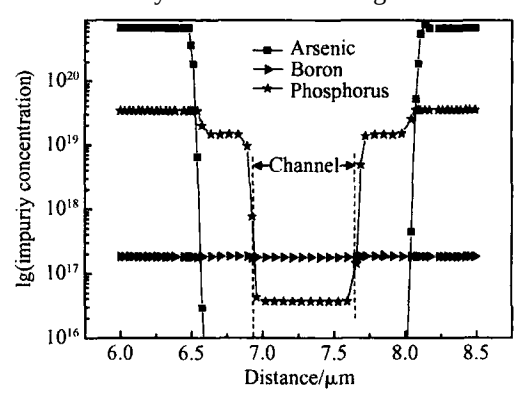

Fig. 3 Impurity concentrations along the channel region after process simulation

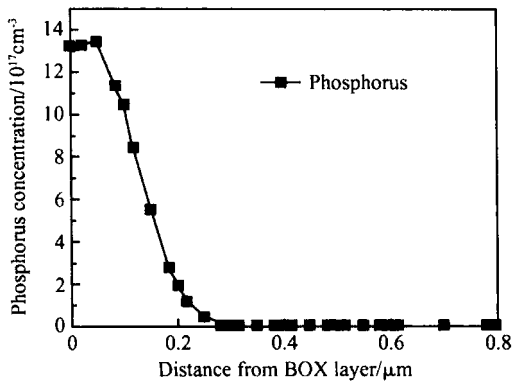

Fig. 4　Phosphorus concentration distribution beneath the BOX layer after process simulation

3　Mechanism of DGDT FDSOI nMOSFET

3.1　Theory of operation

We use a four-terminal (source, drain, front-gate, and back-gate) thin film FDSOI nMOSFET as shown in Fig. 5 to explain the operation mechanism of our proposed structure. In a DGDT FDSOI nMOSFET's case, the back-gate is connected with front-gate, while in a conventional FDSOI nMOSFET's case, the substrate is grounded. Impurity distributions in the top silicon films of a DGDT FDSOI and conventional FDSOI nMOSFET are the same.

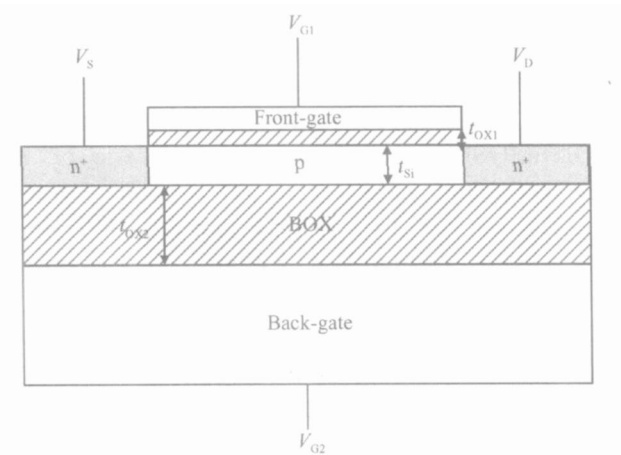

Fig. 5　Cross section of the four-terminal thin film FDSOI nMOSFET

The threshold voltage of a FDSOI nMOSFET has a strong relationship with its back-gate, which is called the "back-gate effect". When back channel is in the "depletion state", which is the case for DGDT FDSOI nMOSFET, the threshold voltage of the front channel can be expressed as [11]

$$V_{th1,dep2} = V_{th1,acc2} - \frac{C_{Si}C_{OX2}}{C_{OX1}(C_{Si}+C_{OX2})}(V_{G2} - V_{G2,acc}) \quad (1)$$

where C_{OX1} and C_{OX2} are the capacitances of the front-gate and back-gate oxides, respectively, $C_{Si} = \frac{\varepsilon_{Si}}{t_{Si}}$ where ε_{Si} is the permittivity of Si, $V_{th1,acc2}$ is the threshold voltage of the front channel when the back channel is in the "accumulation state", and $V_{G2,acc}$ is the back-gate bias voltage that puts the back channel in the "accumulation state" when the front channel is turned on.

For a thin film FDSOI nMOSFET, the back-gate effect factor "γ" can be expressed as a back-gate-voltage derivative of the front channel threshold voltage. When the back channel is in the "inversion state" or "accumulation state" by back-gate bias, an inversion charge or accumulation charge can mask the effect of the back-gate electronic field, so the back-gate effect factor can be assumed to be zero. When the back channel is in the "depletion state"[11]

$$\gamma = \frac{dV_{th1,dep2}}{dV_{G2}} = -\frac{C_{Si}C_{OX2}}{C_{OX1}(C_{Si}+C_{OX2})} = -\frac{\varepsilon_{Si}C_{OX2}}{C_{OX1}(\varepsilon_{Si}+t_{Si}C_{OX2})} \quad (2)$$

In most cases, γ is approximately $-\frac{t_{OX1}}{t_{OX2}}$. The minus sign of the back-gate effect factor shows that the threshold voltage drops when $V_{front\text{-}gate\text{-}source}$ = $V_{back\text{-}gate\text{-}source}$ rises. Figure 6 illustrates this behavior for a FDSOI nMOSFET, where a separate terminal is used to control the back-gate voltage.

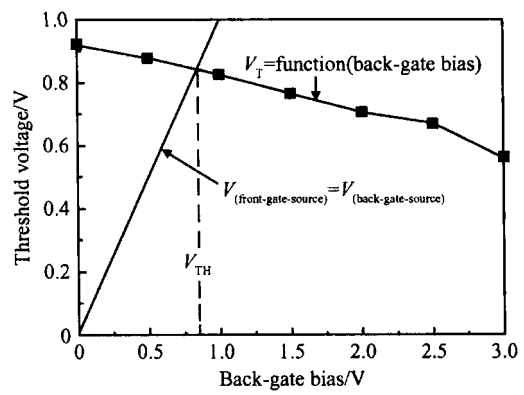

Fig. 6　Threshold voltage of FDSOI nMOSFET as a function of the back-gate-source forward bias V_T ($V_{back\text{-}gate\text{-}source}$ = 0V) = 0.92V, but V_T ($V_{back\text{-}gate\text{-}source}$ = 3V) = 0.56V　V_{TH} represents the point where the gate bias of the DGDT FDSOI nMOSFET and the threshold voltage become identical.

The threshold voltage is a function of the back-gate-source forward bias and drops when the back-gate bias rises. When $V_{\text{front-gate-source}} = V_{\text{back-gate-source}} = V_{TH}$, the front channel is turned on for a DGDT FDSOI nMOSFET. We should note that $V_{TH} = 0.844$V is less than V_T ($V_{\text{back-gate-source}} = 0$V) $= 0.92$V and that V_T drops further from 0.844 to 0.56V when $V_{\text{front-gate-source}} = V_{\text{back-gate-source}}$ rises further beyond threshold voltage to 3V. According to the theory of operation above, ΔV_T is approximately $\gamma\Delta V_{gs} = -\frac{t_{OX1}}{t_{OX2}}\Delta V_{gs} = -0.38$V. The simulation shows that $\Delta V_T = V_T$ ($V_{\text{back-gate-source}} = 3$V) $- V_T$ ($V_{\text{back-gate-source}} = 0$V) $= -0.36$V. So the theory fits the numerical simulation well.

This lower threshold voltage does not come at the expense of a higher off-state leakage current, for DGDT and conventional FDSOI nMOSFETs have the same V_T when $V_{\text{front-gate-source}} = V_{\text{back-gate-source}} = 0$V. In fact, they are almost the same in all respects and consequently have the same leakage current, but a DGDT FDSOI NMOSFET has more drivability.

That γ is approximately $-\frac{t_{OX1}}{t_{OX2}}$ means that we need to make the BOX layer thinner and the influence of the back-gate more obvious: in other words, the threshold voltage can drop faster and farther. But there is another factor we should consider. That is the avoidance of back channel leakage or turn-on. When the BOX layer is thinner, the voltage needed to turn on the back channel is smaller, and the back channel leakage is more obvious. This is unwanted. If the BOX layer is too thick, the influence of the back-gate is negligible, and the performance of the DGDT FDSOI nMOSFET will almost be the same as a conventional FDSOI nMOSFET. We need the turn-on voltage of the back channel to be much higher than the supply voltage, and at the same time the BOX layer must be as thin as possible to enhance the back-gate effect. Usually, we set the thickness of the back-gate oxide or BOX layer at about 8～10 times the thickness of the front-gate oxide. In this work, the ratio of the BOX layer thickness to the front-gate oxide thickness is 150nm/19nm. For a sub-100nm gate length nMOSFET as shown in Ref. [12], the BOX can be thinner than 20nm.

3.2 Simulation results

We used Medici[13] as a device simulator to simulate the DC characteristics of the DGDT FDSOI nMOSFET. The parameters of this device are based on process simulation above with Tsuprem 4[14] with 0.8μm channel length, 75nm t_{Si}, 19nm t_{OX1}, and 150nm t_{OX2}.

In Fig. 7, the simulated output characteristics of DGDT FDSOI nMOSFET are compared with those of the conventional FDSOI nMOSFET with the substrate grounded. The gate is biased at 1, 2, and 3V, respectively. The kink effect is not observed.

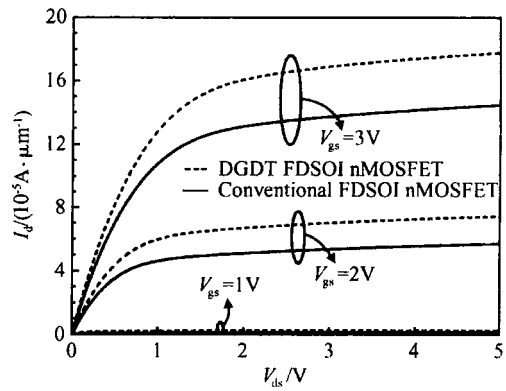

Fig. 7 Simulated output characteristics of the DGDT and conventional FDSOI nMOSFET

The threshold voltage of the DGDT FDSOI nMOSFET drops when the gate voltage rises, so the difference of drive current between the DGDT FDSOI nMOSFET and the conventional FDSOI nMOSFET is greater. But the ratio of I_{on} (DGDT FDSOI nMOSFET) and I_{on} (conventional FDSOI nMOSFET) degrades. The ratio is 2 when $V_{gs} = 1$V, 1.3 when $V_{gs} = 2$V, and 1.23 when $V_{gs} = 3$V, respectively.

Simulated I_{ds}-V_{gs} characteristics of DGDT and conventional FDSOI nMOSFETs are shown in Fig. 8. No anomalous subthreshold slope is found for both the DGDT and the conventional FDSOI nMOSFET. The gate's controllability of the drain current of the DGDT FDSOI nMOSFET is better than that of the conventional FDSOI nMOSFET; in other words, the transconductance of the DGDT FDSOI nMOSFET is greater, as shown in Fig. 9. The DGDT FDSOI nMOSFET shows better subthreshold slope characteristics, the same leakage current the conventional FDSOI nMOSFET, and

greater transconductance.

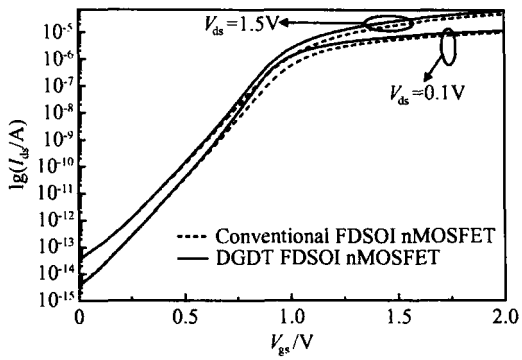

Fig. 8　Simulated I_{ds}-V_{gs} characteristics of the conventional FDSOI and DGDT FDSOI nMOSFETs biasing at 0. 1 and 1. 5V

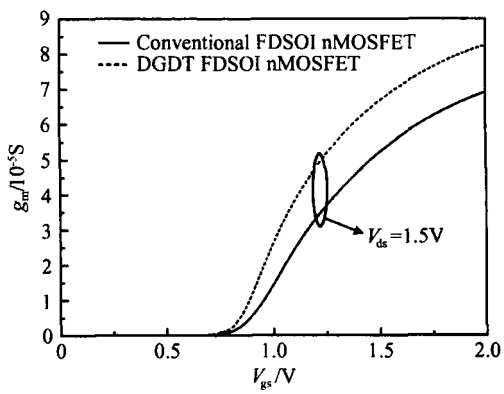

Fig. 9　Simulated transconductance characteristics of the DGDT and conventional FDSOI nMOSFETs with the drain biased at 1. 5V

4 Conclusion

A double-gate dynamic threshold voltage (DGDT) SOI nMOSFET inherits advantages from the conventional FDSOI nMOSFET, including the avoidance of anomalous subthreshold slope and kink effects in partially depleted (PD) SOI nMOSFETs. In addition, the DGDT FDSOI nMOSFET changes threshold voltage dynamically to enhance drivability. But the improvement does not come at the expense of greater off-state current. When the gate is biased at 0V, the off-state current of the DGDT FDSOI nMOSFET is the same as the conventional FDSOI nMOSFET. In addition, the DGDT FDSOI nMOSFET shows better subthreshold slope and transconductance characteristics than the conventional FDSOI nMOSFET.

References

[1] Jin W, Chan P C H, Chan M. On the power dissipation in dynamic threshold silicon-on-insulator CMOS inverter. IEEE Trans Electron Devices, 1998, 45(8): 1717

[2] Assaderaghi F, Hu C M, Ko P K, et al. Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI. IEEE Trans Electron Devices, 1997, 44(3): 414

[3] Roy K, Mukhopadhyay S, Mahmoodi-Meimand H. Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits. Proceedings of the IEEE, 2003: 305

[4] Chen Guoliang, Huang Ru. Design guidelines of nano-scaled SOI-DTMOS device. Solid-State and Integrated Circuits Technology, 2004: 295

[5] Chang S J, Chang C Y, Chen C, et al. High-performance and high-reliability 80-nm gate-length DTMOS with indium super steep retrograde channel. IEEE Trans Electron Devices, 2000: 2379

[6] Solomon P M, Guarini K W, Zhang Y, et al. Two gates are better than one double-gate MOSFET process. IEEE Circuits and Devices Magazine, 2003: 48

[7] Philip Wong H S, Chan K K, Yuan Y, et al. Self-aligned (top and bottom) double-gate MOSFET with 25nm thick silicon channel. IEDM Tech Dig, 1997: 427

[8] Lin J T, Chang S C, Huang K Y, et al. Recessed multi-gate SOI MOSFET in deep decananometer regime. IEEE International SOI Conference, 2001: 47

[9] Losavio A, Crivelli B, Cazzaniga F, et al. Oxide damage by ion implantation in silicon. Appl Phys Lett, 1999, 74(17): 2453

[10] Garrido B, Samitier J, Morante J R, et al. Configurational statistical model for the damaged structure of silicon oxide after ion implantation. Phys Rev B, 1994, 49(21): 14845

[11] Colinge J P. Silicon-on-insulator technology: materials to VLSI. 2nd edition. Kuwer Press, 1997: 129

[12] Yamaoka M, Osada K, Itoh K, et al. Dynamic-Vt, dual-power-supply SRAM cell using D2G-SOI for low-power SoC application. IEEE International SOI Conference, 2004: 109

[13] Medici, two-dimensional device simulation program. Version 4. 0, 1997

[14] Tsuprem-4, two-dimensional process simulation program. Version 6. 5, 1997

双栅动态阈值 SOI nMOSFET 数值模拟

毕津顺† 吴峻峰 海潮和

(中国科学院微电子研究所, 北京 100029)

摘要: 提出了新型全耗尽 SOI 平面双栅动态阈值 nMOS 场效应晶体管,模拟并讨论了器件结构、相应的工艺技术和工作机理. 对于 nMOS 器件,背栅 n 阱是通过剂量为 $3\times10^{13}cm^{-2}$,能量为 250keV 的磷离子注入实现的,并与 n^+ 前栅多晶硅直接相连. 这项技术与体硅工艺完全兼容. 通过 Tsuprem4 和 Medici 模拟,发现全耗尽 SOI 平面双栅动态阈值 nMOSFET 保持了传统全耗尽 SOI nMOSFET 的优势,消除了反常亚阈值斜率和 kink 效应,同时较传统全耗尽 SOI nMOSFET 有更加优秀的电流驱动能力和跨导特性.

关键词: 双栅结构; 动态阈值; 全耗尽绝缘体上硅; nMOS 场效应晶体管

EEACC: 2560

中图分类号: TN386.1 **文献标识码**: A **文章编号**: 0253-4177(2006)01-0035-06

†通信作者. Email: bravehawk@126.com

2005-05-25 收到,2005-10-09 定稿