Analysis and Design of a ΔΣ Modulator for Fractional-N Frequency Synthesis *

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Abstract: This paper presents the design considerations and implementation of a novel topology digital multi-stage-noise-shaping (MASH) delta-sigma modulator suitable for fractional-N phase-locked-loop (PLL) frequency synthesis. In an effort to reduce the complexity and dissipation, a pipeline technique has been used, and the proposed carry save tree (CST) algorithm optimizes the multi-input adder structure. The circuit has been verified through Matlab simulation, ASIC implementation, and FPGA experiment, which exhibits high performance and potential for a gigahertz range, low-power monolithic CMOS frequency synthesizer.

Key words: ΔΣ modulator; fractional-N frequency synthesis; MASH architecture
EEACC: 1230; 1250; 2570D
CLC number: TN761 **Document code:** A **Article ID:** 0253-4177(2006)01-0041-06

1 Introduction

Frequency synthesizers are widely used as local oscillators for frequency translation, which provide accurately defined frequencies and desired channel selection in wireless transceivers[1]. Standard frequency synthesizers with integer-N dividers have difficulties meeting various specifications due to their fundamental tradeoffs between loop bandwidth and channel spacing. The fractional-N approach eliminates this limitation, which allows frequency steps far smaller than the reference frequency. Therefore, the loop bandwidth can be larger, alleviating the requirements for the voltage-controlled oscillator (VCO) phase noise and the reference frequency suppression. However, the fractional division causes spurious tones at fractional multiples of the reference frequency. Several methods to overcome the spurious problem have been proposed[2,3], of which the ΔΣ fractional-N architecture seems to be widely accepted as the best one, as shown in Fig. 1. This is achieved by randomizing the feedback division ratio such that the quantization noise of the fractional-N divider is transferred to higher frequencies.

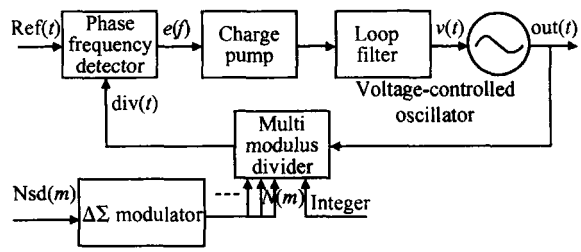

Fig. 1 FN synthesizer with ΔΣ modulator

For fractional-N frequency synthesis, two types of ΔΣ modulators have been used[4,5]. One is a single-loop modulator and the other is a cascaded modulator called the MASH architecture. The latter has the advantage that higher-order noise filtering can be achieved using lower-order modulators. The overall cascaded system should remain stable since the lower-order modulators are more stable.

This paper focuses on the MASH 2-1-1 all-digital delta sigma modulator topology design and implementation, which offers larger output dynamic range and better noise shaping performance.

* Project supported by the Shanghai AM R&D Fund (No. 0302)

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Received 27 May 2005, revised manuscript received 14 September 2005

2 The proposed ΔΣ modulator

The ΔΣ modulator is a non-linear system with a filter (digital or analog), a feedback loop, and a quantizer, which operates at an oversampled frequency. The filter in the loop attenuates the noise introduced by the quantization so that the quantization noise, which remains at the DSM output, is low compared to the DSM input signal in the band of interest. This action of shaping the quantization noise is also referred to as noise shaping[6].

In our case the input (x) is a digital word, representing the desired fractional value to synthesize. Therefore, we consider a digital equivalent to the analog ΔΣ modulator. A first-order digital ΔΣ modulator is shown in Fig. 2.

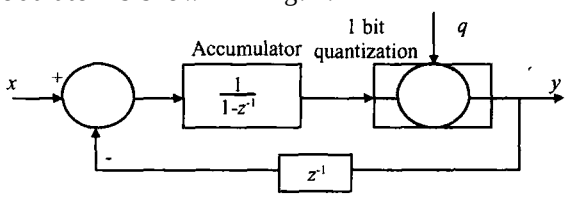

Fig. 2 Block diagram of a first-order ΔΣ modulator

The ΔΣ modulator filters differently the quantization noise (q) and the input signal (x), as illustrated by Eq. (1).

The expression of the output of the first-order ΔΣ modulator y is given by

$$\begin{aligned} Y(z) &= \frac{H_{\text{int}}}{1 + z^{-1} H_{\text{int}}} X(z) + \frac{1}{1 + z^{-1} H_{\text{int}}} Q(z) \\ &= X(z) + (1 - z^{-1}) Q(z) \end{aligned} \tag{1}$$

The signal-flow graph for this modulator in its digital implementations is illustrated in Fig. 3, where the n-bit input signal $K[n]$ is summed with the n-bit register content to produce the $(n+1)$ bit quantizer input signal $v[n]$. The 1-bit quantization process is accomplished by simply taking the most significant bit (MSB) of $v[n]$. The residual n-bit signal, which represents the negative of the quantization error signal, is then stored in the register to be summed in the next clock cycle[7].

We can deduce the frequency noise introduced by fractional division when the MASH controls the division ratio $N/(N+1)$ with $x = K/F$ and N is given. Indeed,

$$\begin{aligned} f_{\text{VCO}} &= (N_{\text{integer}} + N_{\text{fractional}}) f_{\text{ref}} \\ &= N f_{\text{ref}} + \left(\frac{k}{F} + H_{\text{noise}}(f) Q_3(f)\right) f_{\text{ref}} \end{aligned} \tag{2}$$

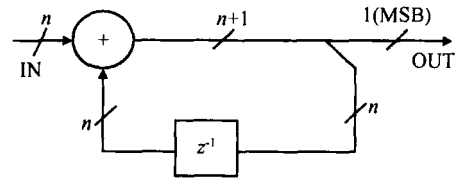

Fig. 3 Signal flow graph

The constant term $Nf_{\text{ref}} + \frac{k}{F} f_{\text{ref}}$ is removed and the fluctuating term $f_{\text{noise}}(f) = H_{\text{noise}}(f) Q_3(f) \times f_{\text{ref}}$ remains, which is the expression of the frequency fluctuation noise introduced by fractional N frequency synthesis.

A 1-bit quantizer produces a quantization q_3, uncorrelated with x. Furthermore, if q_3 is assumed to be a uniformly distributed white-noise sequence, the mean of q_3 is zero and the variance is $\sigma_{q_3}^2 = \frac{\Delta}{12}$, with $\Delta = 1$[2]. As the power is spread over the bandwidth f_{ref}, the power spectral density (PSD) of the quantization error q_3 is $\frac{\sigma_{q_3}^2}{f_{\text{ref}}} = \frac{1}{12 f_{\text{ref}}}$. This enables us to write the expression of the frequency fluctuation f_{noise} as

$$S_{f_{\text{noise}}} = |H_{\text{noise}}(f) f_{\text{ref}}|^2 \frac{1}{12 f_{\text{ref}}} = \frac{|1 - z^{-1}|^6 f_{\text{ref}}}{12} \tag{3}$$

In terms of noise contribution, the noise expression is more relevant than the frequency noise expression. Phase and frequency are related by integration as $\phi = \int 2\pi f_{\text{instantaneous}} \, dt$[2]

$$\begin{aligned} S_{\phi, N \leftarrow N+1}(z) &= S_{f_{noise}} S_{integration} \\ &= \frac{|1 - z^{-1}|^6 f_{ref}}{12} \times \frac{(2\pi)^2}{|1 - z^{-1}|^2 f_{\text{ref}}^2} \\ &= \frac{(2\pi)^2}{12 f_{\text{ref}}} |1 - z^{-1}|^4 (\text{rad}^2 \cdot \text{Hz}^{-1}) \end{aligned} \tag{4}$$

Replacing z by $e^{\frac{2\pi f}{f_{\text{ref}}}}$, we get

$$S_{\phi, N \leftarrow N+1}(z) = \frac{(2\pi)^2}{12 f_{\text{ref}}} \left|2 \sin \frac{\pi f}{f_{\text{ref}}}\right|^4 \tag{5}$$

The transition is generalized to n-order DSM output and results in the phase noise contribution:

$$S_{\phi, N \leftarrow N+1}(z) = \frac{(2\pi)^2}{12 f_{\text{ref}}} \left|2 \sin \frac{\pi f}{f_{\text{ref}}}\right|^{2(n-1)} \tag{6}$$

When $f \ll f_{\text{ref}}$, Equation (6) is approximated as

$$\lim_{x \to 0} \sin x \approx x,$$

$$S_{\phi, N \leftarrow N+1}(f) \approx \frac{(2\pi)^2}{12 f_{\text{ref}}} \left|2\pi \frac{f}{f_{\text{ref}}}\right|^{2(n-1)} \tag{7}$$

When a MASH structure controls the fractional frequency division, the quantization noise is

shaped as shown in Eq. (7). Higher frequencies components are then removed by the low-pass characteristic from the PLL. The spurious performance is improved.

As may be concluded from Eq. (7) ,the degree of noise shaping is directly related to the order of the delta-sigma modulator used.

The first-order DSM presents strong idle tones for DC inputs. With a second-order modulator in the first stage ,there is a smaller amount of noise in band to be MASH structure. Even when some of the modulator noise is not properly cancelled by the following stages in the MASH , the noise leakage has a second order shaping characteristic. Therefore a second-order modulator is better suited for the first stage of the MASH structure. In general ,we first place all the second order modulators to obtain a strong noise shaping within the first stages. Due to potential imperfect cancellation and the stability of the loop ,in practice the number of stages is often limited to 4. A detailed stability analysis of the chosen MASH modulator has been performed. When the outside temperature and power voltage change ,the loop demonstrates good stability. Scaling factors are introduced between stages ,and additives poles may be placed in each second order stage to insure stability of the MASH structure[8] . From the above considerations ,MASH 2-1-1 has been chosen to be the right structure , which is illustrated in Fig. 4.

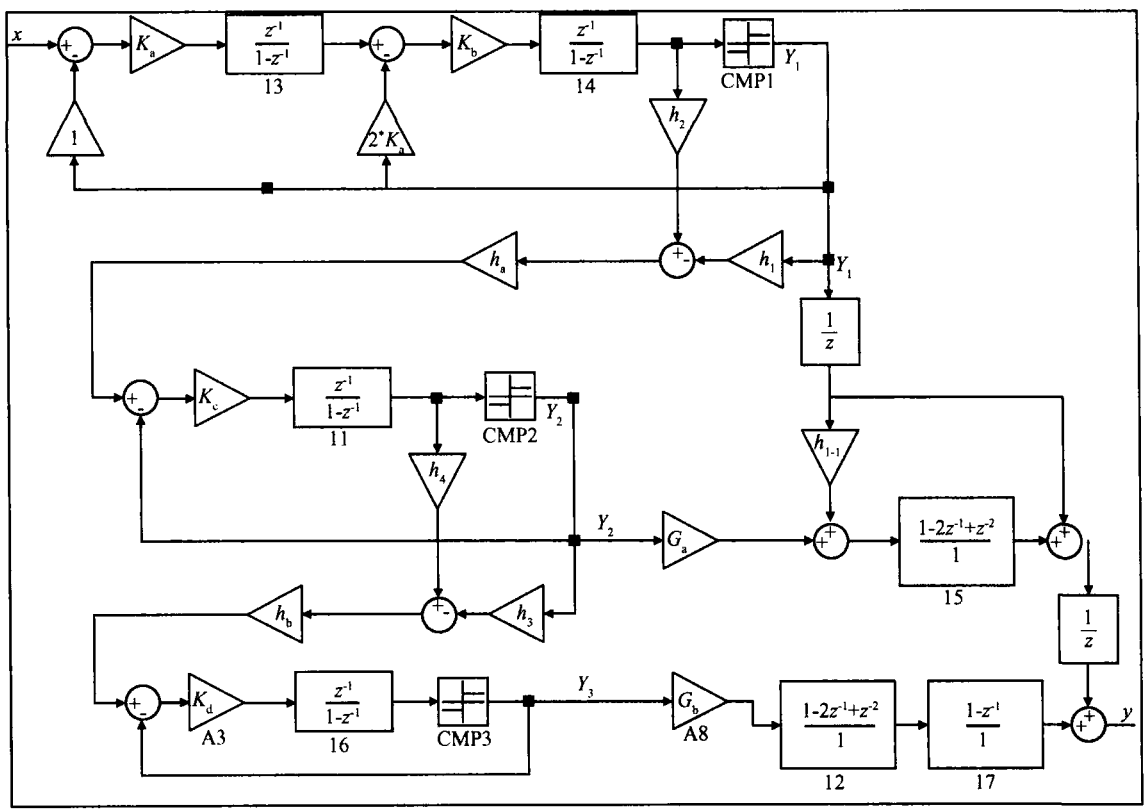

Fig. 4 Diagram of MASH 2-1-1

The poles and scaling factor in the noise transfer function of the second order stages ensure the stability of the system ,without modifications of the frequency characteristic of the signal transfer function. The choice of the scaling factors and poles is a compromise between SNR and stability requirements. If the scaling factors are chosen as powers of 2 ,the divisions and multiplications by 2 are implemented with bit shifters. The scaling factors limit the internal signal amplitude and maintain the input of the quantizer in a bounder range of values resulting in a bounded value for the quantization noise in each stage. If the input scaling factors are chosen to be too large ,the cascade of stages may

lead to large amplitude signals with strong tones in the noise spectrum.

Through the noise cancel network, the optimization scaling factors are chosen: $K_a = 1/3$, $K_b = 3/5$, $K_c = K_d = 1/3$, $h_1 = 3$, $h_2 = 5$, $h_3 = 1$, $h_4 = 3$, $G_a = G_b = 2$. The output of the modulator is

$$Y(z) = z^{-4} X(z) + (1 - z^{-1})^{-4} G_b E_3(z) \quad (8)$$

3 Implementation of the 2-1-1 MASH

In this design, a fourth-order MASH 2-1-1 $\Delta\Sigma$ modulator is used to randomize the instantaneous division ratio of MMD (multi-modulus-divider) such that the spur noise contributed by the divider is shaped to high frequencies, which in turn can be filtered by the loop filter. The input bit length of the modulator is chosen as 24bits, which leads to a frequency resolution[6] smaller than 10kHz when the reference frequency is set to 13MHz, which can fully cover the requirement of the GSM applications.

A pipelining technique is used to speed up the $\Delta\Sigma$ modulator even further, for two reasons. First, it enables an even higher reference frequency to be used during testing to determine the effect of increasing the reference frequency on the phase noise performance of the $\Delta\Sigma$ PLL. Second, it enables the $\Delta\Sigma$ modulator to work at lower supply voltages while still operating at 13MHz. This helps to reduce the power consumption of the $\Delta\Sigma$ modulator. Figure 5 illustrates the circuit realization of the MASH architecture.

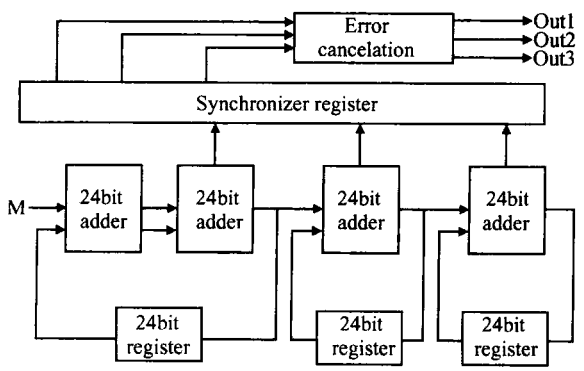

Fig. 5 Implementation of the fourth-order MASH modulator

Each accumulator employs a pipelined 24bit adder and a 24bit register. It can be seen that there is a long delay chain between the accumulator overflow outputs; therefore, they appear at different time instances. To provide synchronization among the carry overflows, they are captured in 1bit registers before being forwarded to the error cancellation network. The network performs the specific function of canceling the quantization error from the first two stages and produces a 3bit output.

A 24bit adder can be easily realized by using 24 full-adder (FA) logic circuits connected in cascade. The key block in the proposed $\Delta\Sigma$ modulator is the multi-input adder. Optimizing this adder structure is pivotal in decreasing the area and power consumption of the entire PLL. In this study, a multi-input addition algorithm is proposed which is capable of adding several operands without sign extension. Several algorithms have been proposed in the literature which is optimized specifically for the case of adding hr partial products of a multiplier[9]. However, in the new proposed algorithm, the most significant bit (MSB) of each operand is given a negative weight. Adding the MSB of an operand to another number would be the same as subtracting the MSB from the other number. Four different cells are possible depending on the number of negatively weighted inputs.

$$\begin{aligned} (C,S) &= X + Y + Z \\ (C,-S) &= -X + Y + Z \\ (-C,S) &= -X - Y + Z \\ (-C,-S) &= -X - Y - Z \end{aligned} \quad (9)$$

where X, Y, and Z are the inputs of each cell, and C and S are the carry-and-sum outputs of the adder cells. Note that the fist and last equations are implemented in the same circuit. This means that two's complement addition of several operands is possible using only three cells in the carry save tree (CST). Using the type of arithmetic illustrated in Eq. (9), the number of required cells was reduced by more than half in comparison to a sign extension solution. This greatly aids in reducing the area and power dissipation of the digital $\Delta\Sigma$ modulator.

Equation (10) depicts the logic diagram of the error cancellation network used in the realization of Fig. 5. The error cancellation network basically performs the following function

$$\begin{aligned} Y[n] = {} & X_3[n] - 2C_3[n-1] + C_3[n-2] + \\ & C_2[n] - C_2[n] - C_2[n-1] + C_1[n] \end{aligned} \quad (10)$$

where C_i represents the carry outs of the ith accu-

mulators.

The output of the MASH is a signed multi-bit number, since the 3bit two 's complement system covers the number levels between - 4 and + 3, while the 2-1-1 MASH produces output levels between - 3 and + 4. To eliminate one additional bit coding at the output, we have coded the output level + 4 as - 4. The coding table of the MASH output and the corresponding levels are shown in Table 1.

Table 1 Coding table for the MASH output

Output level	Out3	Out2	Out1
- 3	1	0	1
- 2	1	1	0
- 1	1	1	1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0

4 Simulation and experimental results

A VHDL implementation of the architecture of Fig. 5 has been undertaken, and the final design was targeted to an FPGA device provided by Altera™ where the EPIS80B95616 device was chosen to fit the design. The clock was generated from a high quality Hewlett Packard pulse generator model No. 81130A, and the data was measured with a Tektronix TLA713.

The MASH modulator was simulated for all possible values of static input K, and no tones in the whole spectrum were observed. For instance, the modulator output noise spectra for a decimal input 3172232, which corresponds to 0. 330548333161 as a fraction, is shown in Fig. 6 (a), where a clock frequency of 13MHz was used. The spectrum was obtained by Hanning windowed 2^{18}-point FFT data that was normalized to the single-bit quantization step size, which in our case was one. The power spectral density of the quantization noise was measured, for a 13MHz clock rate, by capturing the output bitstream of the modulator for a fixed input word. The bitstream was acquired using a computer card developed specifically for the purpose of sampling bits at a desired synchronized clock frequency. The bit sampler sampled the bits and stored them in a RAM buffer. The bitstream file was processed to perform a DFT to generate and scale the power spectral density, in the same manner as was done for the simulation result. Figure 6 (b) shows the result of the measurement. Both the structural bit-level simulation and measurement results in Fig. 6 confirm the 80dB per decade increase in the spectrum, validating the fourth-order noise shaping. Furthermore, for 2^{18} samples of modulator output, the fraction was represented to an accuracy of 99. 696 %. For the extreme high and low values of the input, the modulus controller noise shaping deteriorates. It is found that the maximum range is 893689, which is 80 % of the total range. The Hspice simulation shows (Table 2) that the power the static adder consumes is twice that of the TSPC register. Through the CST algorithm, which reduces the size of the adder structure by 40 % and adds to the size of the register by 20 %, the final measurement demonstrates that the power consumption is only 2. 68mW.

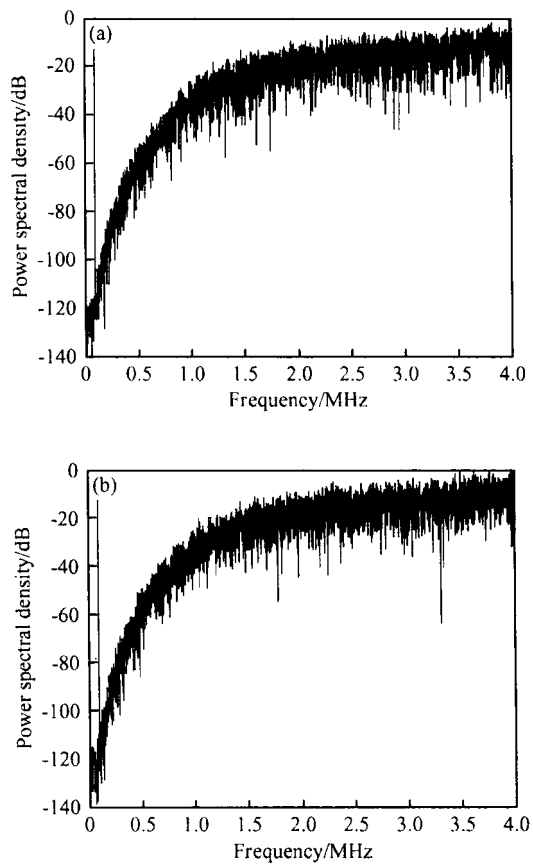

Fig. 6 Output noise spectra of the modulator (a) Structural simulation; (b) FPGA measurement

Table 2 Energy consumption of blocks

Component	Energy consumption
Static adder	0.150fJ/operation
Noninverting TSPC register	0.075fJ/operation

It is also worth noting that DC inputs are the worst case inputs for a ΔΣ modulator, and thus the output spectrum consists of pure tones and oscillations even when the order of the system is high.

The circuit has also been implemented in ASIC full custom design, from the RTL to the layout design, together with a programmable multi-modulus divider ranging from 18500 to 19900 and other blocks to implement a monolithic CMOS F-N PLL frequency synthesis which works at 3700 ~ 3840MHz E-GSM Standard.

5 Conclusion

The choice of an appropriate high order ΔΣ structure requires the consideration of many factors, including noise shaping, spurious content of the output bit number, and circuit complexity. A fourth-order MASH structure was designed and implemented which allows for the input to operate over 80 % of the input adder capacity. Simulations and measurement results confirm the suitability of the proposed architecture for low-power CMOS implementation of gigahertz range frequency synthesizers.

Acknowledgements The authors gratefully acknowledge beneficial cooperation with colleagues in the ASIC & system State-key Laboratory of Fudan University.

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ΔΣ 调制器在分数分频频率综合器中的分析与设计 *

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摘要: 提出了一种适用于分数分频锁相环频率综合器的全数字噪声整型 ΔΣ 调制器电路结构新的设计方法,并将其最终实现. 采用了流水线技术和新的 CST 算法优化多位输入加法器结构,从而降低了整体的复杂度和功耗. 这种电路结构通过了 Matlab 的行为级仿真,ASIC 全定制实现并流片,该结构也通过 VHDL 综合实现验证,最后给出的测试结果表明该电路具有良好的性能,可应用于单片千兆赫兹级低功耗 CMOS 频率综合器中.

关键词: ΔΣ 调制器; 分数分频频率综合器; 噪声整型结构
EEACC: 1230; 1250; 2570D
中图分类号: TN761 **文献标识码**: A **文章编号**: 0253-4177(2006)01-0041-06

* 上海应用材料研究与发展基金资助项目(批准号:0302)

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2005-05-27 收到,2005-09-14 定稿