A 12-Channel ,30 Gb/ s ,0. 18μm CMOS Front-End Amplifier for Parallel Optic-Fiber Receivers *

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Abstract: This paper presents a 12-channel ,30 Gb/ s front-end amplifier realized in standard 0. 18μm CMOS technology for parallel optic-fiber receivers. In order to overcome the problem of inadequate bandwidth caused by the large parasitical capacitor of CMOS photo-detectors ,a regulated-cascode structure and noise optimization are used in the design of the transimpedance amplifier. The experimental results indicate that ,with a parasitical capacitance of 2pF , a single channel is able to work at bite rates of up to 2. 5Gb/ s ,and a clear eye diagram is obtained with a 0. 8mV_{pp} input. Furthermore ,an isolation structure combined with a p^+ guard-ring (PGR) ,an n^+ guard-ring (NGR) ,and a deep-n-well (DNW) for parallel amplifier is also presented. Taking this combined structure ,the crosstalk and the substrate noise coupling have been effectively reduced. Compared with the isolation of PGR or PGR + NGR ,the measured results show that the isolation degree of this structure is improved by 29. 2 and 8. 1dB at 1GHz ,and by 8. 1 and 2. 5dB at 2GHz ,respectively. With a 1. 8V supply ,each channel of the front-end amplifier consumes a DC power of 85mW ,and the total power consumption of 12 channels is about 1W.

Key words: parallel optic-fiber receiver; front-end amplifier; regulated-cascode; substrate noise coupling; isolation

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1 Introduction

As tele- and data-communications are rapidly developing ,optic-fiber networks are being widely implemented. The continuous increase in transmission speed has motivated the design and implementation of high speed , high capacity optic-fiber networks. These performances can be satisfied by parallel optic-fiber transmission systems.

Our 30Gb/ s parallel optic-fiber receiver consists of 12 channels with 2. 5Gb/ s per channel. Each channel includes a front-end amplifier combined with a trans-impedance amplifier (TIA) followed by a limiting amplifier (LA). At such a high bit rate ,the amplifier can be manufactured easily by using a GaAs or a silicon bipolar technology , but with a higher cost. Advanced CMOS technologies are attractive from the standpoints of integration ,power ,and cost. With the feature size scaling down to 0. 18μm and below ,CMOS technology is becoming the most interesting process for optic-electronic integrated circuits. So our 12-channel , 30Gb/ s parallel front-end amplifiers are designed in 0. 18μm CMOS technology.

2 System structure

As shown in Fig. 1 ,our 30Gb/ s parallel optic-fiber receiver includes 12 parallel channels with each channel working at 2. 5Gb/ s. The system consists of a micro-optics module ,12 parallel photodetectors (PD) , and 12 parallel front-end amplifiers[1]. The micro-optics module couples the optical signals from 12 parallel optic-fibers to 12 parallel PDs. The parallel PDs convert the optical signals into electrical ones. The parallel front-end amplifiers amplify the small signals from the PDs with a high enough gain but a low noise factor.

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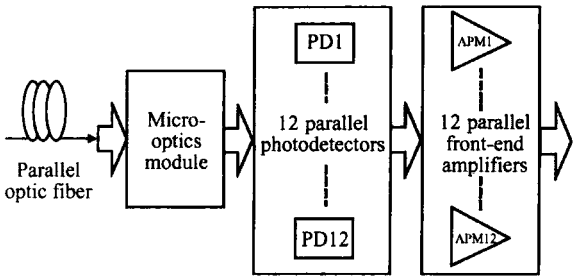

Fig. 1 Parallel optic-fiber receiver structure

3 Design of parallel front-end amplifiers

There are 12 front-end amplifiers in parallel. Each amplifier consists of a TIA, a single-end to differential converter, and an LA, as shown in Fig. 2, where I_{PD} is the output current of the PD, and C_{PD} is the parasitical capacitance of the PD. The TIA converts the weak current detected by the PD into a voltage signal. The LA amplifies the voltage signal of TIA and boosts the signal swing to logical levels.

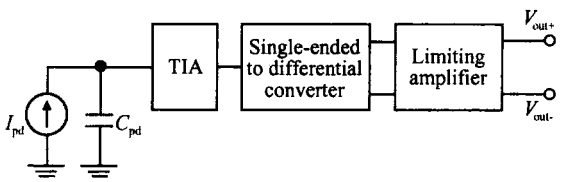

Fig. 2 Principle diagram of front-end amplifier

Twelve parallel front-end amplifiers in CMOS technology share a single silicon substrate, and the signal of one amplifier enters another amplifier by substrate noise coupling. Interference or crosstalk occuring between these amplifiers exacerbate the sensitivity of the receiver. To decrease the interferences between amplifiers, their isolation structures are designed carefully. The design methods of the preamplifier, the single-end to differential converter, and the LA are given in the following sections, and the isolation structures are also discussed.

3.1 Design of TIA

The output current from a PD is very weak, on the order of a microampere. To amplify this weak current, the TIA must be optimized for minimal equivalent input noise current to achieve maximal sensitivity. The bandwidth of the amplifier is determined by the data rate with consideration to the influences of noise, inter-symbol interference, and jitter on signals. A smaller bandwidth corresponds to a smaller noise, but to a bigger inter-symbol interference. The choice of bandwidth is a trade-off between the noise and the inter-symbol interference. The bandwidth is chosen at 0.8 times the data rate[2]. With consideration of the parasitical parameters of CMOS technology, the bandwidth of the design is normally greater than this value. The TIA must have a high enough gain to amplify the signal and restrain the noise of the following circuits.

The basic circuit of the TIA is shown in Fig. 3[3]. The feedback resistor R_f is used for providing the voltage shunt negative feedback and realizing high gain, wide bandwidth, and wide dynamic range. The bandwidth can be expressed by

$$BW = 1/2\pi R_{in} C_{in} \quad (1)$$

where R_{in} is the input resistance of the TIA, and C_{in} is the total input capacitance combined with C_{PD} and the input capacitor of the amplifier.

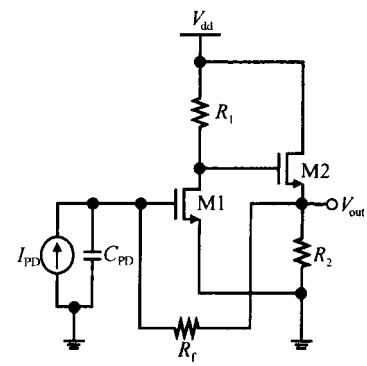

Fig. 3 Circuit diagram of the TIA

The PD in CMOS technology has greater size than the one in GaAs or InP technology. It shows therefore a larger C_{pd}. Along with the transistor's capacitance and the parasitical capacitance, C_{in} reaches about of 2pF. As the basic TIA has a large input resistance, assuming that R_{in} is about 100Ω, BW is 2GHz, and the calculated value of C_{in} is equal to 0.8pF which is much smaller than the total input capacitance of 2pF. Therefore, the TIA shown in Fig. 3 does not satisfy the bandwidth requirement, and another TIA structure must be developed.

A regulated cascode (RGC) input configuration[4] is used for the TIA as shown in Fig. 4. The first stage is an RGC input configuration that includes a common gate amplifier combined with R_1, M1, and R_s, and a common source amplifier combined with R_B and MB. The second stage is a TIA that includes a source follower combined with M2 and R_2, a common source amplifier combined with M3 and R_3, and another source follower combined

with M4 and R_4. The RGC circuit has two advantages: The first is that the RGC circuit has a very stable DC bias. For example ,if the current of M1 increases ,then the voltage at node 2 increases ,and the current of MB increases. Therefore the voltage of node 1 decreases ,thereby constraining the increase of current in M1 and enhancing the circuit stability. The second advantage is that the RGC circuit has a very low R_{in} , $R_{in} = 1/ g_{M1} (1 + g_{MB} R_B)$, resulting in a wider bandwidth and a higher feedback resistance when compared with the TIA shown in Fig. 4. Figure 5 shows the input resistance of an RGC-type TIA.

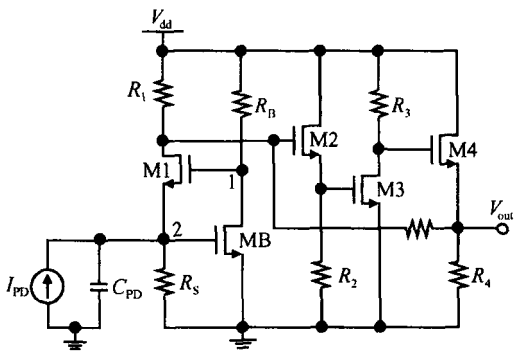

Fig. 4　RGC-type TIA

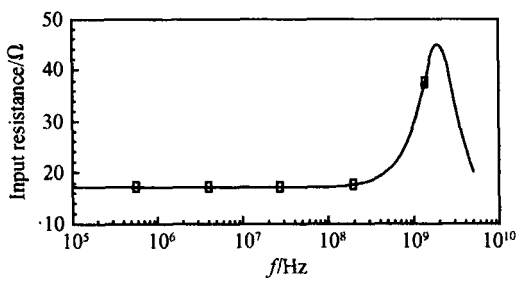

Fig. 5　Input resistance of RGC-type TIA

To achieve a low noise level ,the RGC TIA must be optimized to have a minimal equivalent input noise current which is determined mostly by the RGC input configuration and is expressed as follows[4].

$$\langle \overline{i_{eq}^2} \rangle = \overline{i_{nRs}^2} + \overline{i_{n1}^2} + \overline{i_{nB}^2} + \overline{i_{nR1}^2} + \overline{v_{nB}^2} \left| \frac{1}{R_S} + j\omega C_{tot} \right|^2$$

$$= \frac{4kT}{R_S} + 2qI_{g1} + 2qI_{gB} + \frac{4kT}{R_1}$$

$$+ \frac{8kT}{3g_{MB}} \left[\frac{1}{R_S^2} + \omega^2 (C_{PD} + C_{gsB} + C_{gdB} + C_{gs1})^2 \right] \quad (2)$$

From Eq. (2) ,the noise optimization methods are described as follows.

(1) To decrease the equivalent input noise current , R_1 and R_S should be increased;

(2) The gate-width of MB (W_{MB}) should be optimized.

Figure 6 shows the equivalent input noise current spectral density of the RGC TIA as a function of W_{MB} at 2 GHz with a total input capacitance of 2pF for a fixed feedback resistor of 1kΩ. The optimum W_{MB} was found to be 437μm with a minimal equivalent input noise current of about 12. 2pA/ $\sqrt{\text{Hz}}$. The equivalent input noise spectral density has been improved by 6pA/ $\sqrt{\text{Hz}}$ at the frequency of 2 GHz by the optimization as shown in Fig. 7.

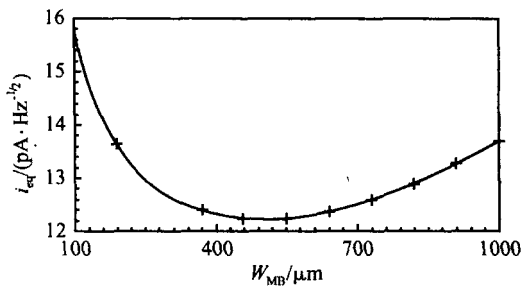

Fig. 6　Equivalent input noise current spectral density as a function of the gate width W_{MB}

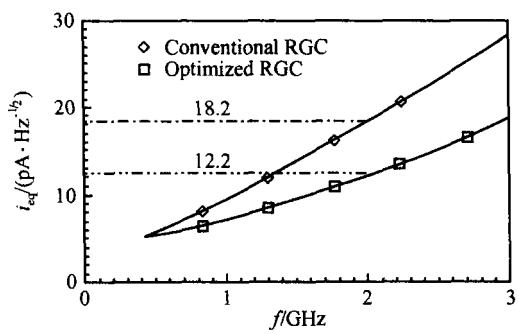

Fig. 7　Comparison of optimized RGC and conventional RGC in noise performance

3.2　Design of single-end to differential converter

Because the TIA has a single-ended output and the LA has differential inputs ,a single-end to differential converter ,as shown in Fig. 8 is needed between the TIA and LA. This circuit could hold the same DC bias on the inputs of the differential amplifier and transform the single-ended input into the differential outputs.

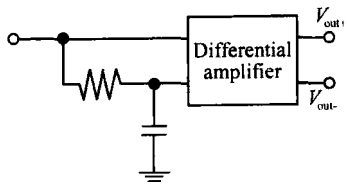

Fig. 8 Single-end to differential converter

3.3 Design of limiting amplifier

The function of the LA is to hold the output signal to a limiting-amplitude state, once the amplitude of input signal exceeds a defined voltage. Besides high speed and high gain, the LA must hold an invariable output voltage in a large dynamic input range. Figure 9 shows the LA structure, which contains three broad-band amplifiers, an output buffer, and a DC feedback network. Furthermore, the full differential structure of the LA could reduce the interferences caused by the variation of the power voltage and temperature. In order to improve the bias stability and reduce the crosstalk among stages, we adopt direct coupling among stages and provide independent bias for different stages.

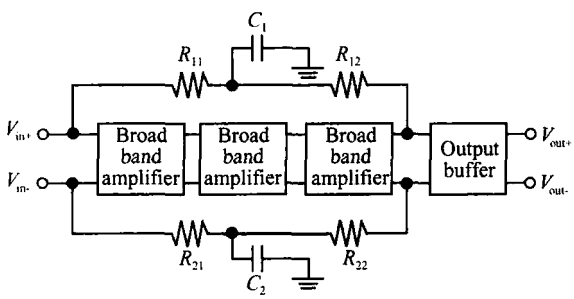

Fig. 9 Limiting amplifier structure

Due to the high-gain and direct coupling, a small voltage offset at the input could cause the output stage to saturate and even make the circuit lose the function of limiting amplifying. The DC feedback networks, which include R_{11}, R_{12}, R_{21}, R_{22}, C_1, and C_2, are used to make the circuit stable.

3.4 Isolation design of parallel front-end amplifiers

Some isolation methods, such as a p^+ guard ring (PGR) or an n^+ guard-ring (NGR)[5], have been used to protect CMOS devices. Both of them only surround the devices on the sides and cannot cover the bottom of the devices. Though most of the substrate coupling noise can be absorbed by the surrounding PGR or NGR, part of substrate coupling noise can be coupled through the bottom of the CMOS devices.

As for the isolation design of the parallel front-end amplifier, we can use the PGR or a combination of PGR and NGR to surround each front-end amplifier of the 12 channels, as shown in Figs. 10 and 11. The bottom of the amplifier is uncovered, so the substrate noise can be coupled into each amplifier through the bottom. In order to enhance the isolation of each amplifier, a new isolation structure is shown in Fig. 12. This structure, combined with PGR, NGR, and DNW, is used to shield each amplifier from the substrate noise. The PGR is connected to ground. The NGR is connected to V_{dd} and is used to surround the PGR to form reverted p-n junctions respectively with p-well and p-sub. The DNW is buried deeply in the substrate and connected to the NGR. Thus the reverted p-n junction between the p-well and the DNW, and the reverted p-n junction between the p-sub and the DNW are formed. The PGR and

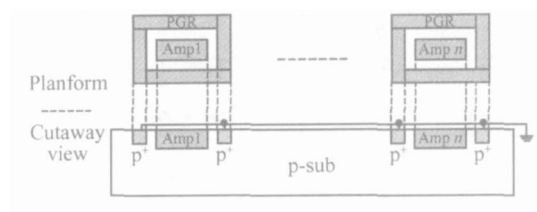

Fig. 10 PGR isolation structure

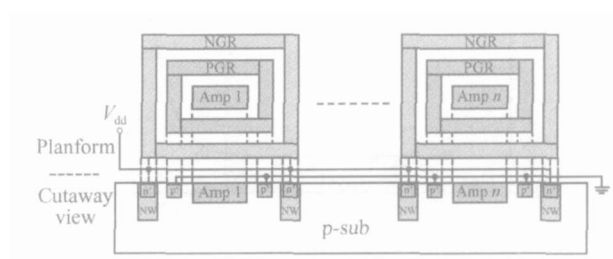

Fig. 11 PGR + NGR isolation structure

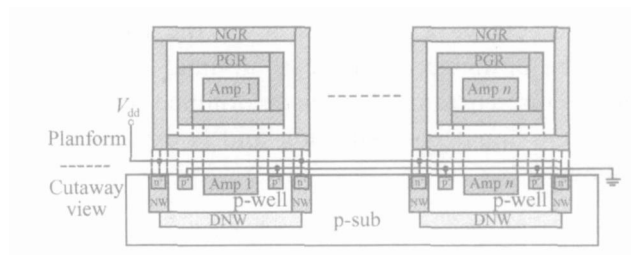

Fig. 12 PGR + NGR + DNW isolation structure

the NGR could interdict the side coupling pass ,and the DNW could interdict the bottom coupling pass. Compared with other isolation structures , this structure improves the isolation performance between front-end amplifiers.

4　Chip fabrication

The 12-channel parallel front-end amplifiers for parallel optical receivers are designed and fabricated in standard 0. 18μm CMOS technology as shown in Fig. 13. The chip has dimensions of 3. 75mm ×0. 62mm = 2. 325mm^2 , and each front-end amplifier has the same circuit structure and layout. In order to compare the performances of different isolation structures ,three types are presented: (1) The use of PGR only; (2) The use of a combination of PGR and NGR; (3) The use of a combination of PGR ,NGR , and DNW.

Fig. 13　Microphotograph of 12 parallel front-end amplifiers

5　Measured results

Together with a pulse pattern generator (Advantest D3186) ,a digital sampling scope (Agilent 86100A) ,a cascade probe station and 40 GHz microwave probes ,the chip is measured and performs well in on-chip testing. With a 1. 8V power supply , each front-end amplifier consumes 85mW. The total power consumption of 12 front-end amplifiers is about 1. 02W.

5. 1　Measurements of single front-end amplifier

Two eye diagrams are shown in Figs. 14 (a) and (b) with a 2. 5 Gb/ s 2^{31} - 1 pseudorandom bit sequence (PRBS) signal at the input , which are measured with two voltage amplitudes of 2 and 0. 8mV$_{pp}$ at input. Some typical measurement results are listed in Table 1. The eyes are clear without any noise points in them. Both eyes angle and eyes height are large. Very little intersymbol interference (ISI) is present in the eyes and the measured RMS jitter proportion is less than 0. 03UI (unit interval).

Table 1　Measurement results of single front-end amplifier

Parameter	Value
Technology	0. 18μm CMOS
Supply voltage	1. 8V
Data rate	2. 5 Gb/ s
RMS jitter	11ps at 2mV$_{pp}$ 20ps at 0. 8mV$_{pp}$
Rise/ Fall time	100ps/ 101ps at 2mV$_{pp}$
Single-end output swing	288mV
Power dissipation	85mW

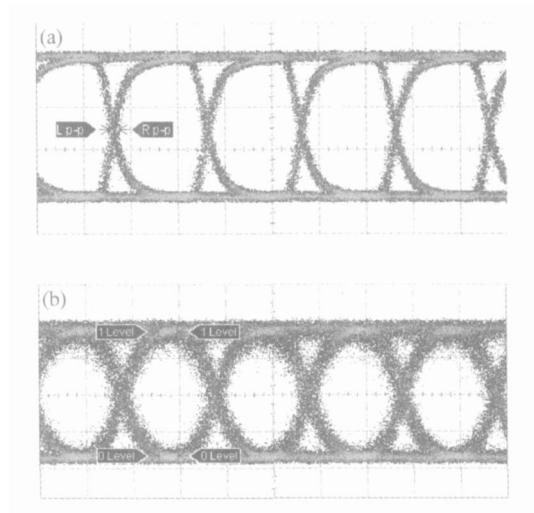

Fig. 14　(a) Output eye diagram with 2mV$_{pp}$ at 2. 5 Gb/ s; (b) Output eye diagram with 0. 8mV$_{pp}$ at 2. 5 Gb/ s

5. 2　Measurements of two adjacent front-end amplifiers

In order to measure the crosstalk of two adjacent front-end amplifiers , two 2. 5 Gb/ s 2^{31} - 1 PRBS signals with 2mV$_{pp}$ are input in two adjacent front-end amplifiers isolated by the PGR + NGR + DNW structure ,and their output eye diagrams are shown in Fig. 15. Some typical measurement re-

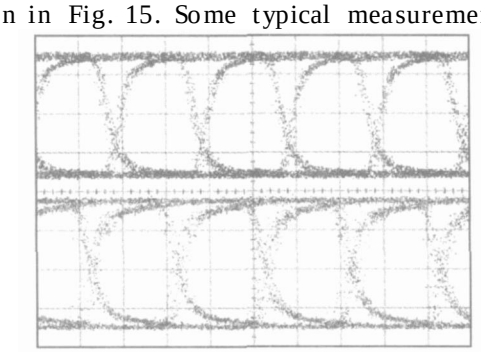

Fig. 15　Output eye diagrams of two adjacent front-end amplifiers

sults are shown in Table 2. Compared with the output eye diagrams of a single front-end amplifier (shown in Fig. 14(a)), the output eye diagrams of two adjacent front-end amplifiers are very clear without obvious crosstalk. The following measurement results show that the PGR + NGR + DNW structure isolates the parallel front-end amplifiers effectively.

Table 2 Measurement results of two adjacent front-end amplifiers

Number	Input voltage	Jitter	Single-ended output swing
1	$2mV_{pp}$	11ps	288mV
2	$2mV_{pp}$	11ps	286mV

5.3 Isolation measurement of parallel front-end amplifiers

The input voltage of amplifier n is represented by V_{n1}, and the output voltage of amplifier m is V_{m2}. Then the isolation degree of amplifier m to amplifier n is defined as $I_{nm} = 20\lg(V_{n1}/V_{m2})$ when other ports are matched. The higher the magnitude of I_{nm} is, the better the isolation degree will be. When a small sine signal is applied to the input of amplifier n, and the output signal of amplifier m is measured, then I_{nm} can be calculated. An HP8593A spectrum analyzer is used to measure output signal amplitude at frequencies of 155MHz, 622MHz, 1GHz, 1.25GHz, 2GHz, 2.5GHz, 2.655GHz, and 3.318GHz, generated by the R&S SMP04 Signal Generator. The measured isolation degrees are listed in Table 3 and a comparison of different isolation curves is shown in Fig. 16.

Table 3 Measured results of isolations for different structures

Frequency	PGR / dB	PGR + NGR / dB	PGR + NGR + DNW / dB
155MHz	41.5	67.4	66.2
622MHz	30.2	39.6	53.9
1GHz	23.2	44.3	52.4
1.25GHz	32.2	45.4	49.3
2GHz	34.8	40.4	42.9
2.5GHz	37.6	46.9	51.4
2.655GHz	44.8	49.6	59.4
3.318GHz	51.8	57	59.2

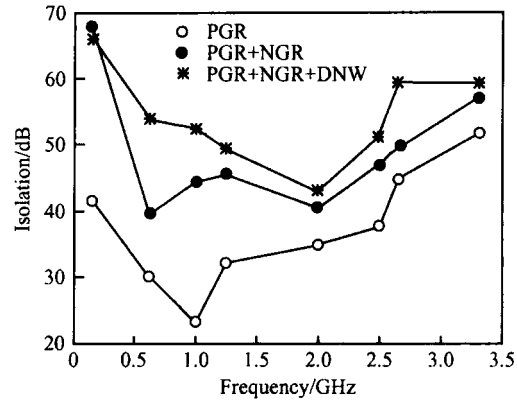

Fig. 16 Isolation curves of different structures as function of frequency

At the frequencies of 1.25 and 2.5GHz, the PGR + NGR + DNW structure improves the isolation degree by 29 and 8dB respectively over PGR isolation structure. It also improves the isolation degree by 8 and 2.5dB, respectively, over the PGR + NGR isolation structure. This shows that the combination structure of PGR, NGR, and DNW has the best isolation among these three structures.

6 Conclusion

This paper presents a 12-channel, 30Gb/s front-end amplifier designed and fabricated in standard 0.18μm CMOS technology for parallel optic-fiber receivers. The RGC structure and noise optimization are used in the design of the TIA, which overcomes the problem of inadequate bandwidth caused by the large parasitical capacitor of CMOS PD, and makes the front-end amplifiers monolithically integrated with CMOS PDs into reality. An isolation structure combined with PGR, NGR, and DNW for parallel amplifiers is also presented, which effectively decreases the substrate noise coupling and the crosstalk between the parallel amplifiers, and achieves good isolation performance. The measured results show that this chip has the merits of low noise, low cost, low power consumption and monolithic integration, and can be used in ultra high speed parallel optic-fiber communication systems.

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12 路并行 30 Gb/ s 0. 18μm CMOS 光接收前端放大器 *

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摘要: 给出了一个采用 TSMC 0. 18μm CMOS 工艺设计并实现的 12 路 30 Gb/ s 并行光接收前端放大器. 电路设计采用 RGC 结构和噪声优化技术,克服了 CMOS 光检测器大寄生电容造成的带宽不够的问题. 测试结果表明,在 2pF 的寄生电容下单信道传输速率达到了 2. 5 Gb/ s,在 0. 8 mV_{pp} 输入下得到了清晰的眼图. 提出了一种同时采用 p^+ 保护环(PGR)、n^+ 保护环(NGR)和深 n 阱(DNW)的并行放大器隔离结构,有效地抑制了并行放大器之间的串扰,减小了放大器之间的衬底耦合噪声. 测量结果表明,这种结构与 PGR 和 PGR + NGR 相比,在 1 GHz 时放大器之间的隔离度分别提高了 29. 2 和 8. 1 dB,在 2 GHz 时放大器之间的隔离度分别提高了 8. 1 和 2. 5 dB. 芯片采用 1. 8 V 电源供电,单路前端放大器的功耗为 85 mW,12 路总功耗约为 1 W.

关键词: 并行光接收; 前端放大器; RGC 结构; 衬底噪声耦合; 隔离

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