Elmore Delay Estimation of Two Adjacent Coupling Interconnects *

Dong Gang†, Yang Yintang, and Li Yuejin

(*Key Laboratory of Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, Microelectronics Institute, Xidian University, Xi'an 710071, China*)

Abstract: An approach for analyzing coupling RC interconnect delay based on "effective capacitance" is presented. We compare this new method to the traditional method, which uses Miller capacitance. The results show that the new method not only improves the accuracy but also reflects the delay dependence on rise time. The method has the same complexity as the Elmore delay model and can be used in performance-driven routing optimization.

Key words: capacitance extraction; coupling RC interconnect; effective capacitance; delay
EEACC: 7410D; 5120
CLC number: TN405.97 **Document code:** A **Article ID:** 0253-4177(2006)01-0054-05

1 Introduction

It is accepted that interconnect delay dominates gate delay in present deep submicrometer VLSI circuits[1]. The transition to submicron technology has increased coupling effects between interconnects. The delay resulting from the coupling capacitance between lines is too serious to be ignored. Some earlier works[2,3] give closed estimation of crosstalk noise, but an analytical delay calculation for a general interconnect structure with a coupling capacitance is absent from the literature.

The Elmore delay model is widely used in static calculation and design optimization, but it cannot be applied directly when coupling capacitance is present. This paper presents an approach to analyze coupling RC interconnect delay based on "effective capacitance". We compare this new method to the traditional method, which uses Miller capacitance.

2 Analytical capacitance formula

The coupling capacitance has a greater effect on the signal characterization when the capacitance of the line to the ground plane decreases. Numerical methods can accurately calculate interconnect capacitance using finite element methods, but are too time consuming for performance-driven layout synthesis.

Simple expressions were derived for the coupling and total capacitance of two parallel lines with the same geometry parameter, as shown in Fig. 1, where W is the width of the line, T is the thickness of the line, S is the space between the two lines, and H is the height of the lines above the ground plane.

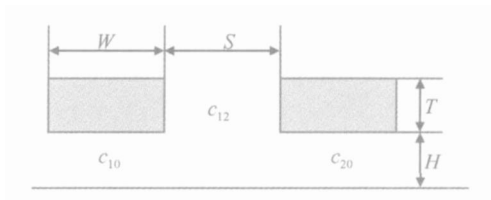

Fig. 1 Two adjacent coupling lines

Several accurate formulas have been derived in the past for line capacitance. However, due to the shrinking of geometries and the increase of line aspect ratios in state of the art technology, these formulas are no longer valid and yield inaccurate estimates. As given in Ref. [4], the capacitance to the ground of the signal line structures can be expressed as

* Project supported by the Advanced Research Foundation for the National Defense of China (No. 41323020204)
† Corresponding author. Email: donggang1978@hotmail.com
Received 18 July 2005, revised manuscript received 23 September 2005

$$\frac{c_{10}}{\varepsilon_{ox}} = \frac{c_{20}}{\varepsilon_{ox}} = 1.11\frac{W}{H} + \left[0.79\left(\frac{W}{H}\right)^{0.10} + 0.59\left(\frac{T}{H}\right)^{0.53}\right] + \left[0.52\left(\frac{W}{H}\right)^{0.10} + 0.46\left(\frac{T}{H}\right)^{0.17}\right]\left(1 - 0.87e^{-\frac{S}{H}}\right) \quad (1)$$

The relative error of the formula is less than 8.2 % for $0.02 < W/H, T/H, S/H < 1.28$.

Here, c_{12} is the coupling capacitance between two parallel signal lines. It can be estimated as

$$\frac{c_{12}}{\varepsilon_{ox}} = \frac{T}{S} + 1.21\left(\frac{T}{H}\right)^{0.10}\left(\frac{S}{H} + 1.15\right)^{-2.22} + 0.25\ln\left(1 + 7.17\frac{W}{S}\right)\left(\frac{S}{H} + 0.54\right)^{-0.64} \quad (2)$$

The relative error of the formula is less than 8.6 % for $0.02 < W/H, T/H < 1.28$ and $0.02 < S/H < 2.56$.

All the capacitances mentioned above are in units of F/cm, and ε_{ox} is the dielectric constant of SiO_2, which is equal to $3.9 \times 8.855 \times 10^{-14}$ F/cm. We will use these formulas to finish the capacitance calculation for our delay model of coupling RC interconnects.

3 Delay computation of coupling RC interconnects

Crosstalk noise in coupling lines can either increase or decrease signal propagation delays. This depends on the line impedances and on whether the neighboring lines are driven by the same input voltage or different input voltages (i.e. the two lines are active) or one of the lines has no input voltage (i.e. one line is quiet). Here we discuss the latter case, in which one input is a rising ramp signal and the other is quiet.

3.1 Model of coupling RC interconnects

In this section, we use a coupling line model presented in Ref. [5] to derive an analytical formula for the delay. A general case for two coupling lines is shown in Fig. 2. The quiet driver is modeled by an effective holding resistance R_h, whereas the active driver is modeled by an effective Thevennin model consisting of a saturated ramp voltage source with a slew rate of t_r and a Thevennin resistance R_{th}. Other components of the model are computed based on the technology and geometrical information. The coupling node is defined to be the middle of the coupling location for both nets.

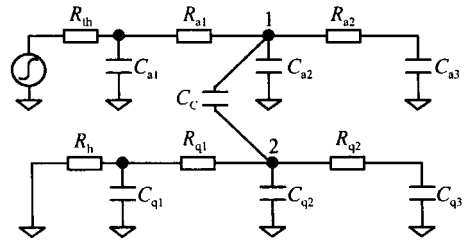

Fig. 2　Model of coupling RC interconnects

It is quite straightforward to calculate the circuit parameters of the proposed model. Taking the quiet net as an example, node 2 is the center of the coupling region, which divides the entire quiet wire into two segments. C_C is the coupling capacitance when two lines with the same length are running parallel. The notations in Fig. 2 can be calculated as follows.

$$R_{a1} = R_{a2} = \frac{1}{2}R_a,\ C_{a1} = \frac{1}{4}C_a,\ C_{a2} = \frac{1}{2}C_a,\ C_{a3} = \frac{1}{4}C_a + CL_a,\ R_{q1} = R_{q2} = \frac{1}{2}R_q,\ C_{q1} = \frac{1}{4}C_q,\ C_{q2} = \frac{1}{2}C_q,\ C_{a3} = \frac{1}{4}C_q + CL_q$$

3.2 Delay computation

Effective capacitance was first presented in Ref. [6] to estimate the delay of a logic gate. Ding *et al*. [7] used this idea to complete the quiet aggressor net reduction for crosstalk estimation. This concept also can be used in RLC tree reduction[8]. Here we use this method to match the quiet net at the coupling node of the active net.

Let $Y(s)$ denote the point admittance of a general circuit. The Taylor series expansion is

$$Y(s) = \sum_{n=0}^{\infty} y_n s^n \quad (3)$$

where y_n is the nth expansion coefficient. For many circuit applications, the terms up to s^3 are adequate to characterize the transient response of a linear circuit.

$$Y(s) = y_0 + y_1 s + y_2 s^2 + y_3 s^3 + O(s^4) \quad (4)$$

Note that the first term y_0 is zero when there is no DC conducting path from the observation point to the ground.

Here we use an effective capacitance to evaluate the quiet net and coupling capacitance as shown in Fig. 3.

Consider the model of a quiet net and coupling capacitance. We first reduce the net to a single re-

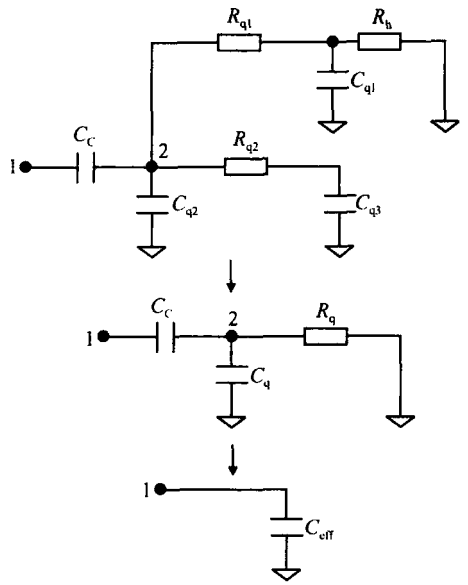

Fig. 3 Reduction flow

sistor R_q and a single capacitor by matching the first two Taylor series expansion coefficients y_0 and y_1 of the quiet net at node 2. The admittance at node 2 is obtained as

$$Y_1(s) = \frac{1}{R_h + R_{q1}} + \left(\frac{R_h^2}{(R_h + R_{q1})^2} C_{q1} + C_{q2} + C_{q3} \right) s + O(s^2) \quad (5)$$

Therefore, we have the following equations:

$$R_q = R_h + R_{q1} \quad (6)$$

$$C_q = \frac{R_h^2}{(R_h + R_{q1})^2} C_{q1} + C_{q2} + C_{q3} \quad (7)$$

Next, we derive the formula to estimate the effective coupling capacitance C_{eff} of the simplified circuit shown above. It is found by matching the current drawn by the circuit in Fig. 3 with that taken by the effective capacitor which is grounded at the other end. The current drawn from nodes 1 to 2 through the coupling capacitor C_C is

$$I = C_C \left(\frac{dV_1(t)}{dt} - \frac{dV_2(t)}{dt} \right) \quad (8)$$

Therefore, our task is to find a constant C_{eff} such that

$$C_{eff} \frac{dV_1(t)}{dt} \approx C_C \left(\frac{dV_1(t)}{dt} - \frac{dV_2(t)}{dt} \right) \quad (9)$$

The effective capacitance value during the entire input rising period can be estimated by integrating both sides of Eq. (9). The following formula for the effective capacitance is obtained.

$$C_{eff} = \left(1 - \frac{R_q C_C}{t_r} (1 - e^{-t_r / R_q (C_q + C_C)}) \right) C_C \quad (10)$$

After reducing the coupling capacitance and quiet interconnect, we can get the decoupling active interconnect as shown in Fig. 4. It is a cascaded RC construction. According to the Elmore delay definition, the equivalent Elmore delay of the active line can be expressed as

$$t_D = R_{a1} C_{a1} + (R_{a1} + R_{a2}) \times \left(C_{a2} + \left(1 - \frac{R_q C_C}{t_r} (1 - e^{-t_r / R_q (C_q + C_C)}) \right) C + (R_{a1} + R_{a2} + R_{a3}) C_{a3} \right) \quad (11)$$

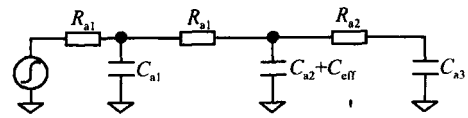

Fig. 4 Decoupling active interconnect

4 Simulation results and discussion

We have compared our delay calculation with the SPICE simulation for different methods. We have Cu interconnect resistance and capacitance data extracted by analytical expressions with $W = 0.25\mu m$, $S = 0.3\mu m$, $T = 0.25\mu m$, and $H = 0.5\mu m$.

Table 1 shows the values for interconnect parasitic parameters. R_a, R_q, C_a, and C_q can be given as:

$$R_a = r_a L, \quad C_a = c_a L, \quad R_q = r_q L, \quad C_q = c_q L$$

R_{th}, R_h, CL_a, CL_q, and L are given by $R_{th} = 20\Omega$, $R_h = 30\Omega$, $CL_a = 0.2pF$, $CL_q = 0.1pF$, and $L = 2mm$ respectively.

Table 1 Values for interconnect parasitic parameters

c_a/ (pF · m^{-1})	r_a/ (kΩ · m^{-1})	c_q/ (pF · m^{-1})	r_q/ (kΩ · m^{-1})
170	15	170	15

Example 1. Let the coupling capacitance C_C equal 240fF and change the rise time of the input signal from 10 to 100ps.

The simulation results for our method, the conventional method[9] that uses Miller theory to decouple the two adjacent interconnects, and HSPICE are plotted in Fig. 5. In our method, when computing the Elmore delay, we used different input rising times, but this information is not available when the conventional delay model is used to analyze the circuit. The error of our method is always within 19 % of simulation results. The elmore delay method with $2C_C$ replacing coupling capacitance may have an error up to 50 % compared to circuit simulation results.

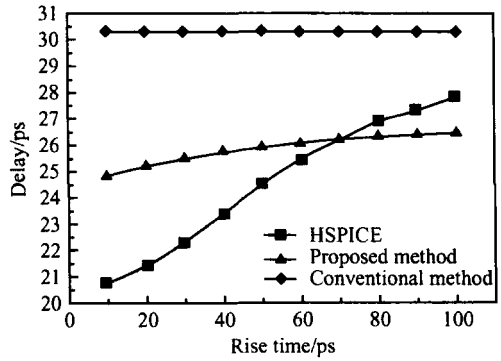

Fig. 5　Relation between delay and rise time

Example 2. Let the rise time of the input signal equal 0. 1ns and change the coupling capacitance C_C from 30 to 420pF.

The simulation results obtained are shown in Fig. 6. The delay estimates calculated using our analytical model have error within 7% of HSPICE-computed delay estimates, while the Elmore delay estimates vary by as much as 60% from HSPICE computed delays.

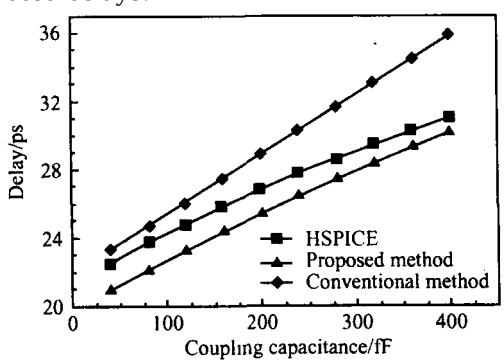

Fig. 6　Relation between delay and coupling capacitance

The above examples show that our method is more accurate than the conventional method.

5　Conclusion

Compared with numerical simulation techniques, fast analytical estimation methods of interconnect delay are needed for incremental performance driven layout synthesis. We give an approach for analyzing coupling RC interconnect delay. Compared to the traditional method, which uses Miller capacitance, the new method not only improves the accuracy but also reflects the delay dependence on the rise time. It has the same complexity as the Elmore delay method and can be used in performance-driven routing optimization.

References

[1] Ismail Y I, Friedman E G, Neves J I. Equivalent Elmore delay for RLC trees. IEEE Trans CAD, 2000, 19(1): 83

[2] Devgan A. Efficient coupled noise estimation for on-chip interconnects. ICCAD, 1997: 147

[3] Vittal A, Marek-Sadowska M. Crosstalk reduction for VLSI. IEEE Trans CAD, 1997, 16(3): 290

[4] Delorme N, Belleville M, Chilo J. Inductance and capacitance analytic formulas for VLSI interconnects. Electron Lett, 1996, 32(11): 996

[5] Becer M R, Blaauw D, et al. Analysis of noise avoidance techniques in DEM interconnect using a complete crosstalk noise model. Proc DATE, 2002: 456

[6] Qian J, Pullela S, Pillage L. Modeling the "effective capacitance" for the RC interconnect of CMOS gates. IEEE Trans CAD, 1994, 13(12): 1526

[7] Ding L, Blaauw D, Mazumder P. Accurate crosstalk noise modeling for early signal integrity analysis. IEEE Trans CAD, 2003, 22(5): 627

[8] Dong Gang, Gao Haixia, Yang Yintang, et al. A stable construction of RLC interconnect π model and its application. Chinese Journal of Semiconductors, 2005, 26(3): 582 (in Chinese) [董刚, 高海霞, 杨银堂, 等. 一种稳定的 RLC 互连 π 模型构建及其应用. 半导体学报, 2005, 26(3): 582]

[9] Chen P, Kirkpatrick D, Keutzer K. Miller factor for gate-level coupling delay calculation. ICCAD, 2000: 68

两相邻耦合互连的 Elmore 延时估计 *

董 刚† 杨银堂 李跃进

(西安电子科技大学微电子研究所 宽禁带半导体材料与器件教育部重点实验室, 西安 710071)

摘要: 基于"有效电容"的概念提出了一种分析两相邻耦合 RC 互连延时的方法. 与采用 Miller 电容的传统方法比较,该方法不但提高了计算精度而且反映出了延时随信号上升时间的变化规律. 该方法与 Elmore 延时法具有相同的计算复杂度,可广泛用于考虑耦合电容的面向性能的布线优化.

关键词: 电容提取; 耦合 RC 互连; 有效电容; 延时
EEACC: 7410D; 5120
中图分类号: TN405.97 **文献标识码**: A **文章编号**: 0253-4177(2006)01-0054-05

*国防科技预研资助项目(批准号:41323020204)
†通信作者. Email:donggang1978@hotmail.com
2005-07-18 收到,2005-09-23 定稿