S-Band 1mm SiC MESFET with 2W Output on Semi-Insulated SiC Substrate

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Abstract: A SiC MESFET structure is successfully prepared on a semi-insulated 50mm SiC substrate using a hot-wall SiC reactor. The doping concentration for the channel layer is about $1.7\times10^{17}\,cm^{-3}$, and the thickness is about 0.35μm. An unintentionally n-doped buffer layer is employed between the substrate and the channel layer. A cap layer for Ohmic contact is doped to $10^{19}\,cm^{-3}$. MESFET devices are fabricated using inductively coupled plasma etching and other conventional tools. Power devices with a 1mm gate width are measured and a 2W output at 2GHz is obtained.

Key words: MESFET; SiC; buffer layer
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1 Introduction

Due to its superior physical properties, SiC is one of the most promising materials for high power, high frequency, and high temperature electronic devices. Its device technology is relatively mature compared to other wide bandgap material device technologies. Cree, a leading company in the SiC business, announced their establishment of a 75mm SiC foundry a few years ago, and S-band 60W power devices have been one of their standard products from the line ever since. In addition, a CW output power of 80W and pulsed output power of 120W under 3.1GHz operation were also reported 6 years ago[1,2]. However, in China, research on SiC related devices is still in a very early stage. In this paper, we report our initial research results on SiC MESFETs.

2 Material growth and device fabrication

The growth of the MESFET structure was performed in a hot-wall CVD reactor with a $SiH_4 + C_3H_8 + H_2$ system. The typical growth temperature is ~1550 ℃ at the susceptor top, and the system pressure is controlled at about 6666Pa. The growth rate is adjustable from 1 to 5μm/h. The MESFET structure consists of a cap layer, a channel layer, and a buffer layer on a SiC substrate, as shown in Fig. 1. For a better ohmic contact, the cap layer was doped to a $1.5\times10^{19}\,cm^{-3}$ concentration with a thickness of 0.15μm. The channel doping concentration was designed to be about $1.7\times10^{17}\,cm^{-3}$, the achievement of which was confirmed by 9 cross-plots obtained by mercury CV measurement as shown in Fig. 2. The thickness of the channel layer was 0.35μm. The buffer layer can prevent damage and deep level impurities in the substrate from the active layer. Due to the lack of a p-doping source at the moment, we used an unintentionally n-type layer as the buffer in order to minimize the influence of the substrate, which had a thickness of 2μm and a concentration of about $5\times10^{15}\,cm^{-3}$. The substrate we used was a 50mm 8° off-axis (0001) compensated semi-insulated (SI) 4H-SiC substrate. A Lehighton non-contact mapping system was used to measure the uniformity of the square-resistance, which was

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4.47 %. The surface morphology was evaluated using an atomic force microscope, showing a roughness of 0.882nm, as depicted in Fig. 3.

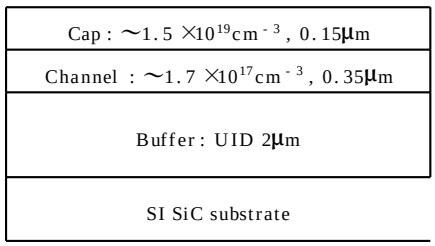

Fig. 1　Schematic SiC MESFET structure

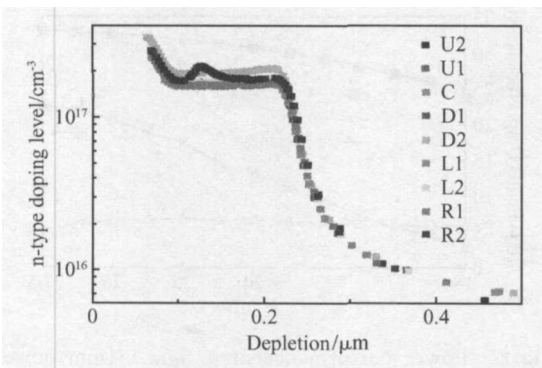

Fig. 2　Multiple point mercury CV measurement results showing the channel concentration of 1.7 ×10^17 cm^-3

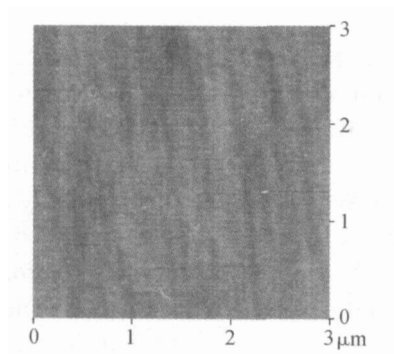

Fig. 3　AFM image after the epilayer is grown

For the device fabrication, there are two key processes. One is the dry etching process to expose the channel layer for the gate; the other is the ohmic contact process. Dry etching was used to etch the SiC since conventional wet chemical etching is very difficult due to the chemical inertness of SiC and the high bond energies between silicon and carbon. ICP etching is a high-density plasma etching technique in which the plasma is formed in a dielectric vessel encircled by an inductive coil to which RF power is applied. Anisotropic profiles were obtained by using low-pressure conditions to minimize ion scattering and lateral etching. Hence ICP provides the potential of achieving excellent anisotropy, low surface damage, smooth morphology, and even a high etching rate for SiC material. The ICP reactor we used is a fluorine-based etching system. The recipe for a typical case is a mixture of SF_6 and Ar at a coil power of 550W and an RF power of 200W. The etching rate was about 95nm/min. The surface morphology after ICP etching is shown in Fig. 4. After the cap layer etch, Pt/Au was evaporated to form the gate after photolithography.

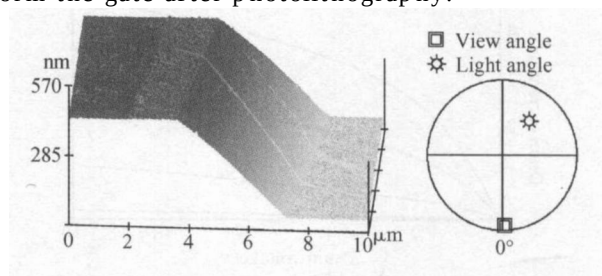

Fig. 4　AFM image after the SiC cap layer is dry-etched

Ohmic contact is very important for microwave devices. It's more important for applications using high current densities that may result in large voltage drops even across a small resistance. The contact resistance specific to n-type SiC is normally in the range of 10^{-4}~$10^{-6}\Omega \cdot cm^2$ and is highly dependent on the surface doping concentration, choice of the metallization system, sample preparation, and the post metallization heat treatment. In our device, a Ti-based metallization system was used. After the deposition of Ti/Pt/Au by electron beam evaporation, the sample was annealed at 980 ℃ using RTA (rapid thermal annealing) for 5min in an ambient of nitrogen to form the Ohmic contact. The specific contact resistance achieved was about $2 \times 10^{-6}\Omega \cdot cm^2$ by using the transmission line method (TLM), as depicted in Fig. 5.

3　Results

The device fabricated was measured using Keithley semiconductor parameter analyzer. Figure 6 shows typical I-V curves for a 0.5μm × 100μm SiC MESFET device. The saturation current I_{ds} was 200mA/mm and the peak transcon-

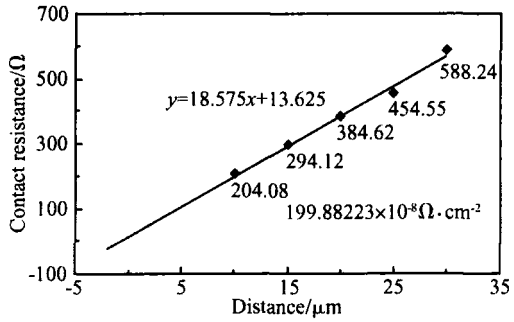

Fig. 5 Transmission line to measure the contact resistance

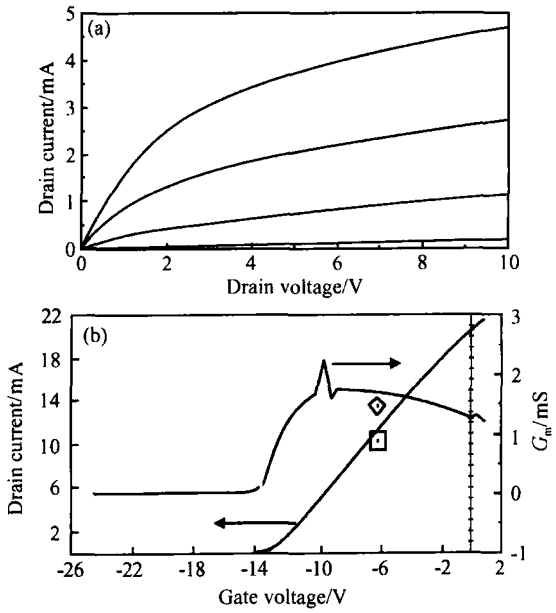

Fig. 6 DC performance of the 0.5μm ×100μm device (a) Typical I-V curves; (b) Transconductance and I_{ds} versus gate voltage

ductance was about 18mS/mm. Breakdown voltage was about 120V. The small signal RF performance was characterized using on wafer RF coplanar probes. From the small-signal S-parameters, the calculated cutoff frequency (f_T) and maximum frequency of oscillation (f_{max}) were 6.7 and 25GHz, respectively, as shown in Fig. 7. Power devices with a 1mm gate width were also fabricated. The devices were biased in class A with a 40V drain bias and tested in the CW mode at 2GHz using a manually tuning matching system. An output power of 2W and gain over 5dB at 2GHz were measured from the 0.5μm ×1mm gate width device (Fig. 8), showing its superior microwave power potential over conventional Si based devices.

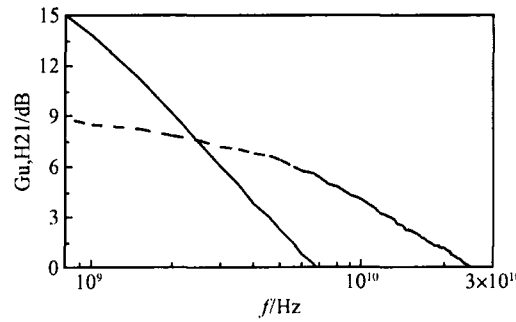

Fig. 7 Small signal performance of the SiC MESFET showing f_T and f_{max}

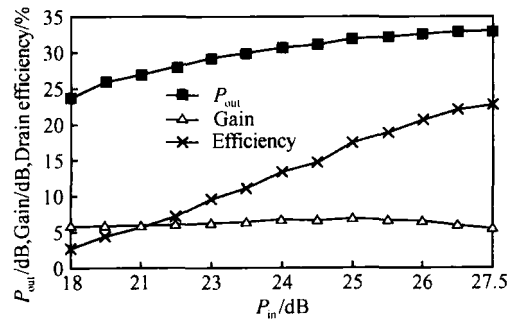

Fig. 8 Power performance of 0.5μm ×1mm power SiC MESFETs at 2GHz

4 Conclusion

A SiC MESFET structure was successfully prepared on a semi-insulated 50mm SiC substrate using a hot-wall SiC reactor. A SiC MESFET with a 1mm gate width that produced an output of 2W at 2GHz CW power was developed, which is an improvement by a factor of two over conventional Si devices due to the outstanding performance of SiC. The relatively low drain efficiency (23%) was caused by the leaky n-type buffer layer, which will be replaced by a lightly p-doped buffer in the near future. To further improve the power performance in future development, effective thermal management will be the key because of the high power density dissipated in the device.

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在半绝缘 SiC 衬底上制备的 S 波段 2W 碳化硅 MESFET

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摘要: 介绍了用热壁反应炉在 50mm SiC 半绝缘衬底上制备的 SiC MESFET 外延材料. 其沟道层厚度约为 0.35μm, 掺杂浓度约为 $1.7\times10^{17}cm^{-3}$. 沟道和衬底之间的缓冲层为非有意掺杂的弱 n 型. 欧姆接触用的帽层掺杂浓度约 $10^{19}cm^{-3}$. 器件制备采用了 ICP 刻蚀等技术. 微波测试结果表明, 1mm 栅宽功率器件封装后在 2GHz 下输出功率达到了 2W.

关键词: 碳化硅; 微波; 功率; MESFET

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