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Study of Electron Mobility in 4H-SiC Buried-Channel MOSFETs*

Gao Jinxia, Zhang Yimen†, and Zhang Yuming

(Key Laboratory of the Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, Microelectronics Institute, Xidian University, Xi'an 710071, China)

Abstract: The effects of several factors on mobility in 4H-SiC buried-channel (BC) MOSFETs are studied. A simple model that gives a quantitative analysis of series resistance effects on the effective mobility and field-effect mobility is proposed. A series resistance not only decreases field-effect mobility but also reduces the gate voltage corresponding to the peak field-effect mobility. The dependence of the peak field-effect mobility on series resistance follows a simple quadratic polynomial. The effects of uniform and exponential interface state distributions in the forbidden band on field-effect mobility are analyzed with an analytical model. The effects of non-uniform interface states can be ignored at lower gate voltages but become more obvious as the gate bias increases.

Key words: 4H-SiC; buried-channel; MOSFET; mobility; series resistance; interface states
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1 Introduction

The bulk mobility of 4H-SiC is approximately two times higher than that of 6H-SiC. Therefore, the 4H-SiC MOSFET is a promising candidate for high-power devices with high speed and low loss. However, the reported channel mobility of 4H-SiC surface channel MOSFETs is extremely low[1,2], with a typical value of 5～40cm^2/(V·s). It is believed that the channel mobility[3] is lowered by the high density traps at 2.9eV above the valence band edge at the SiO_2/4H-SiC interface. Recently, 4H-SiC MOSFETs fabricated on other crystal faces have demonstrated higher mobility[4], but few improvements have been made on commercial Si faces. It has been reported that oxidation in N_2O or NO can improve mobility noticeably[5], but the process has not been refined and needs to be further studied.

One possible way to raise the channel mobility is to keep the transported electrons away from the SiO_2/4H-SiC interface. Some research groups have reported that a buried channel (BC) structure can improve the channel mobility in 4H-SiC MOSFETs[6～8]. An effective mobility in a 4H-SiC BC-MOSFET of 230cm^2/(V·s) was reported[9]. This result shows that this BC-MOSFET structure has important potential in high speed circuits.

We have found[10] that interface states and series resistances still influence the transconductance and channel conductance of the device and therefore affect the field-effect mobility and effective mobility. A series resistance decreases the voltage across the channel and makes the measured channel conductance smaller than actual value. Large densities of interface states within the bandgap possibly affect the observed drain current and transconductance because interface states capture carriers and change the mobile carrier density. At present, the effects mentioned above have not been reported.

In this paper, the effects of interface states and series resistance on effective mobility and field-effect mobility are studied quantitatively. Several analytical models are deduced to describe the effects. The dependence of peak field-effect mobility on series resistance and interface states is obtained. Mrinal et al.[11] pointed out that the interface state density increases rapidly with energy near the band edges. So the effect of non-uniform interface state distribution on field-effect mobility is also discussed in this paper.

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† Corresponding author. Email: ymzhang@xidian.edu.cn
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2 Device fabrication and main parameters

The detailed fabrication processes of SiC BC-MOSFETs are described in Ref. [8]. The main parameters of a 4H-SiC BC-MOSFET are listed in Table 1, in which d is the thickness of the oxide layer, N_D^+ the channel carrier concentration, V_{FB} the flatband voltage, and x_i the implanted channel depth. They are extracted from C-V measurements. Q_{sc} is the interface effective charge density obtained from the relation $Q_{sc} = -C_{ox}(V_{FB} - \phi_{ms})/q$, Q_{ds} is the density of deep level traps in the SiC/SiO_2 interface estimated by the voltage shift in forward- and reverse-scanned C-V curves. The threshold voltage of MOSFETs is determined by extrapolating the point of maximum slope on the $I_D \sim V_G$ curve to the gate-voltage axis. A specific contact resistance of $5.5 \times 10^{-4} \Omega \cdot cm^{-2}$ is obtained by the measurement with the transfer length method.

Table 1 4H-SiC BC-MOSFET parameters

N_A/cm^{-3}	N_D^+/cm^{-3}	W/L	d /nm	V_T /V	x_i /μm	V_{FB} /V	Q_{sc} /cm^{-2}	Q_{ds} /cm^{-2}
2.3×10^{16}	7.64×10^{16}	100/3	44	2.29	0.19	5.7	-2.7×10^{12}	1.2×10^{11}

3 Extraction of effective mobility and field-effect mobility

The SiC surface can be in the depletion, accumulation, and flatband states at different gate biases. Different surface states allow the BC MOSFETs to operate in several modes: surface channel mode, buried-channel mode, and surface-buried channel mixed mode. The analytical expression of the drain current is different in each operational mode. The surface/buried channel mixed mode can be ignored if the drain voltage is very small, and the drain current in the linear region for a BC-MOSFET can be described by

$$I_D = -\frac{W}{L} q \bar{\mu}_n Q_{ch} V_D \quad (1)$$

where W and L are the channel width and length, $\bar{\mu}_n$ is the average mobility in the channel, and Q_{ch} is the electron density per unit area in the channel, which includes the implanted charge Q_I, the charge Q_S in the surface depletion/accumulation region, and the depletion layer charge Q_B of the pn junction

$$Q_{ch} = Q_I + Q_S + Q_B = -\frac{1}{q}\left[qN_D^+ x_i + \bar{C}(V_G - V_{FB}^*) - \sqrt{\frac{2\varepsilon_s\varepsilon_0 qN_A^- N_D^+}{N_A^- + N_D^+}}(V_{bi} - V_{BS})^{1/2}\right] \quad (2)$$

Here x_i is the channel depth, N_D^+ and N_A^- are the ionized donor and acceptor densities respectively, V_{bi} is the built-in potential of the channel-substrate junction, and V_{BS} is the substrate/source bias. V_{FB}^* is a function of the surface potential V_S if interface state charge cannot be neglected.

$$V_{FB}^* = V_{FB} - \frac{qQ_{it}(V_S)}{C_{ox}} + \frac{qQ_{it}(V_S = 0)}{C_{ox}} \quad (3)$$

Here $Q_{it}(V_S)$ is the charged interface state density which varies with surface potential. $Q_{it}(V_S) = -qD_{it}(V_S + \phi_B)$ if the interface states are distributed uniformly in the forbidden band. Equation (3) can be rewritten as

$$V_{FB}^* = V_{FB} + \frac{q^2 D_{it} V_S}{C_{ox}} \quad (4)$$

V_{FB}^* equals the flatband voltage V_{FB} if the interface state density is very small. $\bar{C}$ is the average capacitance. When $V_{GS} - V_{FB} > 0$, the surface is in complete surface accumulation, the device operates in the surface channel mode, and $\bar{C} \approx C_{ox}$. At a gate bias of $V_{GS} - V_{FB} < 0$, the surface is in complete surface depletion and the device operates in buried channel mode. In this case, $\bar{C}$ hardly varies with drain voltage in linear region, and the average capacitance can be calculated by

$$\bar{C} = \frac{C_{ox}}{\left(1 - \frac{2C_{ox}^2(V_G - V_{FB}^*)}{q\varepsilon_s\varepsilon_0 N_D^+}\right)^{1/2}} \quad (5)$$

According to Eq. (1), the effective mobility and field-effect mobility can be extracted by

$$\mu_{eff} = \frac{g_D}{-\frac{W}{L} qQ_{ch}} \quad (6)$$

$$\mu_{FE} = \frac{g_m}{\frac{W}{L}\bar{C}V_D} \quad (7)$$

where g_D is the channel conductance, and g_m is the transconductance.

4 Effect of interface states and S/D series resistance

For SiC devices, the influence of interface

states and source-drain series resistance usually cannot be neglected. It is believed that the negative interface effective charge with a density of about $-2.7\times10^{12}\mathrm{cm}^{-2}$ shown in Table 1 is determined by the interface states that capture electrons. $\overline{C}$ and V_{FB}^{*} in Eq. (2) are related to the interface states, and the existence of the source-drain series resistance R_{SD} makes the voltage across the channel smaller than the drain bias. In practice, however, the measured mobility is includes the effects of the interface states and R_{SD}.

Assume Q_{ch}^{0} to be the channel electron density without the effect of interface states. Then μ_{eff}^{0} (or μ_{FE}^{0}) refers to the intrinsic effective (or field-effect) mobility without taking into account the effects of the interface states and series resistance. Equation (1) can be rewritten as

$$I_D = \frac{W}{L}q\mu_{eff}V_D Q_{ch}^{0} = \frac{W}{L}q\mu_{eff}^{0}(V_D - I_D R_{SD})Q_{ch} \quad (8)$$

The effective channel conductance is thus expressed by

$$g_D = \frac{W}{L}q\mu_{eff}Q_{ch}^{0} = \frac{g_D^{0}}{1 + R_{SD}g_D^{0}} \quad (9)$$

where the intrinsic channel conductance g_D^{0} is given by

$$g_D^{0} = \frac{W}{L}q\mu_{eff}^{0}Q_{ch} \quad (10)$$

Let $g_D = \partial g_D/\partial V_G$

$$g_G = \frac{g_G^{0}}{(1 + R_{SD}g_D^{0})^2} \quad (11)$$

where $g_G^{0} = \partial g_D^{0}/\partial V_G$. From Eqs. (9～11)

$$\mu_{eff} = \frac{Q_{ch}}{Q_{ch}^{0}} \times \frac{\mu_{eff}^{0}}{1 + R_{SD}g_D^{0}} \quad (12)$$

$$\mu_{FE} = \frac{\mu_{FE}^{0}}{(1 + R_{SD}g_D^{0})^2} \quad (13)$$

Differentiating Eq. (13), the following expression is obtained:

$$\frac{\partial\mu_{FE}}{\partial V_G} = \frac{1}{(1 + R_{SD}g_D^{0})^2} \times \frac{\partial\mu_{FE}^{0}}{\partial V_G} - \frac{2R_{SD}(\mu_{FE}^{0})^2}{(1 + R_{SD}g_D^{0})^3} \quad (14)$$

We define $V_{G,max}^{0}$ as the gate bias at which the intrinsic field-effect mobility μ_{FE}^{0} is maximum, and $V_{G,max}$ is at the maximum of μ_{FE}. So $\partial\mu_{FE}^{0}/\partial V_G = 0$ at $V_G = V_{G,max}^{0}$. From Eq. (14)

$$\left.\frac{\partial\mu_{FE}}{\partial V_G}\right|_{V_{G,max}^{0}} = -\frac{2R_{SD}(\mu_{max}^{0})^2}{(1 + R_{SD}g_D^{0}(V_{G,max}^{0}))^3} \quad (15)$$

It can be seen from Eqs. (13) and (15) that $\mu_{FE} < \mu_{FE}^{0}$ and $\partial\mu_{FE}/\partial V_G < 0$ at $V_G = V_{G,max}^{0}$, which means the existence of R_{SD} not only decreases the field-effect mobility but also changes the gate voltage corresponding to peak field-effect mobility. We conclude from $\mu_{FE} < \mu_{FE}^{0}$ that $V_{G,max}^{0} > V_{G,max}$.

The effects of series resistance and interface states on effective mobility μ_{eff} can be analyzed with Eq. (12). But Equation (13) is only used to analyze the effect of series resistance on field-effect mobility μ_{FE}. Let g_m^{0} be the intrinsic transconductance without taking into account the effect of interface states

$$g_m = g_m^{0}\left(1 - \frac{C_{it}}{C_{ox} + C_s + C_{it}}\right) \quad (16)$$

$$\mu_{FE} = \frac{\mu_{FE}^{0}\left(1 - \frac{C_{it}}{C_{ox} + C_s + C_{it}}\right)}{(1 + R_{SD}g_D^{0})^2} \times \frac{\overline{C}^{*}}{\overline{C}} \quad (17)$$

where C_s is the capacitance of surface depletion layer, $C_{it} = -\partial Q_{it}/\partial V_S$ is taken as the interface state capacitance ($C_{it} = q^2 D_{it}$), and $\overline{C}^{*}$ and $\overline{C}$ are the average capacitance with and without the effect of the interface state capacitance, respectively.

5　Results and discussion

5.1　Effect of average capacitance

Chung et al. replaced $\overline{C}$ with C_{ox} to extract the field-effect mobility[6]:

$$\mu_{FE} = \frac{g_m}{\frac{W}{L}C_{ox}V_D} \quad (18)$$

This simplification is suitable in the surface channel mode, but an error occurs in the buried-channel mode. Figure 1 shows the extraction results of the field-effect mobility with Eqs. (7) and (18). The field-effect mobility at $V_G < V_{FB}$ is underestimated if $\overline{C} = C_{ox}$. From experiment data, the peak field-effect mobilities are 41 and 24.3$\mathrm{cm}^2/(\mathrm{V\cdot s})$ respectively. When $V_G < V_{FB}$, the device operates in the buried-channel mode, and the actual gate capacitance should be smaller than the oxide capacitance C_{ox}. When $V_G > V_{FB}$, the device operates in surface-channel mode. In this case, the surface of the semiconductor is in accumulation, so that $\overline{C} = C_{ox}$, and the two curves match well.

5.2　Effective mobility

The measured sheet resistance of the source/

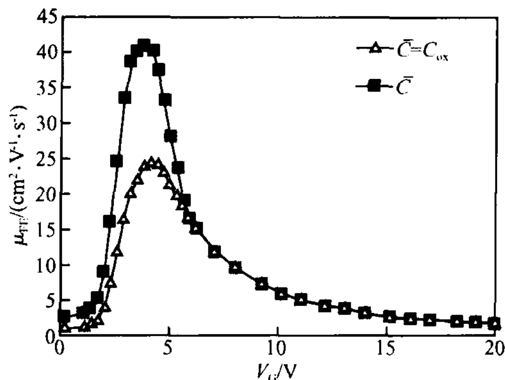

Fig. 1 Effect of average capacitance on field-effect mobility

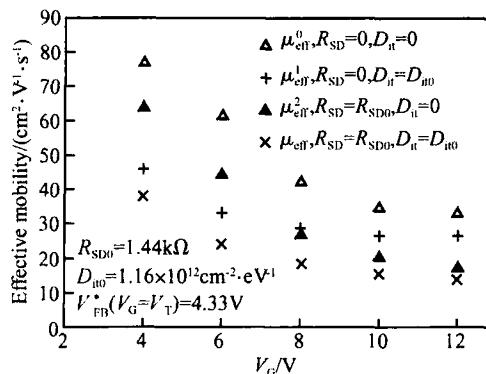

Fig. 2 Dependence of effective mobility on gate voltage

drain region is about 4.5kΩ/ □ and the source (or drain) series resistance calculated according to the designed size of 16μm ×100μm is about 0.72kΩ. Therefore the total source/drain series resistance R_{SD} is 1.44kΩ. The expression for intrinsic effective mobility is obtained from Eq. (12).

$$\mu^0_{eff} = \frac{Q^0_{ch}}{Q_{ch}} \times \frac{\mu_{eff}}{1 - R_{SD} g_D} \tag{19}$$

In our calculation, the interface state density is obtained to ensure that $V^*_{FB} = V^*_{FB}(V_G = V_T)$ at the threshold voltage. In our samples, $V^*_{FB}(V_G = V_T)$ is about 4.33V, and $D_{it} = 1.16 \times 10^{12} cm^{-2} \cdot eV^{-1}$. The interface state charge density Q_{it} depends on the bending of the surface band qV_s, and the relation between V^*_{FB} (or $\bar{C}$) and V_s can be determined only by solving Poisson's equation numerically.

Figure 2 shows the effective mobility versus gate bias at a very small drain voltage. The parameters used in calculation are listed in the inset. The effective mobility μ_{eff} can be extracted easily with Eq. (6). Then the intrinsic effective mobility μ^0_{eff} can be calculated from Eq. (19). μ^1_{eff} and μ^2_{eff} express the effective mobility in terms of different interface states and the series resistance referred to μ^0_{eff}. At $V_G = 4V$, μ_{eff} is about $38cm^2/(V\cdot s)$ and the intrinsic effective mobility μ^0_{eff} can reach $77cm^2/(V\cdot s)$. Also it can be seen in Fig. 2 that the interface state and series resistance both decrease effective-mobility noticeably at a lower gate voltage. The effect of the series resistance becomes more obvious at a higher gate voltage because the drain current increases greatly with the gate voltage, and the voltage dropped across the series resistance becomes more serious, so R_{SD} is the one of main factors that decreases mobility at a larger gate voltage.

5.3 Field-effect mobility

The field-effect mobility extracted directly from experimental transconductance is shown in Fig. 1 (black square). The intrinsic field-effect mobility can be calculated from Eq. (20)

$$\mu^0_{FE} = \frac{\mu_{FE}(1 + R_{SD} g^0_D)^2}{\left(1 - \frac{C_{it}}{C_{ox} + C_s + C_{it}}\right)} \times \frac{\bar{C}}{C^*} \tag{20}$$

To the second-order, Eq. (13) takes the following form:

$$\mu_{max} = \mu^0_{max}[1 - 2R_{SD} g^0_d(V^0_{G,max}) + 3(R_{SD} g^0_d(V^0_{G,max}))^2] \tag{21}$$

Figure 3(a) shows the field-effect mobility versus the gate voltage for various source-drain series resistances R_{SD}, and Figure 3 (b) illustrates the dependence of the maximum mobility μ_{max} and its gate voltage point $V_{G,max}$ on R_{SD}. The peak field-effect mobility decreases from 75 to about $53cm^2/(V\cdot s)$ when the series resistance R_{SD} increases from zero to 1.4kΩ, and $V_{G,max}$ decreases from 4.2 to 3.7V. Moreover, the peak field-effect mobility calculated with Eq. (21) is also shown in Fig. 3(b). The quadratic polynomial can be used to exactly describe the dependence of the peak field-effect mobility on series resistance.

Figure 4 shows the effect of the interface states on field-effect mobility. Uniform interface state density in the forbidden-band is assumed. The peak field-effect mobility decreases linearly with interface state density, and $V_{G,max}$ varies only slightly with interface state density. This is because the effect of the interface states is screened by electrons in the accumulation layer. Thus in

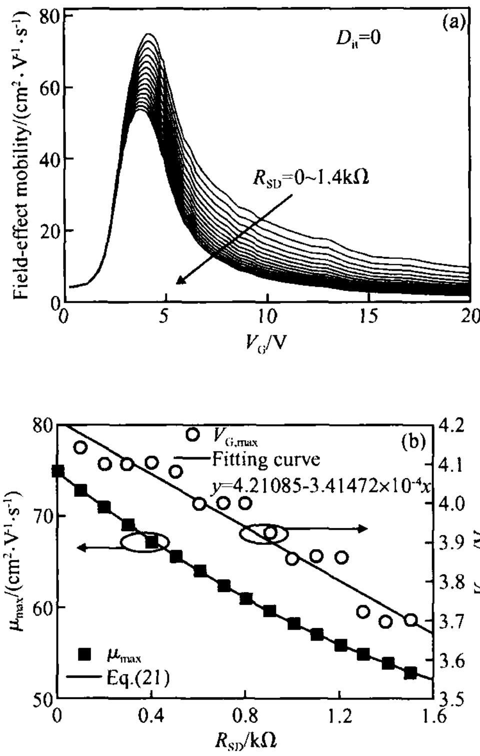

Fig. 3　(a) Dependence of field-effect mobility on gate voltage with R_{SD} from 0 to 1.4kΩ; (b) Dependence of maximum mobility μ_{max} and its gate voltage point $V_{G,max}$ on R_{SD}

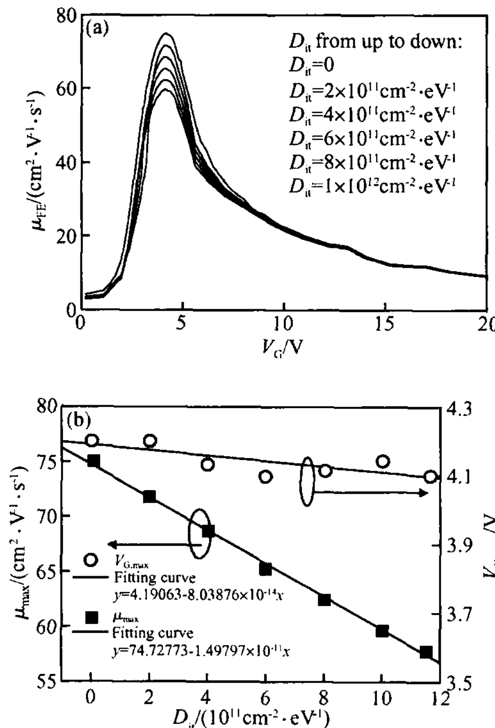

Fig. 4　(a) Dependence of field-effect mobility on gate voltage for various D_{it}; (b) Dependence of maximum mobility μ_{max} and its gate voltage point $V_{G,max}$ on D_{it}

this case the field-effect mobility in the surface channel mode hardly changes with interface state.

As a matter of fact, the experiment shows that the interface state density in the forbidden band is non-uniform, following an exponential relation with energy:

$$D_{it} = D_{it0} + D_c e^{-(E_c - E)/\xi} \qquad (22)$$

Here D_{it0} is the interface state density in the midband, and D_c is the peak interface state at the bottom of the conduction band. Keeping D_{it0} and D_c constant, the effect of interface states for different ζ on field-effect mobility is shown in Fig. 5. The calculated distribution and experimental data[11] of interface states are also plotted in the inset. The reduction of peak field-effect mobility caused by non-uniform interface states is smaller

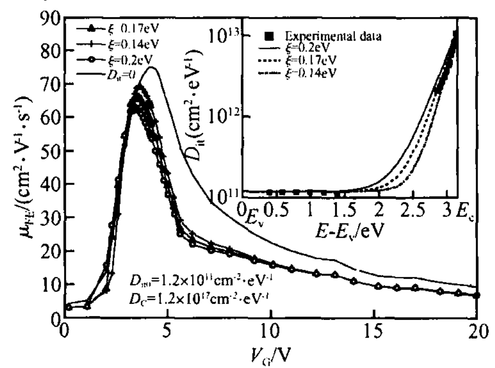

Fig. 5　Effect of non-uniform interface states density on field-effect mobility

than that caused by uniform interface states, as shown in Fig. 6. Usually the surface of a semiconductor is in depletion and the Fermi energy level is far from the bottom of the conduction band E_C corresponding to the point of peak field-effect mobility, while the interface state density is smal-

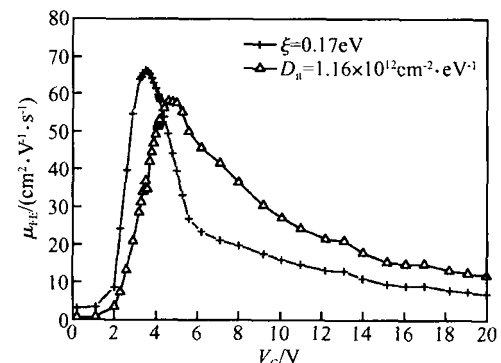

Fig. 6　Dependence of field-effect mobility on gate voltage for different interface state distributions

ler than the average interface state density. With the increase of the gate voltage, the Fermi energy level moves forward E_C and the related interface state density increases exponentially, so a greater reduction of the field-effect mobility is observed. When the gate voltage is larger than the flatband voltage, the Fermi energy is very close to E_C, and the interface state density is so large that the effect of interface states is not screened completely by the carriers in the accumulation layer.

6 Conclusion

A buried channel MOS structure can be used to reduce the effect of surface scattering and improve channel carrier mobility. But the influence of the interface states on carrier mobility in the channel cannot be completely avoided. Surface band bending varies with gate voltage, as do charged interface states. This phenomenon leads to the decrease of channel conductance and transconductance and lowers the extracted effective mobility and field-effect mobility. The series resistance has also the same role of decreasing mobility.

A simple quadratic polynomial has been proposed to analyze the effect of series resistance on peak field-effect mobility. The peak field-effect mobility has a linear relation with the average interface state density. The gate voltage corresponding to the peak field-effect mobility decreases linearly with series resistance and varies slightly at different interface state densities. The effects of non-uniform interface states can be ignored at lower gate voltages but become more obvious with the increase of the gate voltage.

Our 4H-SiC BC-MOSFET has exhibited excellent improvement of mobility. The intrinsic peak field-effect mobility can reach $75cm^2/(V\cdot s)$, but it is still smaller than bulk mobility because of the surface roughness. We conclude that reducing the series resistances and improving the SiO_2/SiC interface quality are also important for attaining good performance of 4H-SiC BC-MOSFETs.

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4H-SiC 隐埋沟道 MOSFET 迁移率的研究*

郜锦侠　张义门†　张玉明

(西安电子科技大学微电子学院 宽禁带半导体材料与器件教育部重点实验室, 西安　710071)

摘要: 研究了几种因素对 4H-SiC 隐埋沟道 MOSFET 沟道迁移率的影响. 提出了一个简单的模型用来定量分析串联电阻对迁移率的影响. 串联电阻不仅会使迁移率降低,还会使峰值场效应迁移率所对应的栅压减小. 峰值场效应迁移率和串联电阻的关系可用一个二次多项式来准确描述. 详细分析了均匀分布和不均匀分布的界面态对场效应迁移率的影响. 对于指数分布的界面态,低栅压下界面态的影响基本上可以忽略不计,随着栅压的增加,界面态的影响越来越显著.

关键词: 4H-SiC; 隐埋沟道; MOSFET; 迁移率; 串联电阻; 界面态

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† 通信作者: Email: ymzhang@xidian.edu.cn

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