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Breakdown Voltage and Charge to Breakdown Investigation of Gate Oxide of 0.18μm Dual Gate CMOS Process with Different Measurement Methods

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Abstract: Breakdown voltage (V_{bd}) and charge to breakdown (Q_{bd}) are two parameters often used to evaluate gate oxide reliability. In this paper, we investigate the effects of measurement methods on V_{bd} and Q_{bd} of the gate oxide of a 0.18μm dual gate CMOS process. Voltage ramps (V-ramp) and current ramps (J-ramp) are used to evaluate gate oxide reliability. The thin and thick gate oxides are all evaluated in the accumulation condition. Our experimental results show that the measurement methods affect V_{bd} only slightly but affect Q_{bd} seriously, as do the measurement conditions. This affects the I-t curves obtained with the J-ramp and V-ramp methods. From the I-t curve, it can be seen that Q_{bd} obtained using a J-ramp is much bigger than that with a V-ramp. At the same time, the Weibull slopes of Q_{bd} are definitely smaller than those of V_{bd}. This means that V_{bd} is more reliable than Q_{bd}. Thus we should be careful to use Q_{bd} to evaluate the reliability of 0.18μm or beyond CMOS process gate oxide.

Key words: gate oxide reliability; voltage to breakdown; charge to breakdown; voltage ramp; current ramp
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1 Introduction

Complementary MOS (CMOS) devices with reduced dimensions and thinner gate oxides are needed to increase integrated circuit performance and integration[1]. As the heart of MOS devices, gate oxide reliability has always been a major factor determining the feasibility of MOS devices[2,3]. Breakdown voltage (V_{bd}) and charge to breakdown (Q_{bd}) are two parameters often used to evaluate gate oxide reliability[4]. But there are several ways to get V_{bd} and Q_{bd}, including the use of a voltage ramp (V-ramp) or current ramp (J-ramp). Especially for Q_{bd}, constant voltages and constant currents are also used by researchers and engineers[5]. In this paper, V-ramps and J-ramps are used to evaluate gate oxide reliability for dual gate oxide CMOS processes. From previous literature[1,2], the breakdown mechanism associated with the V-ramp method is dominated by the electric field, while for the J-ramp method, it is dominated by current. When we use V_{bd} and Q_{bd} as the evaluation criteria for gate oxide reliability, the effects of measurement methods on V_{bd} and Q_{bd} should be well understood. Our experimental results for the gate oxide of a 0.18μm dual gate CMOS process show that the measurement methods affect V_{bd} only slightly. But Q_{bd} is seriously affected by the measurement methods and conditions. The reason for above phenomena is proposed below.

2 Experiment

The devices used throughout this study were 3nm thick oxides for low-voltage devices (thin oxide) and 6.7nm for high-voltage devices (thick oxide) of nMOS and pMOS capacitors, and all have an area of 1mm^2. These devices were prepared by Huahong NEC Electronic Company with a standard 0.18μm dual gate CMOS process. V_{bd}

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and Q_{bd} were measured on an HP 4071 semiconductor parameter analyzer with the aid of PDQ-WLR software. The breakdown point was detected with the SILC method for thin oxide. Measurement results were analyzed using the Weibull distribution.

3 Results and discussion

V_{bd} and Q_{bd} are two parameters often used to evaluate gate oxide reliability. There are several methods to measure V_{bd} and Q_{bd}. In this paper, we use the V-ramp and J-ramp methods. The two-parameter Weibull distribution is usually used in data distribution analysis. For a fixed value x, there is a fixed probability F. As a function of x, F is given by

$$F = 1 - \exp(-(x/\eta)^{\beta})$$

$$\ln(-\ln(1 - F)) = \beta\ln(x/\eta)$$

where β is the shape parameter and η is the characteristic value of x. If the ln (-ln (1- F)) versus ln x curve is available, the slope of this linear curve is just β. The greater β is, the better the distribution is. When ln (-ln (1- F) = 0 (or F = 0.632), the value of x is just η, the characteristic value of x.

Figures 1 and 2 show the V_{bd} Weibull distribution of thin oxide nMOS and pMOS capacitors in one wafer obtained using the V-ramp and J-ramp methods. From the figures, it can be seen that there is no big difference between the results of the two measurement methods. The Weibull slope is relatively large and the fit line shape is good. For a thick gate oxide, similar results can be found. Figures 3 and 4 are the V_{bd} distribution of thick oxide nMOS and pMOS capacitors.

Values of Q_{bd} for thin oxide capacitors obtained using the J-ramp and V-ramp methods are shown in Figs. 5 and 6. Some big difference in Q_{bd} can be found between the two methods. The Q_{bd} obtained with the J-ramp method was much bigger than that with the V-ramp method. Furthermore, the Weibull distribution curve is not as good as that of the above V_{bd}. Also, similar results are available for thick oxide nMOS and pMOS capacitors (Figs. 7 and 8). The Weibull slopes of Q_{bd} are definitely smaller that those of V_{bd}. This means that V_{bd} is more reliable than Q_{bd}. So we should be careful when we use Q_{bd} to evaluate gate oxide reliability of a 0.18μm CMOS process. It is better to use V_{bd} as the evaluation criterion.

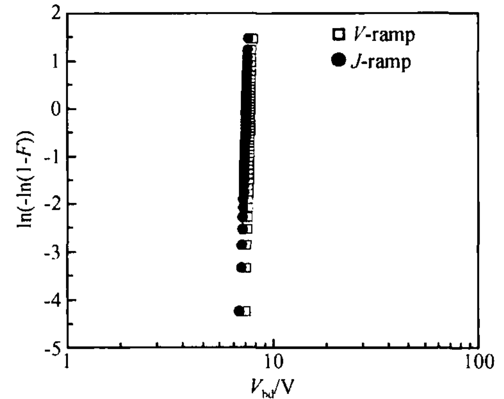

Fig. 1 V_{bd} Weibull distribution of thin oxide nMOS capacitor with J-ramp and V-ramp

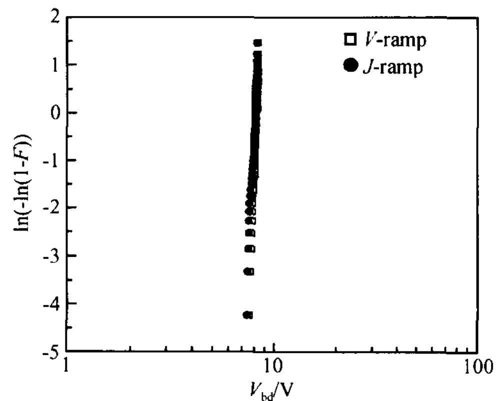

Fig. 2 V_{bd} Weibull distribution of thin oxide pMOS capacitor with J-ramp and V-ramp

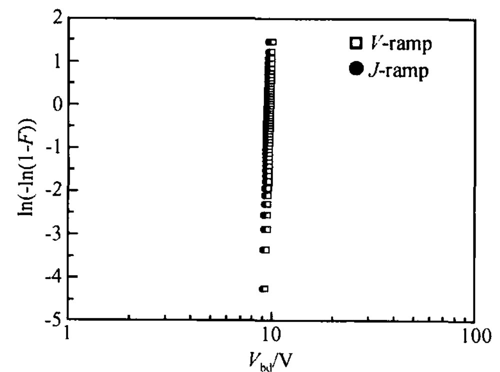

Fig. 3 V_{bd} Weibull distribution of thick oxide nMOS capacitor with J-ramp and V-ramp

From the above results, it can be found that measurement methods affect V_{bd} only slightly. But Q_{bd} can be seriously affected by measurement methods and conditions. We suppose that this re-

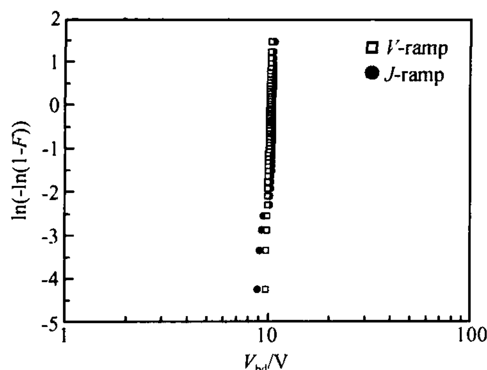

Fig. 4 V_{bd} Weibull distribution of thick oxide pMOS capacitor with J-ramp and V-ramp

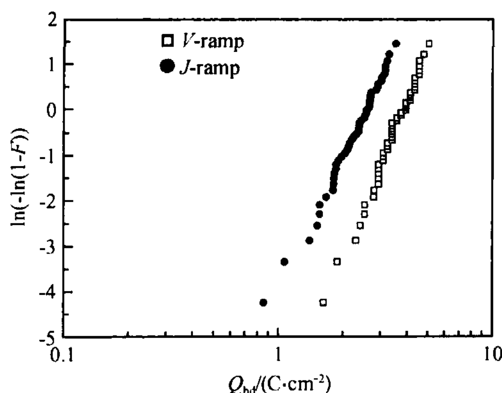

Fig. 7 Q_{bd} Weibull distribution of thick oxide nMOS capacitor with J-ramp and V-ramp

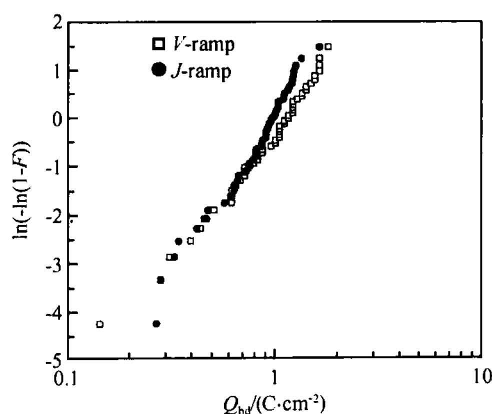

Fig. 5 Q_{bd} Weibull distribution of thin oxide nMOS capacitor with J-ramp and V-ramp

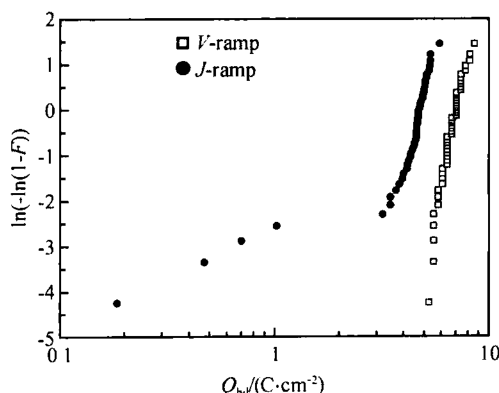

Fig. 8 Q_{bd} Weibull distribution of thick oxide pMOS capacitor with J-ramp and V-ramp

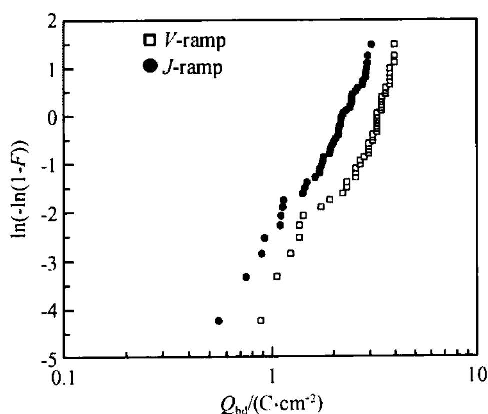

Fig. 6 Q_{bd} Weibull distribution of thin oxide pMOS capacitor with J-ramp and V-ramp

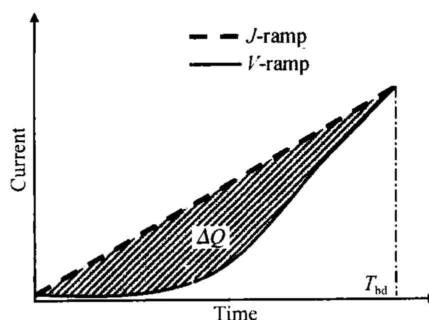

Fig. 9 Current versus time curves of J-ramp and V-ramp

sults in different current versus time curves for the J-ramp and V-ramp (Fig. 9). From Fig. 9, we can see that for the V-ramp curve the current is very small at low voltages. The current increases dramatically just as the voltage approaches V_{bd}. But for the J-ramp curve, the current increases linearly with the current source until the stress field reaches the breakdown field. Thus Q_{bd} for the J-ramp was much bigger than that for the V-ramp. In Fig. 9, ΔQ is just the difference between the Q_{bd} obtained by the J-ramp and V-ramp methods. However for V_{bd}, it is normally determined by the breakdown electrical field, so measurement methods affect it only slightly. At the

same time, the Weibull slopes of Q_{bd} are definitely smaller that those of V_{bd}. This means that V_{bd} is more reliable that Q_{bd}. Thus we should be careful when we use Q_{bd} to evaluate the gate oxide reliability of a 0.18μm CMOS process. It is better to use V_{bd} as the evaluation criterion.

4 Conclusion

In this paper, we investigated the gate oxide reliability for dual gate oxide CMOS processes with the V-ramp and J-ramp methods. The effect of the measurement methods on V_{bd} and Q_{bd} was considered. Our experimental results show that the measurement methods affect V_{bd} only slightly. But Q_{bd} can be seriously affected by the measurement methods and conditions. This results in different current versus time curves of J-ramp and V-ramp methods. At the same time, the Weibull slopes of Q_{bd} are definitely smaller than those of V_{bd}. It is better to use V_{bd} as the criterion to evaluate gate oxide reliability of a 0.18μm CMOS process.

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用不同方法评价 0.18μm CMOS 工艺栅氧击穿电压和击穿电量

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摘要: 利用击穿电压和击穿电量这两个参数评价标准 0.18μm CMOS 工艺栅氧的可靠性,获得击穿电压和击穿电量的两个常用方法是电压扫描法和电流扫描法. 对用这两种方法得到的击穿电压和击穿电量进行了对比. 通过对比,发现测试方法对击穿电压的影响非常小. 但是测试方法却可以在很大程度上影响击穿电量. 用电流扫描法获得的击穿电量要比用电压扫描法的要大,这一差别可以从两种方法不同的电流 - 电压曲线中得到解释. 同时,通过考察 Weibull 分布的斜率还发现,击穿电压值的分布斜率要比击穿电量大的多,而且曲线拟合得更好. 这说明用击穿电压获得的分析结果更可靠. 综合以上结果,可以认为对 0.18μm CMOS 工艺可靠性评价而言,击穿电压是比较合适的评价指标.

关键词: 栅氧可靠性; 击穿电压; 击穿电量; 电压扫描; 电流扫描

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