A New CMOS Image Sensor with a High Fill Factor and the Dynamic Digital Double Sampling Technique

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Abstract: A single CMOS image sensor based on a 0.35μm process along with its design and implementation is introduced. The architecture of an active pixel sensor is used in the chip. The fill factor of a pixel cell can reach 43%, higher than the traditional factor of 30%. Moreover, compared with the conventional method whose fixed pattern noise (FPN) is around 0.5%, a dynamic digital double sampling technique is developed, which possesses simpler circuit architecture and a better FPN suppression outcome. The CMOS image sensor chip is implemented in the 0.35μm mixed signal process of a Chartered by MPW. The experimental results show that the chip operates well, with an FPN of about 0.17%.

Key words: active pixel; CMOS image sensor; fill factor; dynamic digital double sampling; fixed pattern noise
EEACC: 1280; 2570A
CLC number: TN4 **Document code:** A **Article ID:** 0253-4177(2006)02-0313-05

1 Introduction

CMOS image sensors have been becoming increasingly significant in the field of solid image sensors. Compared with CCD image sensors, CMOS image sensors possess many advantages, such as smaller size, more convenient integration with other devices, lower power consumption, and lower cost[1,2]. To date, CMOS image sensors are adopted in almost all mobile phone cameras. In addition, CMOS image sensors have been widely used in digital cameras, PDAs, PC cameras, video telephones, etc.

The fill factor of a pixel is the ratio of sensitive area to the whole area of the pixel. The larger the sensitive area is, the higher the sensitivity of the pixel is. A conventional pixel of APS architecture[3] possesses a fill factor of around 30%[4]. To avoid interference among the wires, a traditional pixel cell uses two-layer wires, while in this paper, four-layer wires are applied to realize a fill factor of 43%, and the resulting interference is minimized by optimizing the design and layout of the three transistors in each pixel cell.

The general double sampling technique (GDS) is a traditional fixed pattern noise (FPN) suppression technique[4]. The FPN is reduced by reading out pixel and reset signals to a difference amplifier. Since the reset and pixel signals are read out through a close signal path, the FPN cannot be completely eliminated. In addition, it is difficult to design and place the column difference amplifier under the limits of pixel pitch, and more random noise is introduced because of its comparatively complicated architecture. After eliminating FPN, this noise becomes one of the factors affecting image quality. Thus a new technique, named the dynamic double sampling technique, is developed in this paper. The pixel and reset signals are read out through the same path, so the FPN is greatly reduced in one difference operation and can be ignored. The design of the readout path is simplified, which makes designing the column and output amplifier into the structure as the difference amplifier unnecessary. At the same time, the random noise introduced is reduced. Moreover, the pixel pitch is minimized to reduce chip area and increase the sensor's resolution.

2 Pixel cell design

2.1 Normal CMOS APS structure

The schematic of a normal CMOS APS struc-

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Received 9 May 2005, revised manuscript received 1 September 2005

ture is shown in Fig. 1 (a). Transistor M1 is the reset transistor of the charge-sensing node at N. M2 is the in-pixel amplifier connected as a source follower with an off-pixel current source M4. A switch M3 is used to select the pixel to be connected to the readout bus. D is a photodiode, and C_p is the capacitance of the node at N[5]. In this structure, the highest output voltage V_{out} is limited by the two drops that result from the nMOS's M1 and M2 to guarantee a proper bias condition. The maximum available output swing is thus given by $V_{CC} - 2V_{tn} - V_{dsat}$ (V_{tn} and V_{dsat} are the threshold voltage and saturation voltage of the nMOS transistor, respectively). The output swing of a CMOS APS is shown in Fig. 1 (b).

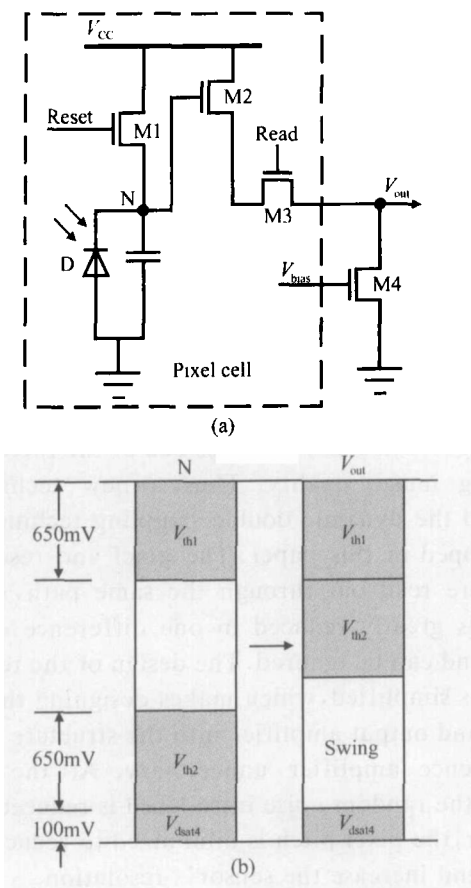

Fig. 1 (a) Schematic of the normal APS; (b) Voltage diagram at node N and V_{out}

2.2 Layout of pixel cell

The layout of the transistors and photodiode in the pixel cell are all optimized according to the requirements of process and array. In Fig. 2, which shows the layout of the pixel cell, the source area of M1 expands to form a large sensitive area (n^+p^- photodiode). Taking full advantages of the four layers of metals, power wire, signal output wire, read signal wire, and reset signal wire, are logically positioned in the layout of the pixel cell. The layout optimization of M1, M2, and M3 ensures that the source area of M1 will occupy a large scope in the pixel cell in order to form a large sensitive area. The area of the pixel cell is 42.25μm^2 (6.5μm ×6.5μm). The sensitive area is 23.3μm^2, with a fill factor of 55%. After the application of the salicide process, in which the active source area is covered by metal silicide, visible light cannot pass through. Thus, an SAB layer (salicide block mask) should be used to cover the source area of M1 to make it transparent to visible light. Covered by the SAB layer, the sensitive area retained is 18.2μm^2, with an actual fill factor of 43%.

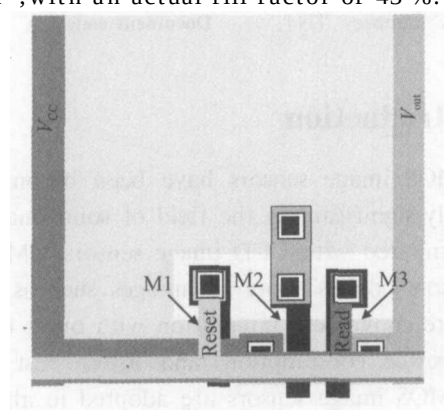

Fig. 2 Layout of pixel cell

3 FPN suppression and DDDS technique

3.1 Fixed pattern noise suppression

FPN caused by device mismatch and process variation has always been a problem with active pixel sensors because of multiple readout paths[6,7]. Two types of FPN have been reported, namely, pixel FPN, which is caused by a mismatch in the cell circuit, and column FPN, caused by a mismatch in the column readout circuits. The threshold voltage mismatch of the source follower transistors is the dominant effect on the pixel FPN and column FPN. Usually, the column FPN is considered to be more serious because the human eye is more sensitive to regular line patterns[8]. The general double sampling technique, shown in

Fig. 3, is the traditional approach used to reduce the fixed pattern noise. The pixel FPN is reduced by reading out the pixel and reset signals to the column difference amplifier. The column FPN is eliminated by reading out the output signal of the column difference amplifier and the compensation signal to the output difference amplifier. To generate the compensation signal, a column difference amplifier with a "cow-bar" must be developed or an additional row, which is shielded by a metal layer, must be added. Still, since the reset signal and pixel signal are read out through a close signal path, the FPN cannot be completely eliminated.

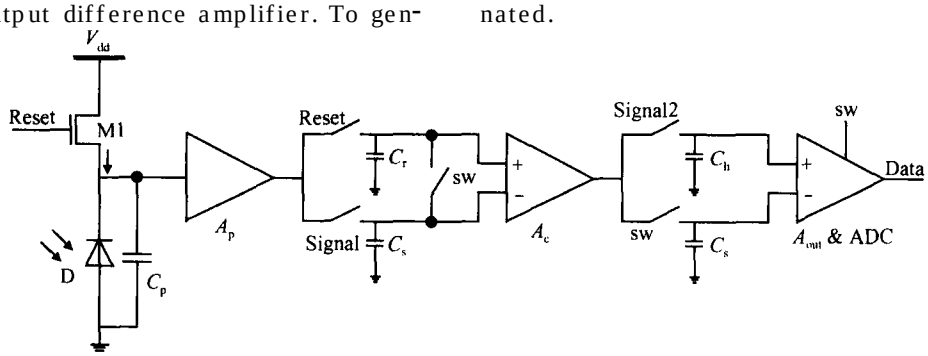

Fig. 3　Diagram of general double sampling

3.2 Dynamic digital double sampling

We develop an improved double sampling technique, namely, DDDS, as shown in Fig. 4. The readout process can be divided into two steps. First, the reset signal of each pixel in the array is read out and stored into memory by converting it into a digital signal through ADC, which is used as FPN background in the pixel array. Then, the signal value of the pixel is read out and the FPN background noise of the correlated position is subtracted after converting the signal into a digital signal through ADC. Since these two values are read out through the same path, the pixel FPN and column FPN are greatly reduced in one difference operation, so that it can be ignored. The dynamic renewal of FPN background results in effective noise suppression.

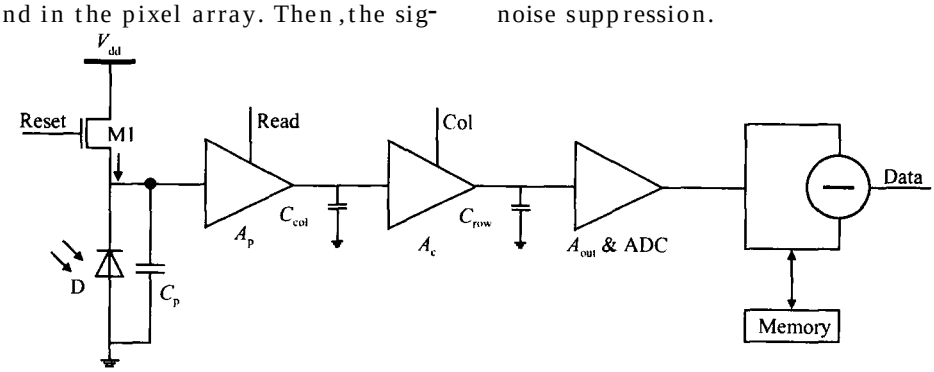

Fig. 4　Diagram of dynamic digital double sampling

$$V_{data} = A_p A_c A_{out} V_{signal} \quad (1)$$

$$V_{data} = A_p A_c A_{out} V_{signal} \pm A_{out} \Delta V_{Aout} \pm \Delta V_{diff} \quad (2)$$

Equations (1) and (2) are the final results of the FPN suppression when DDDS (Fig. 4) and GDS (Fig. 3) are used, respectively. A_p, A_c, and A_{out} are the gains of the pixel amplifier A_p, column amplifier A_c, and output amplifier A_{out}; V_{signal} is the image signal voltage; ΔV_{Aout} is the fixed pattern noise of the output amplifier; ΔV_{diff} is the difference between close output paths. From Eq. (2), we can see that the offset of the output amplifier itself (ΔV_{Aout}) and the difference between close output paths (ΔV_{diff}) are added to output signals in addition to the image signals; while in Eq. (1), the image signal is only the output signal. Thus, DDDS has higher precision, and it produces an image closer to reality. The FPN is 0.17 % when dynamic digital double sampling is used, but that of GDS is 0.5 %[4]. In Fig. 3, the

column amplifier and output amplifier require the architecture of difference amplifier; while Figure 4 is free from the restrictions of this architecture, the source follower is used to realize these two amplifiers in our design of the prototype chip. Through this method, the quantity of amplifier transistors is reduced greatly; the chip becomes smaller or higher resolution can be realized within the same area of the chip. Besides random noise sources, which are the same as those caused by DDDS, GDS has extra random noise generated by the capacitors C_r, C_s, C_h, C_c. These noises increase the GDS system noise.

4 Testing and characterization

The chip was fabricated in a 0.35μm 2P4M CMOS mixed signal process. The dimensions of a sensor are 3.085mm ×2.915mm. Dummy cells and double guard rings are inserted around the sensor cell array to reduce substrate coupling of the digital switching noise. An 8bit pipeline analog-to-digital converter (ADC, provided by others) is used to perform the video rate of analog-to-digital conversion. The die photo of the image sensor chip is shown in Fig. 5.

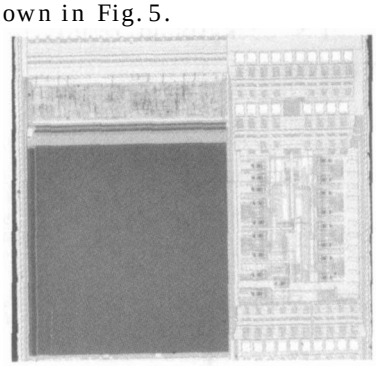

Fig. 5 Photo of the image sensor chip

The fill factor is 43 %, higher than that of a general APS pixel cell, which is 30 %. The FPN is 0.5 % of the saturation output voltage when general double sampling is used, while the FPN is only 0.17 % of the saturation output voltage when dynamic digital double sampling is used. The suppression effect of the second method is almost twice that of the first.

Figure 6 (a) is an image without dynamic digital double sampling; Figure 6 (b) is an image with dynamic digital double sampling. Obviously, the image quality was improved greatly when dynamic digital double sampling was used. A summary of the characteristics of the test chip is given in Table 1.

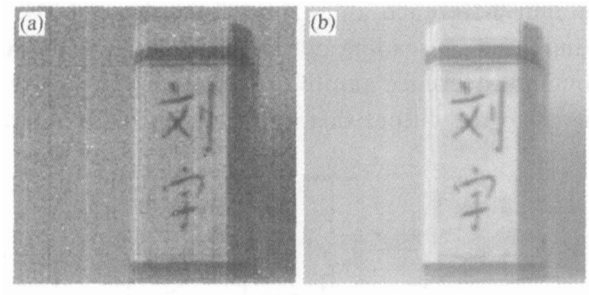

Fig. 6 (a) Image without dynamic digital double sampling; (b) Image with dynamic digital double sampling

Table 3 Characteristics summary of image sensor test chip

Technology	0.35μm 2P4M
Chip size	3.085mm ×2.915mm
Number of pixels	256 ×256
Pixel size	6.5μm ×6.5μm
Load capacitor of node D	29fF
Conversion gain	5μV/electron
Fill factor	43 %
Saturation level	1.3V
Power supply	3.3V
Maximum frame rate	75fps

5 Conclusion

This paper introduces a CMOS active pixel sensor. It applies a DDDS technology to eliminate FPN in pixel and column circuits and processes a high fill factor, which contributes to the increase of sensitivity. However, the adoption of the DDDS technique requires an additional memory, the drawback of which is compensated for by using an advanced DRAM technology. A test chip has been fabricated using a 0.35μm CMOS process. The experimental results validate that FPN can be suppressed effectively by the DDDS technique.

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一种具有高填充因数和动态数字双采样技术的 CMOS 图像传感器

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摘要：介绍了基于 0.35μm 工艺设计的单片 CMOS 图像传感器芯片. 该芯片采用有源像素结构，像素单元填充因数可达到 43 %，高于通常 APS 结构像素单元 30 %的指标. 此外还设计了一种数字动态双采样技术，相对于传统的双采样技术(固定模式噪声约为 0.5 %)，数字动态双采样技术具有更简洁的电路结构和更好抑制 FPN 噪声的效果. 传感器芯片通过 MPW 计划采用 Chartered 0.35μm 数模混合工艺实现. 实验结果表明芯片工作良好，图像固定模式噪声约为 0.17 %.

关键词：有源像素；CMOS 图像传感器；填充因数；动态数字双采样；固定模式噪声
EEACC：1280；2570A
中图分类号：TN4　　**文献标识码**：A　　**文章编号**：0253-4177(2006)02-0313-05

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2005-05-09 收到，2005-09-01 定稿