A Low Power SRAM/SOI Memory Cell Design

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Abstract: A modified four transistor (4T) self-body-bias structured SRAM/SOI memory cell is proposed. The structure is designed and its parameters are obtained by performance simulation and analysis with TSUPREM4 and MEDICI. The structure saves area and its process is simplified by using the body resistor with buried p^+ channel beneath the nMOS gate instead of the pMOS of 6T CMOS SRAM. Furthermore, this structure can operate safely with a 0.5V supply voltage, which may be prevalent in the near future. Finally, compared to conventional 6T CMOS SRAM, this structure's transient responses are normal and its power dissipation is 10 times smaller.

Key words: SRAM/SOI; memory cell; self body bias; low power
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1 Introduction

A SRAM cell's performance can be enhanced with SOI technology because compared to conventional CMOS technology, SOI has low power dissipation, low noise, high resistance to radiation, and no latch-up effect[1].

In an attempt to reduce power dissipation and layout area, much research has been done to change classic 6T SRAM cells into 4T cells. Some such work is based on circuit level modifications, but the resulting stability is always poor[2]. Other work is based on device modifications, but such processes are too complicated[3]. In this paper, a 4T SRAM cell based on self-body-biased (SBB)[4] and dynamic threshold MOS (DTMOS)[5] structures[6] is modified. While the simulation and analysis of 6T SRAM are carried out with Cadence tool kits, others are carried out with MEDICI and TSUPREM4.

2 Basic structure and mechanism

Figure 1(a) shows the plan view of the SBB SOI MOSFET with a H-shaped gate electrode[6]; Figure 1 (b) shows the cross-section view modified in the plane marked AA′ in Fig. 1 (a). The body resistor with buried p^+ channel beneath the gate from terminal Body1 to terminal Body2 generally functions as a pMOS. When a high voltage is applied to the gate, the p^- area is quickly depleted, thereby greatly enhancing the resistance and shutting down the current between Body1 and Body2, as shown in Fig. 2.

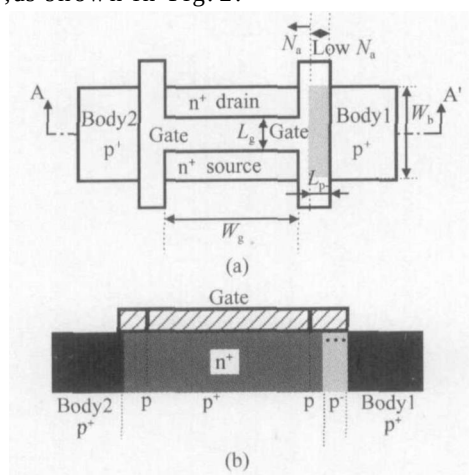

Fig. 1 Plan (a) and cross-section (b) views of H-gate SBB MOSFET

The whole SRAM cell circuit is shown in Fig. 3. Transistors M3 and M4 are DTMOS. Their on-state threshold voltage is low and off-state threshold voltage is high. Because we use a 0.5V supply voltage, the application of DTMOS is safe

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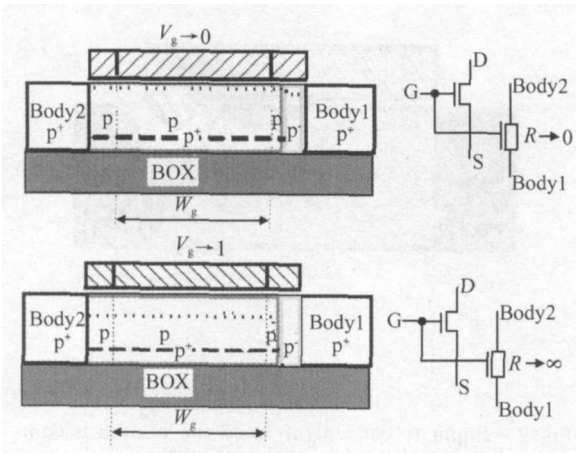

Fig. 2　Operation of the body resistor

and effective.

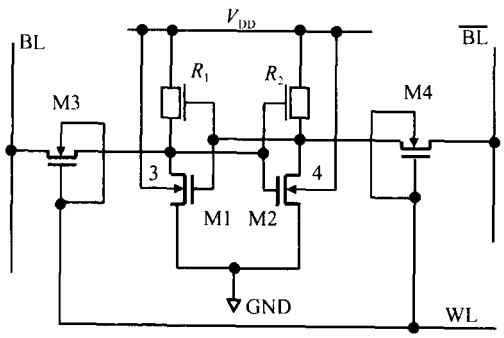

Fig. 3　Proposed 4T SRAM cell circuit

3　Stability analysis

In the proposed H-gate nMOS, there might be a disastrous current flow from substrate to source even though the supply voltage is only 0.5V. To make sure this will not be a problem, we simulate the characteristics of the pn junction under an applied forward voltage of 0.5V using MEDICI. The results are shown in Table 1. If the current flowing between Body2 and Body1 exceeds several nA, the effects of the current flowing between Body2 and the source can be ignored.

Table 1　pn junction currents at various temperatures

T/K	I/(A·μm^{-1})
300	9.46×10^{-11}
310	2.46×10^{-10}
330	1.35×10^{-9}
350	6.31×10^{-9}

4　Design of the body resistor

Figure 4 shows the dependence of the current through the resistor on V_g for various p^- area B concentrations. L_b is the length of the p^- area, which is assumed to be fixed at 0.30μm. We conclude that if other parameters are fixed, the p^- area impurity concentration can be chosen to make the resistor perform as a pMOS.

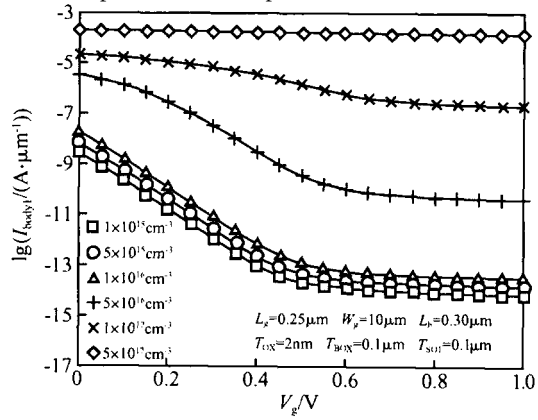

Fig. 4　$I_{body2\text{-}body1}$ versus V_g for different impurity concentrations in the p^- area

The simulation results of the p^- area length's influence on the performance of the resistor are given in Fig. 5. With the variation of L_b, the off state current changes much faster than the on state current.

The thickness of the p^- area is a third factor for further improvement. Local oxidation is applied to the p^- area by wet oxidation for about 20min, and then the SiO_2 is removed leaving shapes around the former p^- area as in Fig. 6. Figure 7 shows $I_{body2\text{-}body1}$ versus V_g curves for 4 different p^- area impurity concentrations, assuming that the equivalent length of the p^- area (L_b) is 0.3μm. Figure 8 shows the $I_{body2\text{-}body1}$ versus V_g curves for various values of L_b, assuming that the impurity concentration of the p^- area is $10^{17}cm^{-3}$. The uptriangle symbol line (L_b = 0.20μm) in Fig. 8 is the best situation with an on-state current close to 10μA and an off-state current of several nA.

After the above steps, the impurity concentration of the p^- area is comparable to that of p area, as shown in Fig. 9. Thus, ion implantation is used to create a buried channel to decrease resistance between Body1 and Body2 and to avoid nMOS threshold variation. Actually, the threshold voltage of nMOS is normally between 0.1 and 0.2V. Figure 10 is the channel impurity concentration curve after ion implantation. Figure 11 shows that the body resistance is enhanced by ion implantation.

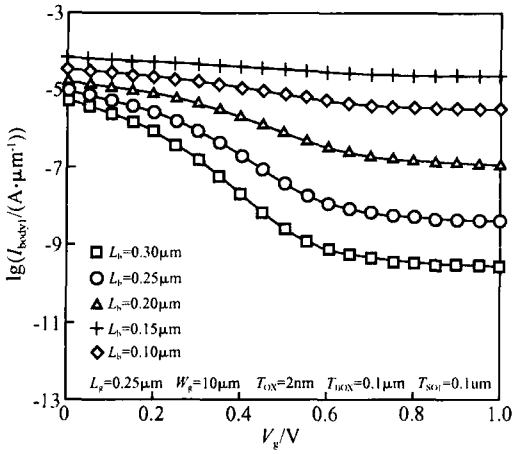

Fig. 5 $I_{body2\text{-}body1}$ versus V_g for different p^- area lengths

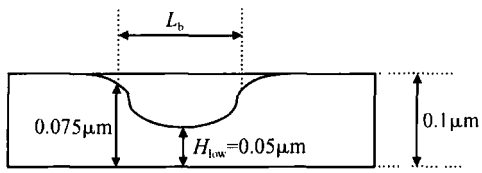

Fig. 6 p^- shape after local oxidation

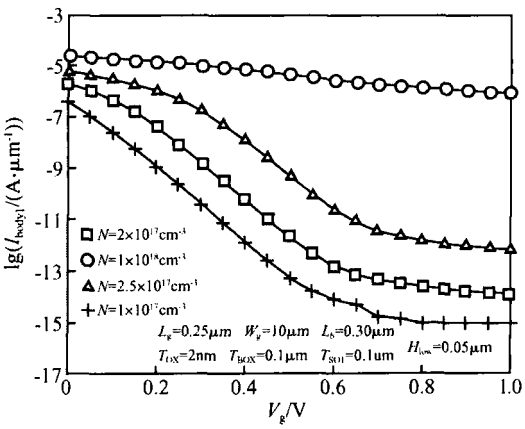

Fig. 7 $I_{body2\text{-}body1}$ versus V_g for various p^- area impurity concentrations

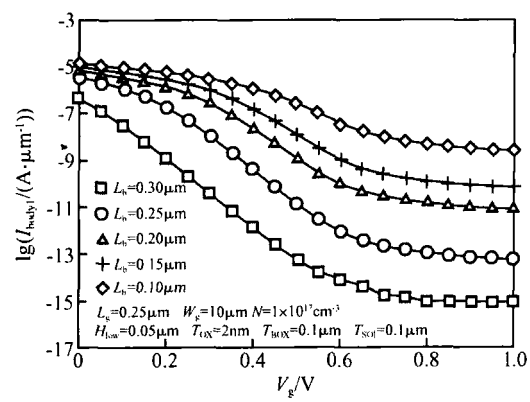

Fig. 8 $I_{body2\text{-}body1}$ versus V_g for various equivalent p^- area lengths

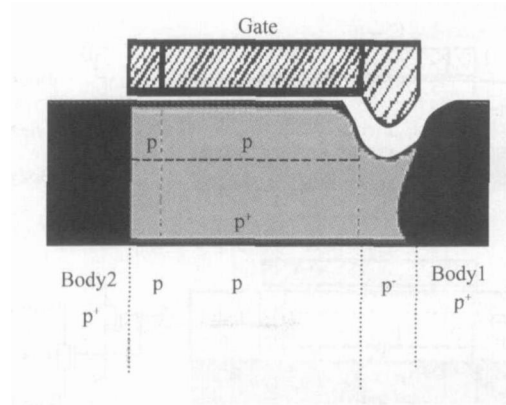

Fig. 9 Impurity concentration of the p^- area is comparable to that of p area

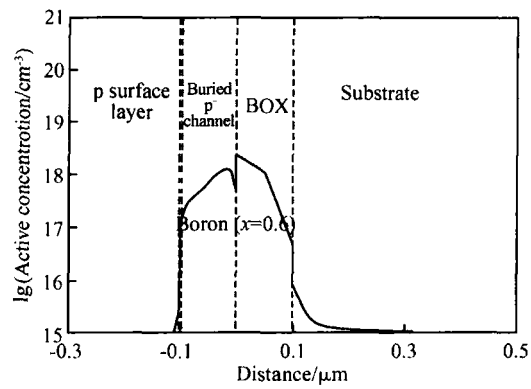

Fig. 10 Buried p^+ channel impurity distribution after ion implantation

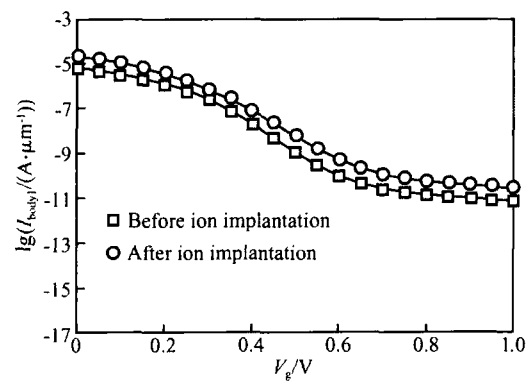

Fig. 11 Current dependence on gate voltage with and without ion implantation

5 Global analysis of SRAM memory cell

The SRAM cell is simulated according to the schematic in Fig. 3. The transfer characteristics described in Fig. 12 show that the 4T SRAM cell functions normally. To compare writing state situ-

ations with a normal 6T SRAM cell, a schematic like Figure 13 is constructed using a composer schematic in the Cadence ICFB environment.

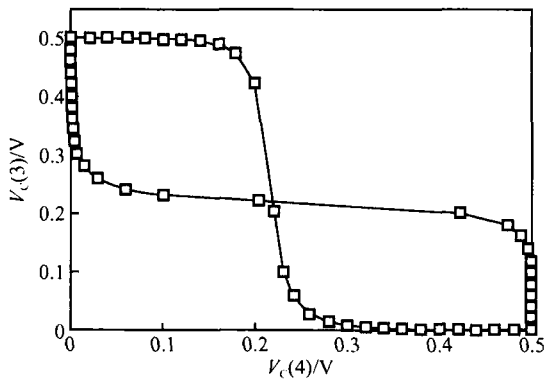

Fig. 12　Transfer curve of the 4T SRAM cell

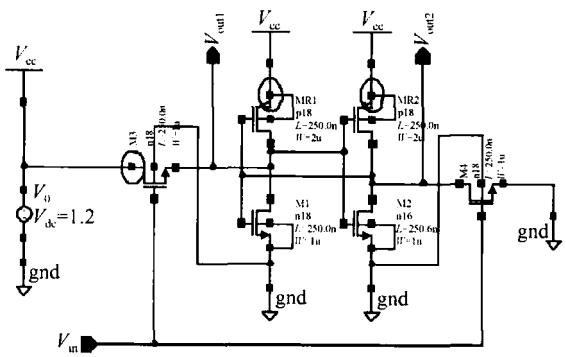

Fig. 13　Schematic of conventional 6T SRAM cell

As shown in Fig. 14, the writing delay of the conventional 6T SRAM is about 250ps. The total current is integrated in 1ns of simulation time with a result of 25fA ·s. Thus the power dissipation is 30μW at a 1.2V supply voltage.

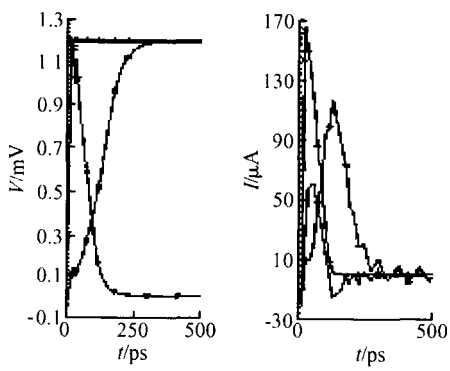

Fig. 14　Transient response of 6T SRAM

Similar simulation results for the 4T SRAM are shown in Fig. 15. The writing delay is 500ps, and its power dissipation is 3.3μW.

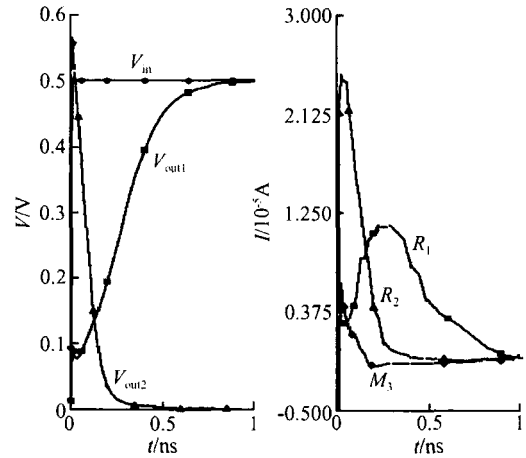

Fig. 15　Transient voltage and current of 4T SRAM

A reading state simulation in 6T SRAM shows that the transfer delay is 200ps, and the power dissipation is 11.9μW. In contrast, the proposed 4T SRAM cell's transfer delay is 500ps, and its power dissipation is 1.7μW.

Thus, whenever it is in the reading or writing states, the proposed 4T SRAM cell has a power dissipation 10 times smaller than a conventional 6T SRAM cell, at the cost of only doubling the transfer delay of the 6T cell.

6　Layout of the SRAM cell

The layout of the 4T SRAM cell with the H-gate SBB structure is shown in Fig. 16. The p$^-$ area is not shown in the structure in order to reduce the complexity. It is located close to GND beneath a terminal of the H-shaped gate.

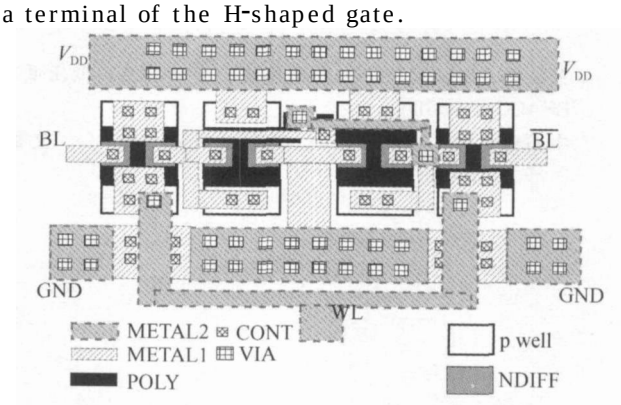

Fig. 16　Layout of the proposed 4T SRAM cell

7　Conclusion

Stability analysis of a basic SBB structure is

processed to ensure that the parasitic pn junction will not affect the function of the SBB structure under a 0.5V supply voltage.

The p^- area of the gate-controlled resistor is the bottleneck of the device performance. Thus, adjustments are made to the p^- area, including its impurity concentration, length, and thickness. The bottom of the nMOS channel is also implanted with boron to enhance the resistor's performance. Finally, the resistor has a 1000 on/off ratio with the shift of gate voltage, and its on-state current is comparable to that of nMOS.

Transfer speed and power dissipation are analyzed by comparing the designed 4T SRAM cell with a conventional 6T cell. Although the transfer speed of the 4T cell is slower, the power dissipation is greatly reduced.

Considering the extremely low power dissipation, the small area of the cell, and the advantages of SOI, this design will be promising when a 0.5V supply voltage becomes prevalent.

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一种低压低功耗 SRAM/SOI 单元设计

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摘要: 提出一种改进 4 管自体偏压结构 SRAM/SOI 单元. 基于 TSUPREM4 和 MEDICI 软件的模拟和结构性能的分析, 设计单元结构并选取结构参数. 该结构采用 nMOS 栅下的含 p^+ 埋沟的衬底体电阻代替传统 6 管 CMOS SRAM 单元中的 pMOS 元件, 具有面积小、工艺简单的优点. 该结构可以在 0.5V 的电源电压下正常工作, 与 6 管单元相比, 该单元瞬态响应正常, 功耗只有 6 管单元的 1/10, 满足低压低功耗的要求.

关键词: SRAM/SOI; 存储单元; 自体偏压; 低压低功耗

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