BSIM Model Research and Recent Progress *

He Jin[1,3,†], Chan Mansun[2,3], Xi Xuemei[3], Wan Hui[3],
Pin Su[1], Ali Niknejad[1], and Hu Chenming[3]

(1 *Institute of Microelectronics, Peking University, Beijing* 100871, *China*)
(2 *Department of Electrical & Electronic Engineering, Hong Kong University of Science & Technology, Hong Kong, China*)
(3 *Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA* 94720, *USA*)

Abstract: The continued development of CMOS technology and the emergence of new applications demand continued improvement and enhancement of compact models. This paper outlines the recent work of the BSIM project at the University of California, Berkeley, including BSIM5 research, BSIM4 enhancements, and BSIMSOI development. BSIM5 addresses the needs of nano-CMOS technology and RF high-speed CMOS circuit simulation. BSIM4 is a mature industrial standard MOSFET model with several improvements to meet the technology requirements. BSIMSOI is developed into a generic model framework for PD and FD SOI technology. An operation mode choice, via the calculation of the body potential ΔV_{bi} and body current/charge, helps circuit designers in the trend of the coexistence of PD and FD devices.

Key words: compact modeling; BSIM5; BSIM4; BSIMSOI; device physics; MOSFETs
EEACC: 2560R; 2560F
CLC number: TN386 **Document code:** A **Article ID:** 0253-4177(2006)03-0388-09

1 Introduction

The continued scaling of CMOS technology provides great challenges for the development of compact models of integrated semiconductor devices[1,2]. The applications of scalable CMOS technologies in analog, RF, microwave circuits, and systems are strongly linked to the accurate modeling of noise, substrate resistance, non-quasi-static (NQS) effects, and device leakage. The precise reproduction of device terminal behavior requires the incorporation of new physical effects and transport mechanisms into a model. The compact model should thus be flexible for easy adoption for various advanced structures and process technologies and accurate for the performance prediction of ULSI circuits.

The BSIM series of compact MOSFET models are industry standard compact models successfully used throughout the semiconductor industry and the research community for digital and analog circuit design. BSIM models are the bridge between semiconductor technology and circuit and system design[3]. The incorporation of new physical effects and enhancements for RF and analog circuit simulation satisfies a critical semiconductor industry need for designs utilizing single gate bulk CMOS, partially depleted SOI, and fully depleted SOI technologies. It is thus crucial to continue model development and enhancement of BSIM4 and BSIMSOI while focusing on analog and RF applications. Furthermore, symmetry, continuity, scalability, computational efficiency, and a minimal number of parameters are desirable properties for the extension of BSIM to the next generation. To address these challenges and satisfy the needs in modeling nano-CMOS, the next generation BSIM model, BSIM5, has been developed based on a new physical core and model architecture. The model results in consistently unified and continuous *I-V* and *C-V* equations that are more analog friendly. The non-charge-sheet formulation also makes the model easily extendible to non-classical CMOS devices like double-gate (DG) MOSFETs[4].

* Project supported by the SRC (Nos. 2002-NJ-1001, 2003-NJ-1134) and partially by the RGC of Hong Kong (No. HKUST6111/03E)
† Corresponding author. Email: jinhe@ime.pku.edu.cn
Received 20 November 2005

This paper reviews the research and the recent progress of the BSIM project at the University of California, Berkeley: BSIM5 research, BSIM4 enhancements, and BSIMSOI development. The BSIM5 model is developed based on basic MOSFET device physics and demonstrates good agreement with numerical and experimental data. BSIM4's several improvements and new enhancements are shown to meet the new technology requirements. BSIMSOI is the extension of BSIM3 to PD and FD devices, with recent updates, e. g. , the unified model framework for PD and FD devices and intelligent model selection. The basic principle of the unified BSIMSOI is elucidated and the RF performance enhancement is also demonstrated.

2 BSIM5 research

The BSIM5 model starts with fundamental 1D MOSFET physics to derive the basic charge and channel current equations, and then extends them to the quasi-2D and 3D cases to include short channel, narrow-channel, poly-silicon depletion and quantum mechanical effects. BSIM5 is a continuous, completely symmetric, and accurate charge-based MOS transistor model including various physics effects, with minimal independent extraction parameters and thus flexibility for advanced process technologies. BSIM5 uses charge density rather than surface-potential as the state variable to construct the model framework from the basic device physics while maintaining computational efficiency and flexibility. The model results in consistent and unified *I-V* and *C-V* equations and robust RF functions[5~7].

The BSIM5 core model is based on the general Poisson equation and Pao-Sah current formulation. The theory derivation starts with the Poisson equation with Gauss's boundary under the background of the gradual channel approximation (GCA) to obtain the first master equation of the surface-potential-plus model concerning the channel charge density.

$$\frac{V_{gb} - V_{fb}}{\beta} - 2\phi_t - V_{ch} - \ln\frac{\beta}{\beta - 1} = \ln\frac{q_1}{\beta} + \frac{q_1}{\beta} \tag{1}$$

Combining the derivative of Eq. (1) with the Pao-Sah current formulation, we derive the second master equation of BSIM5, linking the channel current and the terminal voltages following the Pao-Sah model, the channel current equation:

$$I_{ds} = \frac{\mu W C_{ox} V_t^2}{L}\left[\frac{q_s^2 - q_d^2}{2\beta} + q_s - q_d\right] \tag{2}$$

It is easily found from comparison of the channel current equations between the BSIM5 and the general MOSFET models that this equation already includes both current components: one is the diffusion current, and the other is the drift current.

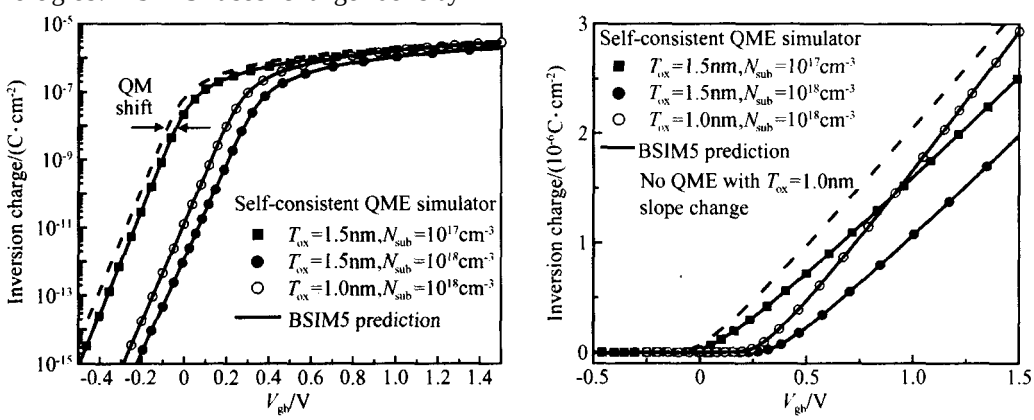

Fig. 1 Inversion charge comparison between the self-consistent simulation and BSIM5 prediction in the sub-threshold region and strong inversion region for different T_{ox} and dopings

Under BSIM5's charge and current formulations, poly-depletion effects and quantum effects can be easily handled by using the n-factor and the effective bulk potential correction. The characteristics of the channel charge distribution including poly-silicon depletion and quantum effects are shown in Figs. 1, indicating good agreement with 2D and quantum numerical simulations.

Velocity saturation, velocity overshoot and ballistic transports are handled in a unified way using the saturation charge concept in the BSIM5 formulation. Analytical modeling of short channel effects in deep sub micron CMOS technologies is a constant challenge. In the BSIM5 framework, we start from the 2D Poisson's equation to handle short-channel effects to extend the BSIM5 model to the 2D case. The model has also been extensively verified by experimental data with gate lengths from 1mm down to 0.125μm. Some examples are given in Figs. 2 and 3.

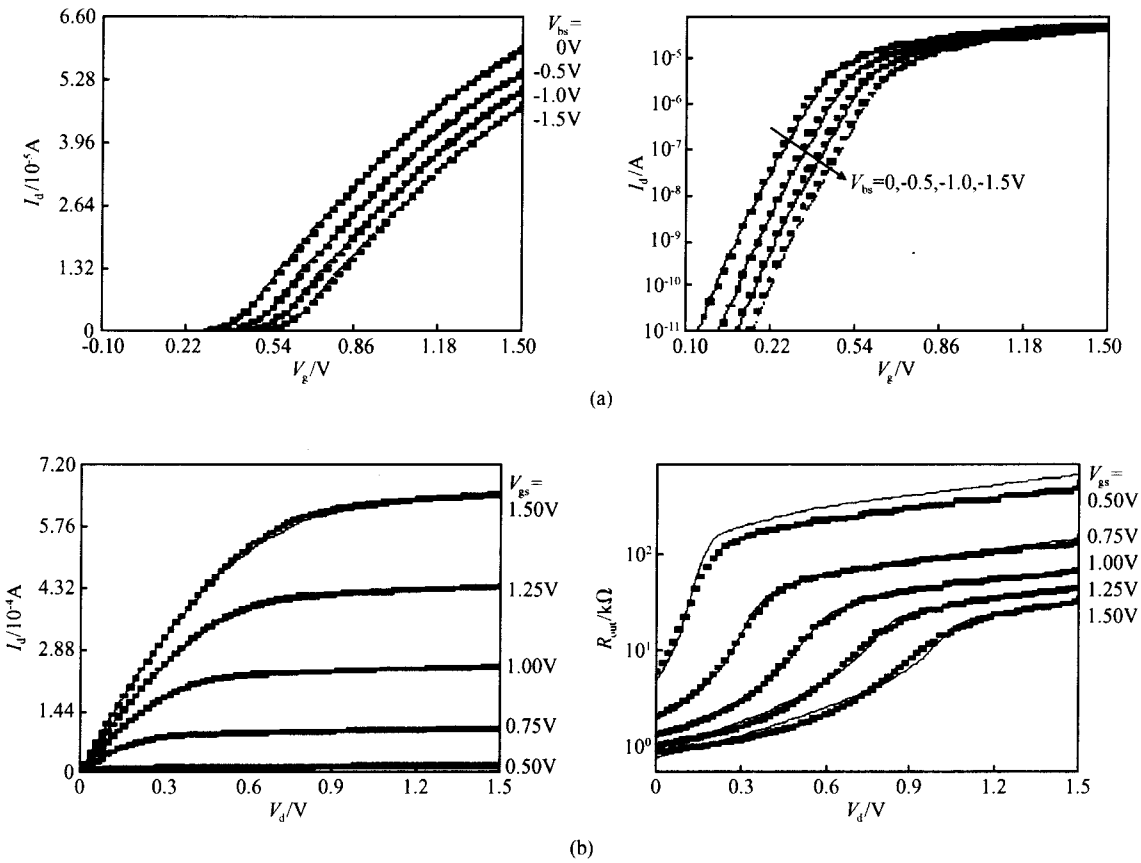

Fig. 2 (a) Comparison of I_{ds} versus V_{gs} between experimental data and BSIM5 fitting for 1μm MOSFET device; (b) Comparison of I_{ds} versus V_{ds} and R_{out} between experimental data and BSIM5 fitting for 1μm MOSFET device

In modern advanced MOS transistor models, symmetry is a basic requirement due to the structure symmetry of the source and drain end and the dynamic sweeping of the bias voltage. The C-V equations in BSIM5 are derived consistently from the symmetric I-V model. Thus, the C-V model is fully symmetric and continuous due to the symmetry of the inversion and current equation as shown in Fig. 4.

3 BSIM4 enhancements

BSIM4 has major improvements and additions on RF functionality, gate tunneling current modeling, current saturation mechanisms, and the stress effects over BSIM3[8]. In the BSIM4 architecture, the RF functionalities were enhanced with an accurate new model of the intrinsic input resistance, flexible substrate resistance network and a new accurate channel thermal noise model and a noise partition model. Figure 5 shows the diagram of the BSIM4 substrate resistance network and the fitting on a LNA fabricated in 0.6μm CMOS. In contrast, the predicted voltage gain of the LNA by BSIM3 shows significant deviation from the measured data.

In the RF/Analog circuit design, the accurate prediction of frequency-related performance such as the Y and S parameters for the multiple networks is very important. Based on the improved substrate network and the input gate resistance modeling, the dependence of Y parameters of the

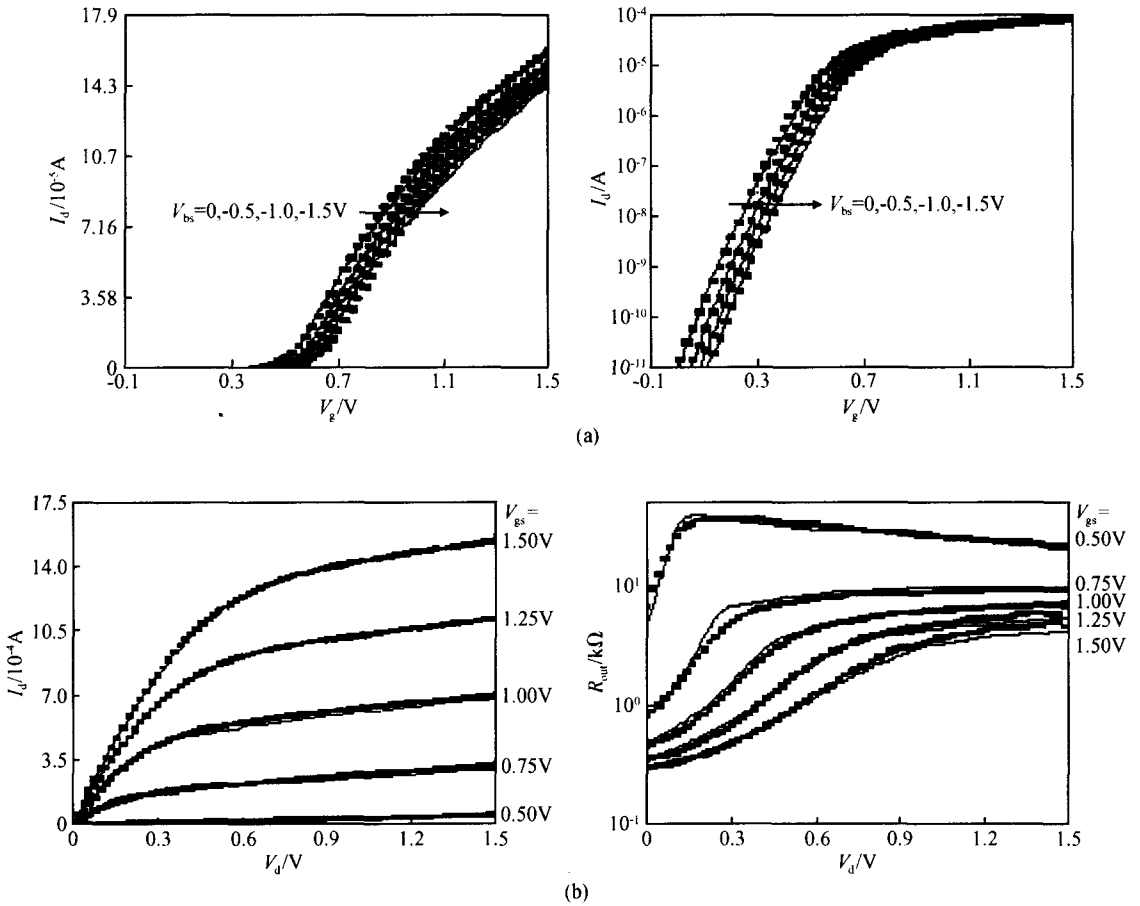

Fig. 3 (a) Comparison of I_{ds} versus V_{gs} between experimental data and BSIM5 fitting for 0.125μm MOSFET device; (b) Comparison of I_{ds} versus V_{ds} and R_{out} between experimental data and BSIM5 fitting for 0.125μm MOSFET device

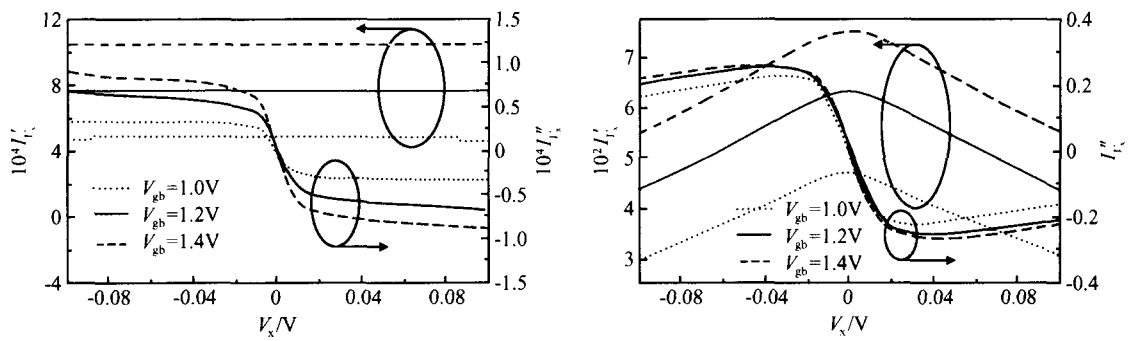

Fig. 4 Symmetry tests of drain current and its high-order derivatives in BSIM5 for 20 and 0.1μm MOSFET devices

two-port network on the frequency up to 20GHz predicted by BSIM4 shows good agreement with the experimental measured values for different MOS transistor lengths, as shown in Fig. 6.

The aggressive scaling of gate-oxide thickness has made gate-tunneling current an essential aspect of MOSFET modeling, and this leakage current density continues to increase for every process generation. Accurate compact models for gate tunneling current and its source/drain partition are extremely critical to valid circuit performance in 90nm technology and beyond. Device leakage behavior was accurately described with an accurate gate direct tunneling model and channel tunneling current partition in BSIM4 by considering three tunneling mechanisms: Electron conductance-band tunneling, electron valence-band tunneling, and the hole valence-band tunneling in the MOSFET transistor.

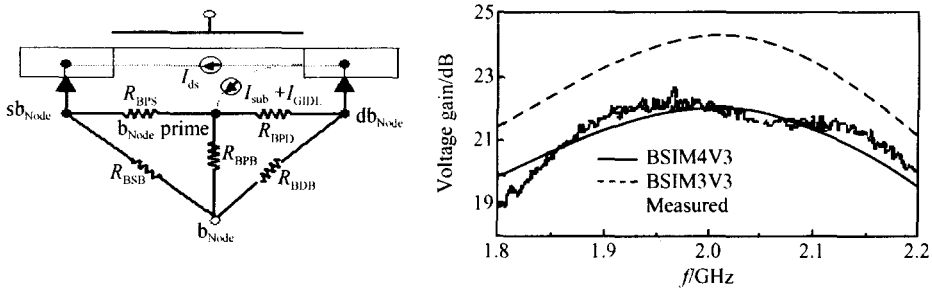

Fig. 5 BSIM4 substrate resistance network and RF function confinement from a prototype LNA was fabricated in 0.6μm CMOS

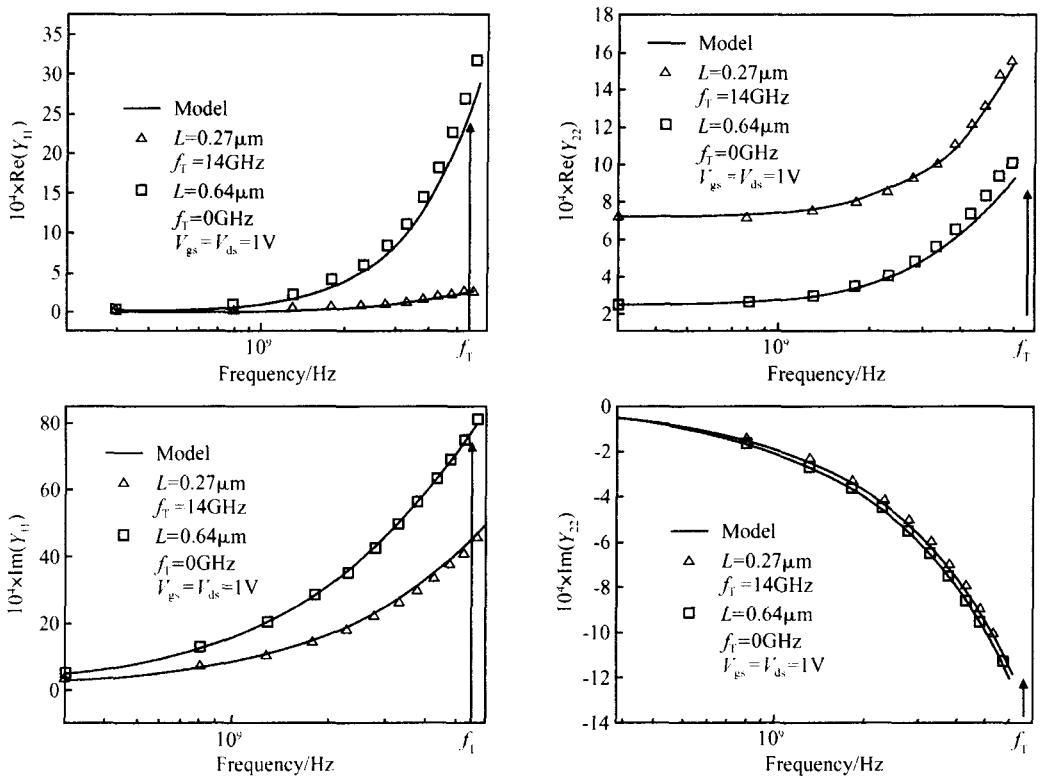

Fig. 6 Comparison of Y parameters of the two-port network MOS transistor between the BSIM4 prediction and the experimental measurements for different device channel lengths

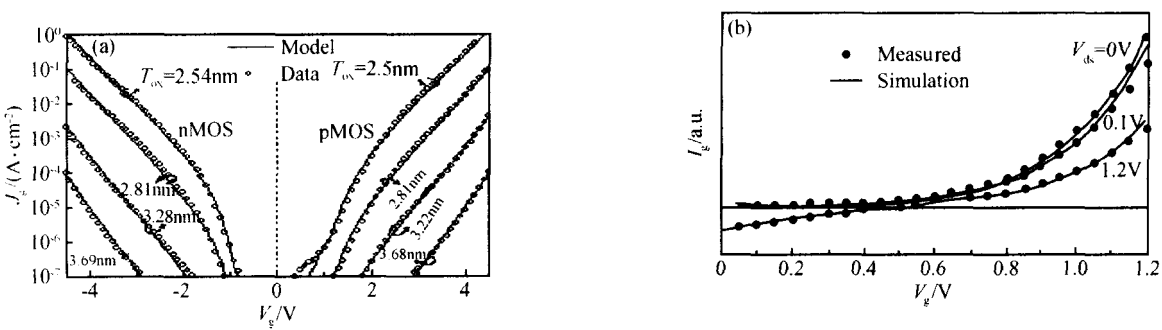

Fig. 7 Gate tunneling current density versus gate voltage (a) and total gate tunneling current versus the source-drain voltage (b)

The lateral non-uniform doping model was improved for Halo or Pocket-implanted devices in BSIM4. Thus, BSIM4 shows better scaling characteristics for different sized MOS transistors. For

example, Halo and Pocket implantation have a strong effect on the output resistance; the BSIM4 prediction demonstrated good agreement with the measured output resistance for the MOSFET transistors with different channel lengths, as shown in Fig. 8

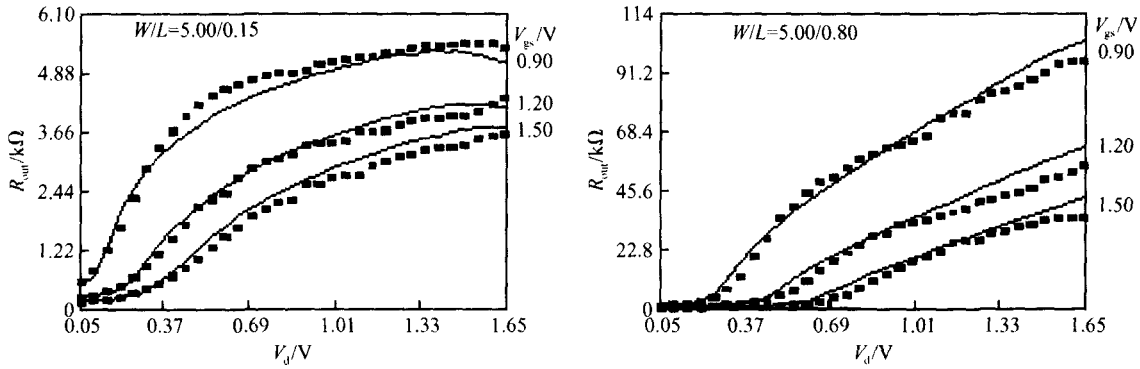

Fig. 8 Comparison of the output resistance between the BSIM4 and the measured values for different channel lengths and gate voltages

Improvements of the transistor drive current for improved circuit performance can be achieved by enhancing the carrier transport in the MOSFET channel. Various strain methods, such as cap layer, SiGe S/D, STI, silicide, spacer, and gate stack, can enhance carrier mobility. Model mobility enhancement is a function of layout geometry: gate length, distance from the shallow trench isolation, and S/D length. BSIM4 has a new scalable isolation-induced stress effect model to capture the mobility and saturation current variation with the process parameters and conditions. Figure 9 shows the model parameter layout dependence in the BSIM4 stress model and the model fitting of the experimental data of the saturation channel current.

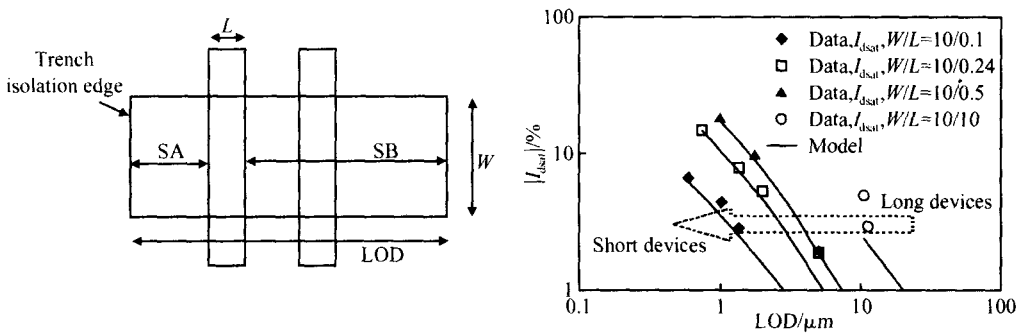

Fig. 9 Stress model parameters SA, SB and LOD layout dependence and comparison of the saturation drain current variation between the BSIM4 model and the measured data

4 BSIMSOI development

Both PD and FD devices may coexist in the same circuit by design. Halo implanting may lead to FD long-channel devices and PD short-channel devices with continuous variations in between. The same device may be PD under some bias conditions and FD under others. Thus, a unified model of the PD-SOI and FD-SOI is required for SOI circuit simulation and design. On the other hand, SOI devices have also been widely used in RF and analog circuits because of their unique advantages; thus, an enhancement of the BSIMSOI's RF functionality is required for SOI circuit simulation and design.

We have explored the essential difference between PD and FD devices, and concluded that the difference regarding the floating-body behavior can be represented by body-source built-in potential lowering ΔV_{bi}[9,10]. The FD model can be made a generalization of the PD model by considering the body-source built-in potential lowering due to vertical capacitive coupling, as shown in Fig. 10. In this case, we can obtain the real source-body potential lowering ΔV_{bi} by measuring the source-body diode current as shown in Ref. [3].

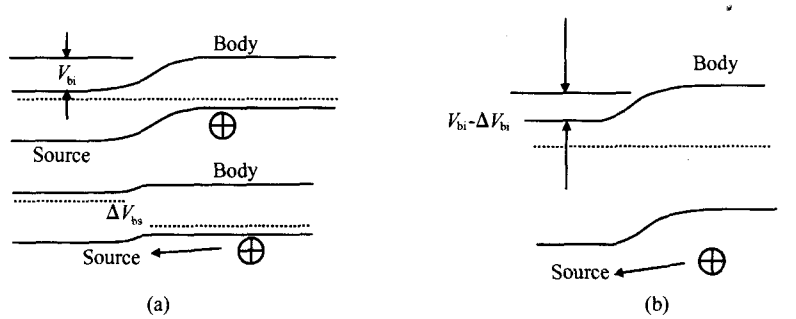

Fig. 10 Comparison of the energy bands of the PD-SOI (a) and FD-SOI (b) and the similarity of both via an effective body-source potential lowering ΔV_{bi}

$$I_{bs} = \exp\left(\frac{\Delta V_{bi}}{kT/q}\right)\exp\left(\frac{V_{bs}}{kT/q} - 1\right) \qquad (3)$$

We have developed a unified SOI model for PD and FD devices showing floating-body behavior using this physical concept. We propose to further construct a generic model framework to deal with various SOI technologies exhibiting various degrees of floating-body effect based on this unified model to gain simulation accuracy and efficiency simultaneously. Figure 11 demonstrates the dependence of V_{bi} on the front-gate and back-gate voltage bias conditions for the given structure parameters and on the channel doping concentration for the given gate biases.

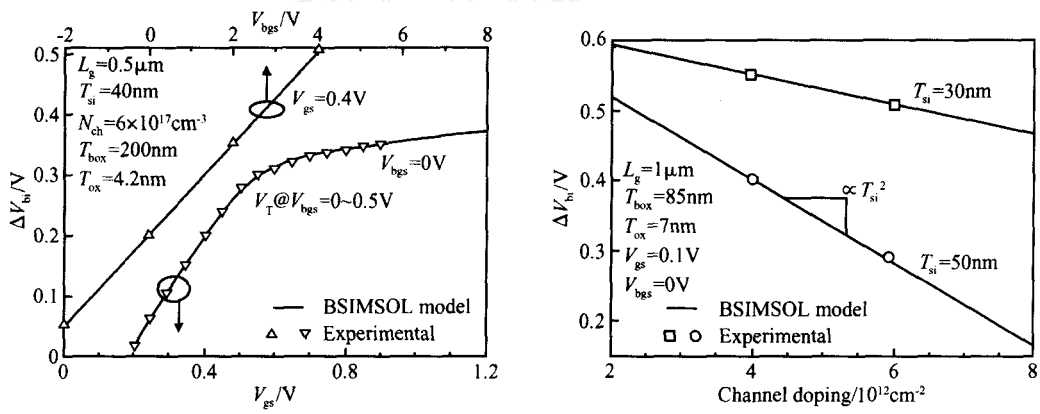

Fig. 11 Dependence of ΔV_{bi} on front gate voltage and back gate voltage for the given structure and process parameters and on the channel doping for the given gate biases

Implementing the lowering of this source-body potential into the threshold voltage model, the unified BSIMSOI framework for PD-SOI and FD-SOI was established. For the unified SOI model both ΔV_{bi} and body current/charge are calculated to capture the floating-body behavior exhibited in FD devices. Figure 12(a) shows the corresponding relation between the threshold voltage and ΔV_{bi} variation with the decrease of the channel length. Integrating the threshold voltage change into the BSIMSOI, the model fits the Please note:the points are the measured data and the line represents the model prediction. The experimental data and the model simulation match measured data for the different channel lengths, as shown in Fig. 12 (b). One can see that the BSIMSOI prediction shows good agreement with the experimental data.

An important feature of the BSIMSOI is to self-consistently model the PD and FD SOI operation mode transition. For the same devices, different back gate combinations can result in different operation modes in the SOI configuration. In this case, BSIMSOI can capture this important transition mechanism from PD to FD as shown in Fig. 13. well in almost all bias regions.

New BSIMSOI releases, e. g. BSIMSOI3. 2 have enhanced analog/RF capabilities via the im-

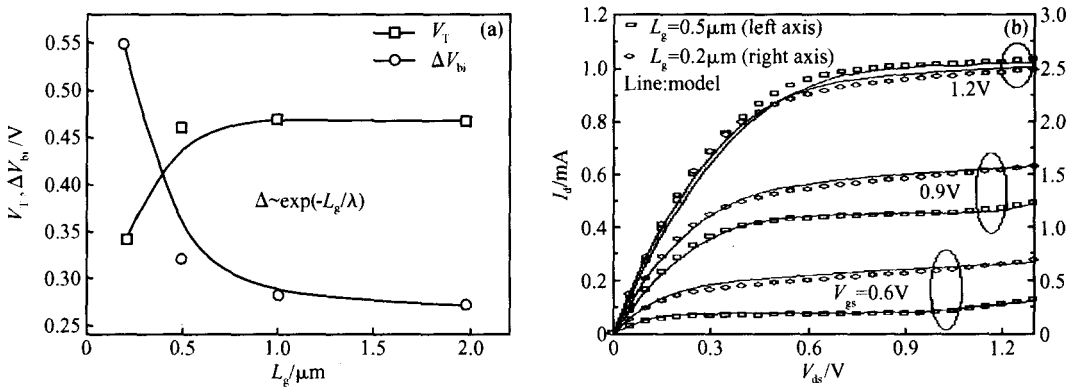

Fig. 12 Threshold voltage and ΔV_{bi} variation with the decrease of the channel length (a) and comparison between BSIMSOI and the measured data for different device channel lengths (b)

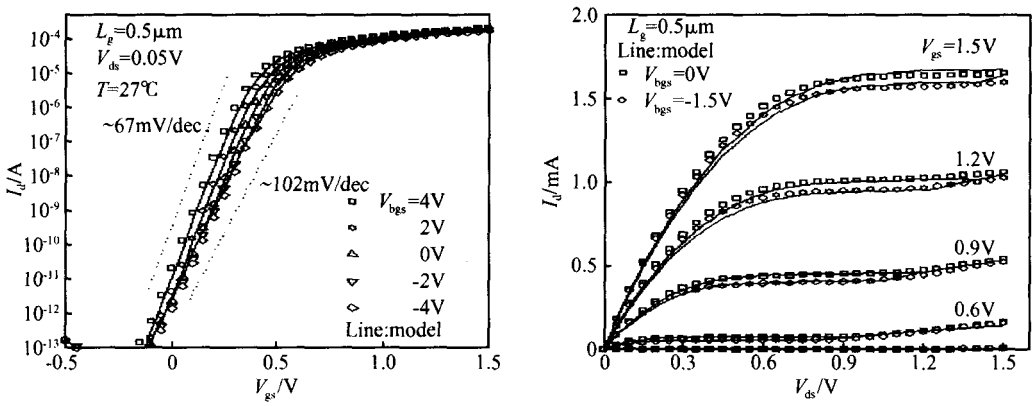

Fig. 13 Model verification of the PD-SOI and FD-SOI transition in BSIMSOI

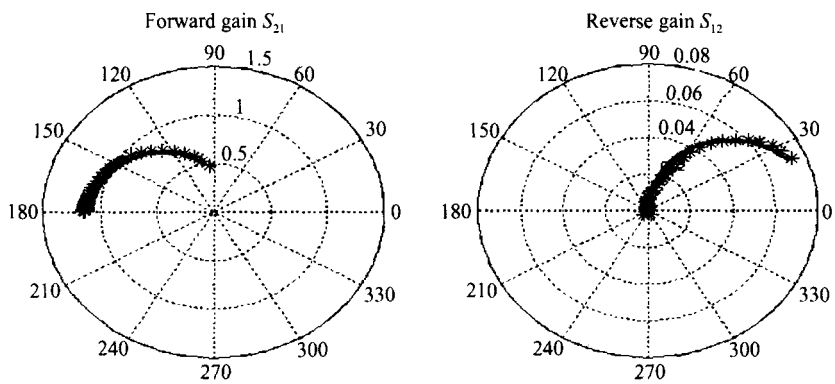

Fig. 14 Comparison of the S parameters between the measured and the BSIMSOI3.2 prediction for a short channel MOS transistor for the frequency range 100MHz ~ 20GHz

proved gate input resistance. A comparison of the S parameters between the measured and the BSIMSOI3.2 prediction is shown in Fig. 14, with frequency range of 100MHz ~ 20GHz, L = 0.2μm, W = 2 ×20μm, and $V_{gs} = V_{ds} = 1.5$V.

5 Conclusion

Based on past experience and present model research developments, about a dozen new physical effects have been modeled over the past several years for the bulk model, BSIM4, and the SOI model, BSIMSOI. The next generation BSIM model, BSIM5, has also been developed. Continuation of the BSIM tradition of handling new physical effects such as ballistic transport, velocity overshoot, and unified mobility, including Coulomb scattering for high k gate stack, and addressing new industry

needs in advanced process technologies and applications are the next research directions for BSIM. Models of comprehensive stress effect, strained silicon devices, gate-edge-drain-leakage (GEDL), and gate tunneling geometry dependence will also be further developed in the BSIM project.

References

[1] http://public.itrs.net

[2] Hutchby J A, Bourianoff G I, Zhirnov V V, et al. Extending the road beyond CMOS. IEEE Circuits and Devices Magazine, 2002, 18(2): 28

[3] http://www-device.eecs.berkeley.edu/~bsim3

[4] He J, Xi X, Chan M, et al. A non-charge-sheet based analytical model of undoped symmetric double-gate MOSFETs using SPP approach. IEEE International Symposium on Quality of Electronic Design, 2004: 45

[5] He J, Xi X, Chan M, et al. An advanced surface-potentialpl-us MOSFET model. Sixth International Conference on Modeling and Simulation of Microsystems, San Francisco, CA, 2003, 2: 262

[6] He J, Xi J, Chan M, et al. Charge-based core and the model architecture of BSIM5. Proc of the Sixth International Symposium on Quality of Electronic Design, 2005: 96

[7] He J, Xi J, Chan M, et al. BSIM5 user's manual. Electronic Research Laboratory, University of California, Berkeley, 2004

[8] Xi J, He J, Chan M, et al. BSIM4.3.0 manual. Electronic Research Laboratory, University of California, Berkeley, 2004

[9] Su P, Fung S K H, Wyatt P W, et al. On the body-source built-in potential lowering of SOI MOSFETs. IEEE Electron Device Lett, 2003, 24(2): 90

[10] Su P, Fung S K H, Wyatt P W, et al. A unified model for partial-depletion and full-depletion SOI circuit designs: using BSIMPD as a foundation. Proc of the IEEE Custom Integrated Circuits Conference, 2003: 241

BSIM 模型的研究和最近进展*

何 进[1,3,†] 陈文新[2,3] 奚雪梅[3] 宛 辉[3] 品 书[1] 阿里·力克纪达[1] 胡正明[3]

(1 北京大学微电子学研究院, 北京 100871)

(2 香港科技大学电子和电气工程系, 香港)

(3 美国 Berkeley 加州大学电气和计算机科学工程系, 加州 94720, 美国)

摘要: CMOS 集成电路技术的进一步发展和不断出现的新技术应用要求我们持续地改进和增强 VLSI 电路设计和模拟的集约模型. 基于此, 美国 Berkeley 加州大学的 BSIM 团队对国际工业标准芯片仿真物理模型 BSIM 进行了一系列的研究和发展工作. 本文分析和介绍了最近几年来本人参与其中的 BSIM 工程的研究和进展情况, 包括 BSIM5 的研究, BSIM4 的增强和 BSIMSOI 的发展. BSIM5 是为满足 RF 和高速 CMOS 电路模拟要求而发展的新一代物理基础的 BSIM 模型, 具有对称、连续和参数少的特点. BSIM4 是一个成熟的工业标准仿真模型, 在衬底电阻网络、隧穿电流、饱和电流原理和应力模型等方面有一系列的功能增强以支持技术进步的需求. BSIMSOI 已经发展成可应用于 SOI-PD 和 SOI-FD 技术的普适模型, 通过有效体电势 ΔV_{bi} 的改变进行器件工作模式的选择, 可以帮助电路设计者实现 PD 和 FD 共存的设计趋势.

关键词: 集约模型; BSIM5; BSIM4; BSIMSOI; 器件物理; MOSFET

EEACC: 2560R; 2560F

中图分类号: TN386 **文献标识码**: A **文章编号**: 0253-4177(2006)03-0388-09

* SRC 基金(批准号:2002-NJ-1001, 2003-NJ-1134)及香港 RGC 基金(批准号:HKUST6111/03E)资助项目

† 通信作者. Email: jinhe@ime.pku.edu.cn

2005-11-20 收到