A Novel High Output Resistance Current Source Based on Negative Resistance

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Abstract: This paper presents a novel scheme for enhancing resistance that utilizes an equivalent negative resistance. Adopting this novel scheme in the proposed current source could remarkably boost its output resistance without requiring increased power supply. Simulation with 0.6μm CMOS process models shows that the output resistance of the novel current source can reach the order of $10^9\Omega$ with a 1.04GHz bandwidth and only 10.6ppm/℃ in the range of -40～145 ℃.

Key words: current source; negative resistance; paralleled resistance
EEACC: 2570; 2570D
CLC number: TN431 **Document code:** A **Article ID:** 0253-4177(2006)03-0443-05

1 Introduction

Current source is one of the most important building blocks in modern analog and mixed-signal integrated circuits and is widely used for biasing, providing active loads in amplifiers or a current reference in current-mode processing. A high-performance current source requires a high output resistance in many applications. The traditional method for increasing the resistance of a circuit is to add a series resistance to the original resistance. Supposing the original resistance is r_o, an increased resistance $r_t = r_o + r_1$ for the circuit can be obtained by adding a series resistance r_1. However, this configuration requires an increase in supply voltage if the output current is to remain constant. Zeki and Kuntman proposed an IAFCCM structure to enhance the output impendence for a CMOS current mirror[1]. But IAFCCM is a 3-stage-cascode structure and requires a high power supply. Low power supply is a direction of development of integrated circuits. Ramirez-Angulo *et al*. summarized the structures of current sources with high output resistance under low supply voltage reported recently and proposed a new configuration[2]. However, proper compensations are necessary both in Refs. [2] and [3]. Quarantelli *et al*.[4] proposed a good method to increase the output resistance of the current source with an op amp, which requires neither a high power supply nor complex compensation. The output impendence of this current source is $r_{out} = r_{o1}(A+1)$. However, a simpler way, which utilizes an equivalent negative resistance circuit, could be adopted to obtain a high-output-resistance current source without increasing power supply. This paper presents this idea for enhancing resistance. A novel scheme for a current source adopting this idea for increasing its output resistance is also proposed in this paper. Simulation results show the other characteristics of the proposed current source are very good.

2 Principle of the proposed current source

2.1 Principle of the scheme

Figure 1 (a) shows the frame of the novel scheme, where r_o is the equivalent resistance of a normal current source, and r_2 is the compensative resistance. The total resistance of this circuit is

$$r_t' = \frac{r_o r_2}{r_o + r_2} \tag{1}$$

Usually, $r_t' < r_o$. However, if the parallel resistance r_2 is a negative resistance whose absolute value is slightly larger than r_o, then r_t' will be quite larger than r_o. This is the original idea of the pro-

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Received 10 September 2005, revised manuscript received 1 December 2005

posed novel current source with a high output resistance.

The relationship between r_t' and r_2 can be described by Fig. 1(b). Supposing r_2 is a variable resistance, then not only a small positive resistance but also different resistances can be obtained when two resistances are in parallel as shown in Fig. 1 (b). The value of r_t' depends on r_2. When r_2 is positive, we get a positive resistance less than r_o, whereas a negative resistance is obtained when r_2 is between $-r_o$ and zero. More interestingly, a positive resistance larger than r_o can be produced when r_2 is less than $-r_o$. If the absolute value of r_2 is equal to r_o, r_t' becomes infinite theoretically, which includes positive infinite resistance and negative infinite resistance even if r_o is a very small positive resistance.

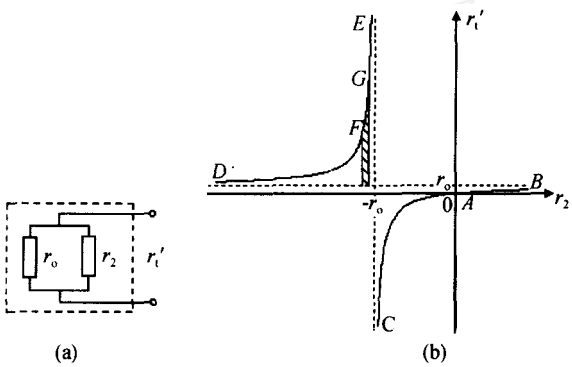

Fig. 1 (a) Parallel resistance; (b) Total resistance versus variable parallel resistance

The proposed current source adopts the above conclusion about two parallel resistances, and a suitable negative resistance is chosen to obtain a satisfactory output resistance of the current source, such as in the range of *F* to *G*. Yan *et al*. also utilized this range to enhance the voltage gain of a low voltage CMOS op amp[5]. If it is necessary and possible, other ranges in Fig. 1(b) can be used in other systems. However, it should be clear that a negative resistance is a resistance whose current decreases with increasing voltage, and a negative resistance can be obtained from a special device or an equivalent circuit.

2.2 Proposed current source with a high output resistance

Figure 2 shows the structure of the novel high-output-resistance current source. There are two parts in the circuit; the left part is a normal current source, such as a cascode current mirror, and the right part is an equivalent circuit that produces the negative resistance.

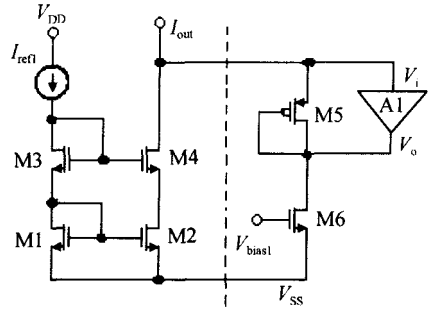

Fig. 2 Structure of the novel current source

A1 in Fig. 2 is a three-stage amplifier depicted in Fig. 3. The total voltage gain of the circuit producing the negative resistance is

$$A_V \approx \left(-\frac{g_{M7}}{g_{M10}}\right)\left(-\frac{g_{M8}}{g_{M11}}\right)\left(\frac{g_{M9}}{g_{M9}+g_{Mb9}}\right) = \frac{g_{M7}\,g_{M8}\,g_{M9}}{g_{M10}\,g_{M11}\,(g_{M9}+g_{Mb9})} \tag{2}$$

where g_{Mi} is the transconductance of Mi, and g_{Mb9} is the back-gate transconductance of M9.

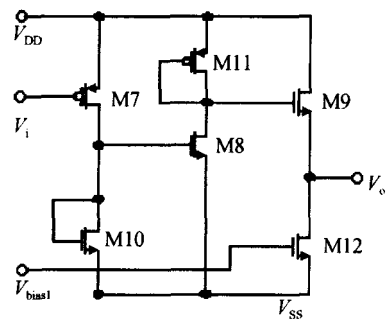

Fig. 3 Structure of A1

Suppose the positive equivalent resistance of the cascode mirror is R_{cm} and the small signal resistance of M5 is R_{ds5}. M6 provides a bias for M5. The equivalent resistance looking from the joint at the source of M5 and the gate of M7 is

$$R_{eq} \approx \frac{R_{ds5}}{1 - A_V} \tag{3}$$

Then the total output resistance of the novel current source is

$$R_{out} = \frac{R_{cm}\,R_{ds5}}{(1 - A_V)\,R_{cm} + R_{ds5}} \tag{4}$$

where $R_{cm} \approx g_{M4}\,R_{ds4}\,R_{ds2}$. In Fig. 2, R_{dsi} is the resistance between the drain and source of Mi. we adjust the parameters of the circuit and make $|(1 - A_V)\,R_{cm}|$ slightly larger than $|R_{ds5}|$ so that a very large output resistance and a more stable output current

can be obtained.

The normal current source is not limited as a cascode current mirror. A Widlar current source and a Wilson current mirror are also adopted in this novel current source. The simulation results of the different left parts are very similar. A typical current source with a negative resistance is shown in Fig. 4, where M13～M18 form an I_{bias} circuit. The key to obtaining a high output resistance is to design a proper W/L ratio for M7, M8, and M9 to make $|(1 - A_V) R_{cm}|$ very close to $|R_{ds5}|$.

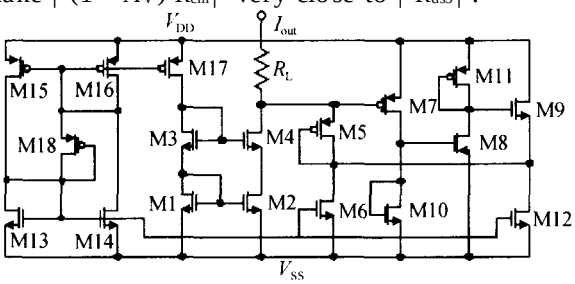

Fig. 4　A typical current source with negative resistance

3　Simulation and discussion

The circuit shown in Fig. 4 was simulated with a 0.6μm CMOS process model, where the power source was set at 3V and I_{out} was 52μA. The W/L ratios of the key transistors in the circuit are listed in Table 1. According to the simulation results, the output resistance of the cascode current mirror is R_{cm} = 30.1552MΩ, the equivalent resistance of the circuit that produces the negative resistance is R_{eq} = - 30.7058MΩ, and the total output resistance of the novel current source is R_{out} = 1.6817GΩ, which is higher than the MΩ range in Ref. [4] and 200MΩ in Ref. [2]. Actually, I_{out} does not approach a limit of 52μA but varies from several μA to several hundred mA. The power source also can be lowered to ensure M4～M9 in a saturation state.

Table 1　W/L ratios of the key transistors in Fig. 4

Device number	Type	W/L ratios (μm/μm)	Status
M4	nMOS	50/2	Saturation
M5	pMOS	50/1	Saturation
M7	pMOS	50/1	Saturation
M8	nMOS	25/1	Saturation
M9	nMOS	40/1	Saturation

Figure 5 displays the output current versus the output voltage. Curve 1 is the reference current I_{ref}, whose value is assumed to be 52μA. Curve 2 is the output current of the novel high resistance current source. Curve 3 is the output current of the cascode current mirror. Curves 2 and 3 are similar in shape. Magnifying the curves near I_{ref}, it can be clearly observed that the V_{omin} of the proposed current source is smaller and the stability is better. Without negative resistance compensation, $V_{omin} \approx$ 2.100V, whereas $V_{omin} \approx$ 1.465V with the compensative circuit.

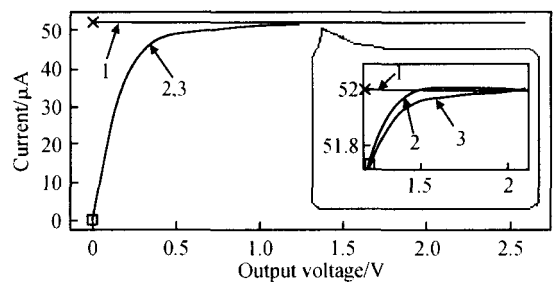

Fig. 5　Output current versus output voltage

Figure 6 is the frequency response of the proposed current source, and Figure 7 shows the temperature characteristics of the output current of the novel current source. From Fig. 6, it can be gathered that the - 3dB frequency is 1.04GHz, implying that the cut-off frequency of the novel current source is large. The bandwidths both in Refs. [2] and [4] are 100MHz. From Fig. 7, it can be seen that the temperature coefficient of the output current is 10.6ppm/ ℃ in the range of - 40～145 ℃, indicating that the temperature characteristic of the proposed current source is very good.

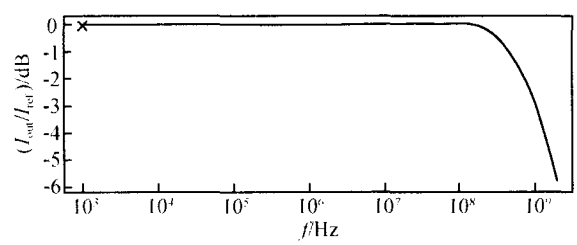

Fig. 6　Frequency response of the proposed current source

Figure 8 is the PSRR curve of the output current of the novel current source shown in Fig. 4. It can be seen that the PSRR value of this current is only about - 82. The relationship between the output current and the load resistance is depicted in Fig. 9. The output current of the novel current

source remains constant with the increase of the load resistance.

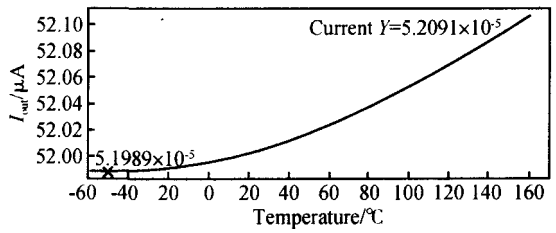

Fig. 7 Temperature characteristic of the output current

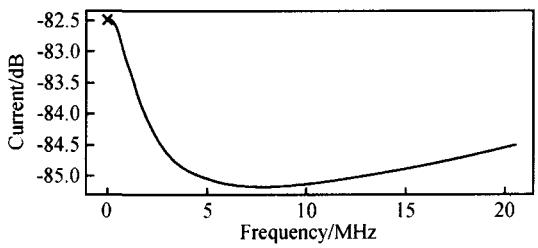

Fig. 8 PSRR of the output current

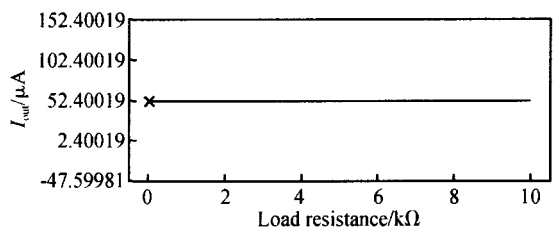

Fig. 9 Output current versus load resistance

4 Conclusion

A novel current source with a high output resistance is proposed in this paper. This current source adopts a parallel negative resistance to enhance the total resistance of the circuit, reaching the order of $10^9\Omega$. Its - 3dB frequency of 1.04GHz is larger than that in Refs. [2] and [4]. The temperature coefficient of the output current is only 10.6ppm/ ℃in the range of - 40～145 ℃. Moreover, the V_{omin} of the proposed current source is smaller than that of the pure cascode current mirror. The PSRR of the proposed current source is less than - 82.5dB. The simulation results indicate that the proposed scheme is good.

Furthermore, the novel concept of two parallel resistances has expansive applications. If one of the parallel resistances is a certain positive resistance and the other parallel resistance is a variable resistance changing from negative to positive, we can obtain different kinds of the total resistance and apply them in many fields. Therefore, this idea is significant.

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一种基于负电阻的高输出阻抗的电流源

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摘要: 给出一种利用等效负电阻实现阻抗增加的方法. 利用该方法,文中所提出的电流源可在不增加电源电压的前提下显著提高其输出阻抗. 基于 0.6μm 的 CMOS 工艺模型,仿真所得电流源的输出阻抗可达 $10^9\Omega$,同时,该电流源频带宽度为 1.04GHz,在 - 40～145 ℃之间,电流源的温度系数只有 10.6ppm/ ℃.

关键词: 电流源; 负电阻; 并联电阻

EEACC: 2570; 2570D

中图分类号: TN431　　**文献标识码**: A　　**文章编号**: 0253-4177(2006)03-0443-05

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2005-09-10 **收到**, 2005-12-01 **定稿**