A Novel Method to Compensate the Sigma-Delta Shaped Noise for Wide Band Fractional-N Frequency Synthesizers *

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Abstract: A novel method to partially compensate sigma-delta shaped noise is proposed. By injecting the compensation current into the passive loop filter during the delay time of the phase frequency detector (PFD), a maximum reduction of the phase noise by about 16dB can be achieved. Compared to other compensation methods, the technique proposed here is relatively simple and easy to implement. Key building blocks for realizing the noise cancellation, including the delay variable PFD and compensation current source, are specially designed. Both the behavior level and circuit level simulation results are presented.

Key words: charge pump; frequency synthesizer; noise compensation; phase frequency detector; phase noise; sigma-delta modulator

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1 Introduction

Sigma-delta fractional-N frequency synthesizers have become very popular for RF transceiver implementation because of their high frequency resolution, fast settling time, and low spurious performance. By applying sigma-delta modulation to the frequency division number, quantization noise that emerges from the fractional divisions is whitened and noise-shaped. The sigma-delta quantization noise is then pushed to a high frequency region and filtered by a low pass loop filter. As a result, the loop bandwidth can be greatly increased, and a fast settling time can be achieved[1~3].

In recent research, in-loop modulation with a 1Mb/s data rate has been required for transmission that demands a very wide bandwidth for sigma delta fractional-N frequency synthesizers[4]. In some other applications such as personal handyphone systems (PHS), seamless switching between different channels is a challenge for the designers, since they require a settling time of 15μs[5]. For these cases, the bandwidth of the frequency synthesizer is required to be as large as several hundred kHz. For state-of-the-art sigma-delta frequency synthesizers, such a large bandwidth is difficult to realize without sacrificing phase noise performance.

In this paper, a new method to partially compensate the sigma-delta shaped noise is proposed. The key point is that the compensation is implemented during the delay time of the PFD. With this technique, the dominant out-band noise is reduced and the total phase noise performance is improved while keeping the bandwidth large enough to meet the requirement of in-loop modulation or fast channel switching.

2 Time domain analysis of sigma-delta shaped noise

Figure 1 shows the phase noise performance of a sigma-delta fractional-N frequency synthesizer by behavior simulation. The noise contributions mainly include VCO noise, charge pump noise, and sigma-delta shaped noise. In Fig. 1, the bandwidth is designed to be 300kHz, which is enough to realize a settling time of less than 15μs. Under such conditions, it can be seen from the figure that the out-band noise becomes very high, and the sigma-delta shaped noise is the dominant source. Therefore, the discrepancy between large bandwidth and low phase noise becomes significant.

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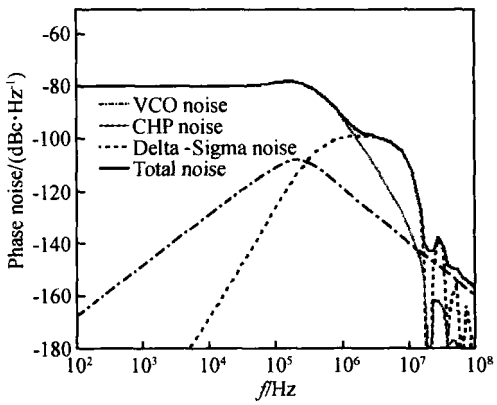


Fig. 1　Behavior simulation results of the phase noise for a sigma-delta fractional-N frequency synthesizer with a bandwidth of 300kHz

Figure 2 illustrates the structure of a sigma-delta fractional-N frequency synthesizer. At the m-th reference cycle, the instantaneous frequency divider modulus $N[m]$ is randomly altered by the sigma-delta modulator, equivalently realizing the fractional division[2]. When reaching the locking state, the VCO output frequency is

$$f_{vco} = N_{av} f_{ref}$$

where N_{av} is the fractional division ratio, and f_{ref} is the reference frequency, which exactly equals the divider output frequency f_{div} in the ideal case.

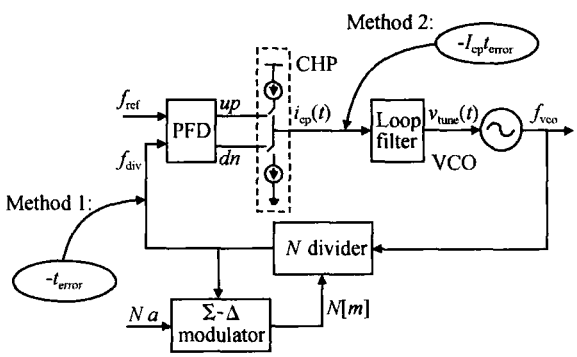


Fig. 2　Structure of the sigma-delta fractional-N frequency synthesizer

The time domain divider output signal f_{div} is shown in Fig. 3, in which both the desired output rising edges and the actual ones are illustrated. The desired output period is

$$T_{div} = N_{av} T_{vco}$$

where $T_{div} = 1/f_{div}$, and $T_{vco} = 1/f_{vco}$. The actual output period T'_{div} is

$$T'_{div} = N[m] T_{vco}$$

Therefore, there exists a time error in each reference cycle, and the frequency synthesizer never actually reaches the locking state. From Fig. 3, the accumulated time error at the n-th cycle can be calculated to be

$$t_{error}[n] = T_{vco} \sum_{m=n_0}^{n-1} (N_{av} - N[m])$$

where $n = 1, 2, 3, 4, \cdots$.

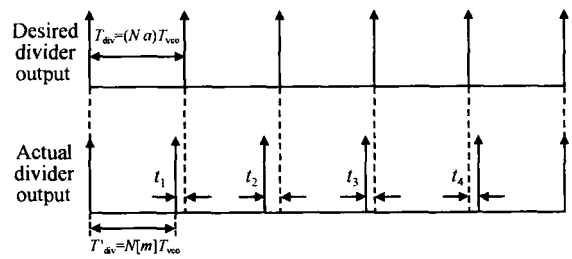


Fig. 3　Ideal and actual frequency divider output signal in the time domain

The above equation can be rewritten as

$$t_{error}[n] = \frac{T_{ref}}{N_{av}} \times \sum_{m=n_0}^{n-1} (N_{av} - N[m])$$

where T_{vco} is substituted by T_{ref}/N_{av} and $T_{ref} = 1/f_{ref}$.

As the sigma-delta modulator alters the divider modulus randomly, t_{error} is consequently modulated. Then t_{error} is transferred to the PFD/charge pump output and generates a noisy electric charge $I_{cp}\, t_{error}$ in the loop filter (I_{cp} is the magnitude of the charge pump current), which then becomes the sigma-delta shaped noise at the VCO output (see the sigma-delta noise in Fig. 1).

If the sigma-delta induced noise, i. e. the time error t_{error} or electric charge $I_{cp}\, t_{error}$, can be partially cancelled, the total noise will be reduced. Therefore, two ideas to compensate this noise were proposed-delay compensation and charge pump current compensation[7]. As shown in Fig. 2, if a time delay $-t_{error}$ is introduced at the divider output, then the time error caused by the sigma-delta modulator can be eliminated. This method was implemented in Ref. [8], but the authors did not achieve the desired results due to the difficulty of realizing a precise delay time and complex extra hardware. Another method is to inject an electric charge $-I_{cp}\, t_{error}$ into the loop filter to compensate this noise. This method was realized in Ref. [4], and it achieved an obvious reduction in noise. However, a large amount of extra hardware is needed, greatly increasing the power consumption and circuit com-

plexity. Another issue in Ref. [4] is that the value of the time span of several VCO cycles used for noise cancellation is not appropriate. The details of this issue will be discussed along with the discussion of our proposed method. Further analysis of the sigma noise cancellation can be found in Ref. [9].

3 Proposed charge pump current compensation technique

In this section, we propose a relatively simple charge pump current compensation scheme. In Fig. 4, both the charge pump response $i_{cp}(t)$ to the time error t_{error} and the compensation current $i_c(t)$ are shown. To compensate the sigma delta noise, the compensation charge injected into the loop filter is

$$Q = I_c t_c = I_{cp} t_{error}$$

where I_c is the compensation current magnitude, and t_c is the compensation time span. For an effective noise cancellation, there are key trade-offs between I_c, t_c and the start point of t_c.

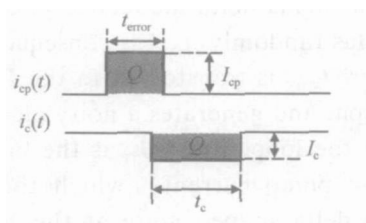


Fig. 4 Illustration of charge pump current compensation to the sigma-delta induced noise

Figure 5(a) illustrates the ideal case of compensation where the compensation current is exactly the opposite of the noise current in both magnitude and phase. The problem in this case is that t_c is very small (usually less than 1ns). It is very difficult to generate accurately such a narrow pulse with a phase precisely opposite to t_{error}. It is also very difficult to turn on the compensation current fully during such a short time. Figure 5(b) illustrates another case where the compensation current is injected during the whole reference period. Since the reference period T_{ref} is much longer than t_{error}, the corresponding compensation current magnitude I_c becomes very small (about several μA) which is difficult to realize with proper precision using even a state-of-the-art IC process.

Our proposed method is to inject the compensation current during the delay time of the PFD, t_{delay}. For the tri-state PFD, there is a delay pulse during which both the charge pump sink and source current are on to eliminate the dead zone problem[1]. The proposed compensation method is shown in Fig. 6. In Fig. 6(a), the f_{ref} signal leads to the f_{div} signal, and the control signal dn represents the delay pulse. During this time span, the compensation current I_c is injected, and the compensation is realized, as can be seen from the I_{total} wave in the figure. If the f_{div} signal leads to the f_{ref} signal, a similar idea can be applied as shown in Fig. 6(b) in which the up control signal represents the delay pulse.

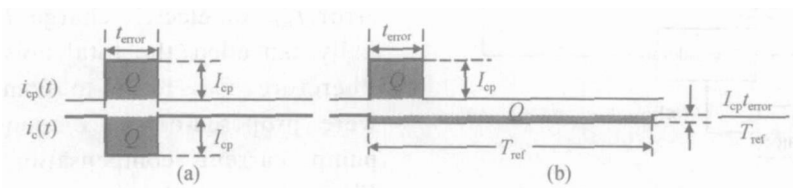


Fig. 5 (a) Compensation current exactly cancels the noisy electric charge; (b) Compensation current injected during the whole reference period

A top-level functional block diagram of the proposed synthesizer is shown in Fig. 7. It differs from Fig. 2 in that the compensation circuit is added. The compensation circuit includes the compensation current source and the digital control circuit. According to the analysis in Sec. 2, the compensation current can be calculated by

$$I_c = \frac{I_{cp}}{t_{delay}} \times t_{error}[n] = \frac{I_{cp}}{t_{delay}} \times \frac{T_{ref}}{N_{av}} \times \sum_{m=n_0}^{n-1} (N_{av} - N[m])$$

As shown in Fig. 7, the digital control circuit takes the average divider modulus N_{av} and the instantaneous divider modulus $N[m]$ as input and is syn-

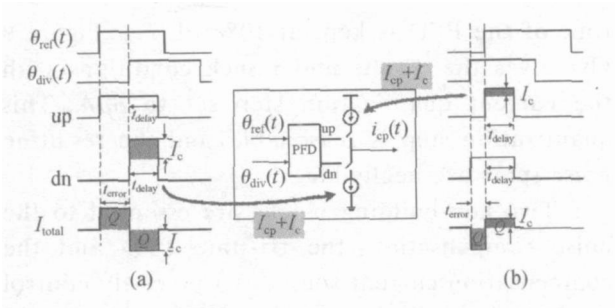


Fig. 6　Proposed compensation scheme　(a) f_{ref} leads to f_{div}; (b) f_{div} leads to f_{ref}

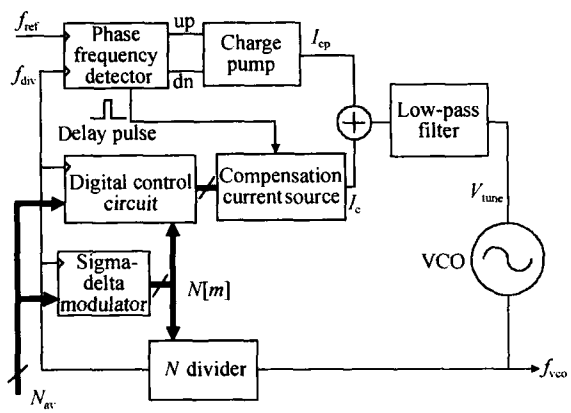


Fig. 7　Functional block diagram of the proposed synthesizer

chronized by the f_{div} signal. The compensation current source is programmed by the digital control circuit output and is switched on and off by the delay pulse signal from the PFD with a pulse width of t_{delay}. The compensation current is then injected into the loop filter to cancel the sigma-delta shaped noise.

This method has two advantages. First, the control pulse of the compensation current naturally exists in the PFD circuit. Therefore, the cost of the extra hardware to generate such a control signal is low. In Ref. [4], the compensation time span is generated by several VCO cycles. This time span is very short, and the related circuits work in a much higher frequency than f_{ref}. This necessitates larger extra hardware and power consumption. Second, the PFD delay time is usually on the order of several ns which is more appropriate. For example, in our simulation to be presented shortly, the typical delay time is designed to be 5ns for a reference frequency of 20MHz. This leads to a compensation current in the range of 0～60μA, which is easily realized with proper precision. Also, the PFD delay time is long enough to turn on both the charge pump current and the compensation current fully. However, in Ref. [4] the compensation time span, which is several VCO cycles, is too short for the compensation current to be fully turned on. At the same time, the VCO cycle will vary due to channel switching, causing the compensation effect to deviate from the desired case.

One issue for the proposed method is that the charge pump noise, which is the dominant in-band frequency synthesizer noise, is related to the delay time of the PFD. The longer the PFD delay time, the more charge pump noise is injected into the passive loop filter. However, this problem can be alleviated by optimizing the synthesizer system parameters.

4　Compensation simulation and key circuit design

To realize the proposed compensation scheme, a behavior level simulation using CppSim is implemented. The frequency synthesizer system parameters are designed and listed in Table 1. Figure 8 shows the simulation results of the noise performance before and after compensation. In the simulation, the delay time of the PFD is chosen to be 10% of the reference period, and a maximum noise reduction of 16dB is achieved.

Table 1　Parameters for the sigma-delta fractional-N frequency synthesizer

f_{ref}	20MHz
Band width	300kHz
I_{cp}	400μA
ΣΔM	3rd MASH
Loop filter	3rd Passive
Divide number	122.3113752
f_{vco}	2.4GHz
K_{vco}	100MHz/V
PFD delay	Variable

In real circuit level realization, the compensation current needs to be quantized. Quantization of the compensation current introduces noise spurs, as shown in Fig. 9(a). In Fig. 9(a), the compensation current is within the range of 0～60μA. With the incrementation of the quantization precision, the noise spurs become small. However, in real circuit design, the higher the quantization precision, the more difficult it is to realize such a current source. Therefore, there is a trade-off between the

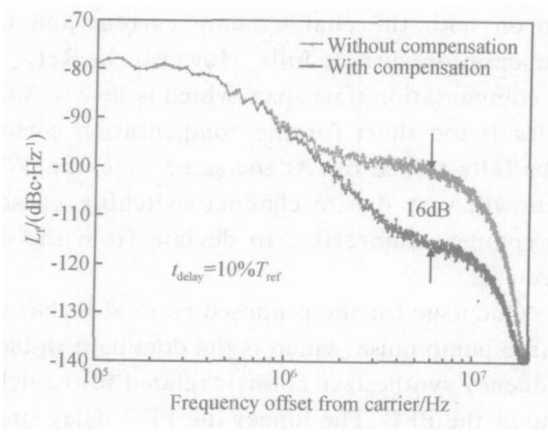
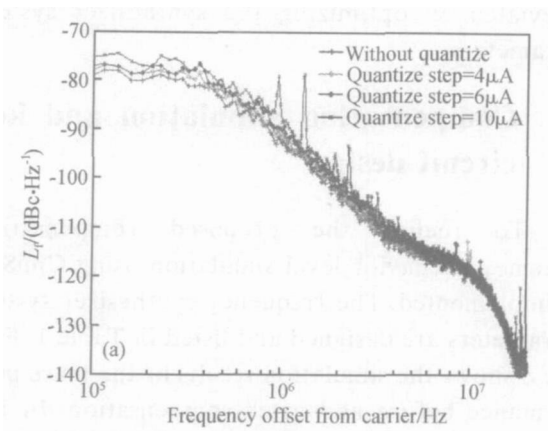


Fig. 8 Behavior simulation results of the noise compensation using CppSim



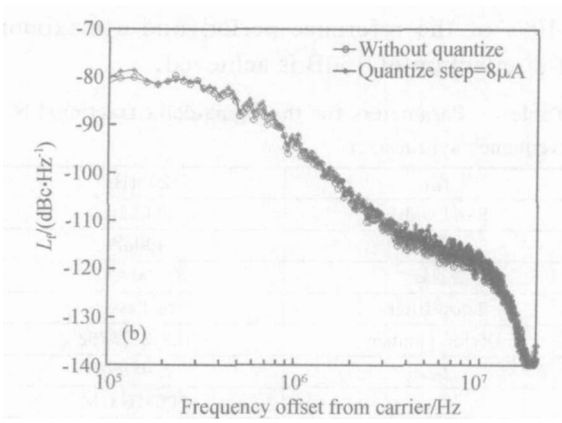
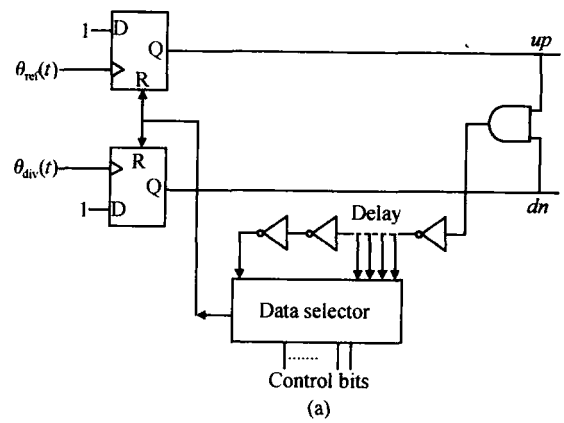


Fig. 9 (a) Spurs arise due to compensation current quantization; (b) Spurs becomes negligible when I_{cp} is increased to 1.2mA with a 8μA quantization step

quantization precision and the quality of the compensation current. Since the compensation current I_c is proportional to I_{cp}, the charge pump current I_{cp} is adjusted to 1.2mA in our design, and consequently the compensation current falls into the range of 0～180μA when the delay time of the PFD is kept at 10% of T_{ref}. Figure 9(b) gives the results under such conditions with the current quantization step set to 8μA. This quantization step is reasonable, and the resulting noise spurs are negligible.

Two key building blocks are essential to the noise compensation: the tri-state PFD and the compensation current source. To precisely control the PFD delay time, a delay programmable PFD is proposed as shown in Fig. 10(a). The delay time can be determined by the data selector when the temperature and process fluctuate. Figure 10(b) gives the simulation results of the delay time which can be programmed in the range of ±20% of the required value (5ns) with a step size of about 0.1ns.



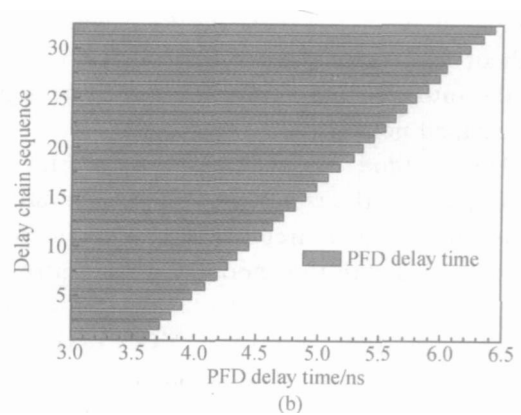


Fig. 10 (a) Delay programmable PFD; (b) Simulation results of the PFD delay time

Figure 11(a) shows the designed compensation current source. In our test chip, it is designed to be a binary-weighted programmable current source with a minimum step size of 16μA. This structure features a very high output impedance and voltage headroom. Figure 11(b) shows the

simulation results of the output current. Note that in the figure the output voltage V_{out} is normalized to the supply voltage. It can be seen that the compensation current source has a very high output impedance and good matching. The output voltage headroom occupies about 80 % of the supply voltage, which supplies a wide enough voltage tuning range for the VCO.

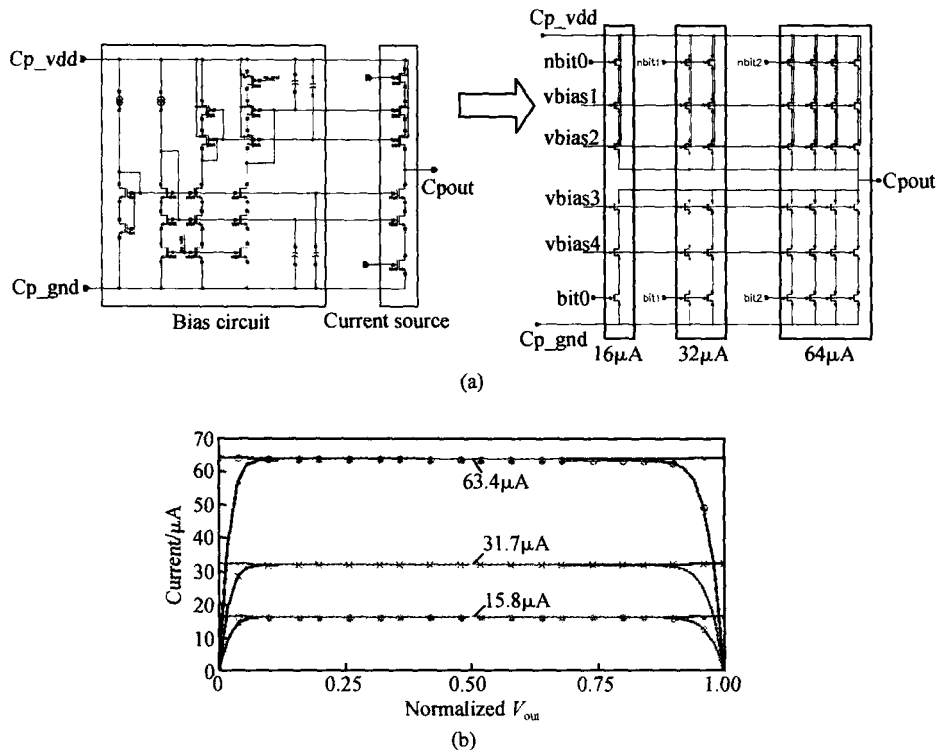


Fig. 11　(a) Binary-weight compensation current source; (b) Simulation results of the compensation current

5 Conclusion

We have proposed a novel method to compensate the sigma-delta shaped noise for wide band fractional-N frequency synthesizers. By injecting the compensation current into the passive loop filter during the delay time of the PFD, a maximum reduction of the phase noise by about 16dB can be achieved. As the PFD delay time naturally exists in the circuit, little extra hardware cost is required. Furthermore, the PFD delay time is appropriate for both the realization of the compensation current precision and its turn-on performance. Therefore, the proposed method is relatively simple and reasonable to implement compared to other compensation schemes. Based on the simulation of the proposed method, possible realizations of the key building blocks are designed, including delay variable PFD and compensation current source, which give appropriate performances.

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一种补偿宽频带小数 N 频率合成器中 Sigma-Delta 整形噪声的新方法 *

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摘要: 提出了一种部分补偿 Sigma Delta 调制器整形噪声的新方案. 通过在鉴频鉴相器中的延迟时段向无源滤波器中注入补偿电流 ,最大可实现 16dB 的噪声补偿. 与其他补偿方案相比 ,文中提出的方案相对简单和易于实现. 特别设计了可变延迟的鉴频鉴相器和补偿电流源 ,并给出了行为级和电路级的仿真结果.

关键词: 电荷泵; 频率合成器; 噪声补偿; 鉴频鉴相器; 相位噪声; sigma delta 调制器
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