A DC-Offset Cancellation Scheme in a Direct-Conversion Receiver for IEEE 802.11a WLAN*

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Abstract: A DC-offset cancellation scheme in a 5GHz direct-conversion receiver compliant with the IEEE 802.11a wireless LAN standard is presented. An analog feedback loop is used to eliminate the DC-offset at the output of the double-balanced mixer. The test results show that the mixer with the DC-offset cancellation circuit has a voltage conversion gain of 9.5dB at 5.15GHz, a noise figure of 13.5dB, an IIP3 of 7.6dBm, a DC-offset voltage of 1.73mV eliminating 76% of DC-offset, and a power consumption of 67mW with a 3.3V supply. The direct conversion WLAN receiver has been implemented in 0.35μm SiGe BiCMOS technology.

Key words: DC-offset; WLAN; BiCMOS
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1 Introduction

Wireless communications will evolve towards high data rate applications in the future, a primary one of which is WLAN (IEEE 802.11a. b. g). In order to get more features and low cost at RF front sections, the choice of a suitable receiver implementation requires a careful study of the system specifications. The superheterodyne architecture is a traditional receiver patented in 1917 by Edwin Armstrong[1], which offers the best performance in most wireless system applications. However, the architecture requires passive filter components mostly because of the intermediate-frequency (IF) and image-reject, which must have high quality factors and often employ an off-chip surface acoustic wave (SAW) filter[2].

Direct-conversion receivers, such as that shown in Fig. 1, have attracted much attention over the past few years. In actual direct conversion systems, the local oscillator (LO) frequency is in the middle of the RF spectrum under consideration. However, this architecture creates additional performance criteria such as DC-offsets, second order intermodulations (IM2), in-band local oscillator radiation, and flicker noise that are not present in a heterodyne counterpart. One of the greatest challenges of these performance criteria is the effective cancellation of the DC-offset[3]. The DC-offset of a receiver can be separated into two components: a constant offset and a time-varying offset. The constant DC-offset is attributed to the mismatch between the mixer components, and the time-varying DC-offset is generated by the self-mixing of the LO[4]. The former can be minimized with the help of specific layout techniques, but the latter can never be completely eliminated.

There are two common DC-offset cancellation solutions: AC coupling (high pass filter)[6] and digital cancellation with DAC sampling[7]. By the former means, a very low corner frequency of the high pass filter is required, indicating large capacitors, which is not suitable for integration. The digital solution involving DAC will complicate the design and increase the power dissipation.

We focus on eliminating the DC-offset at the mixer output with analog feedback loops as first mentioned by Laferriere *et al*.[5], whose design has a shortcoming and cannot be completely implemented. We also analyze the mechanism of the DC-offset of the mixer and the circuit topology.

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2 Circuit topology and analysis

2.1 Topology preview

A full direct-conversion receiver topology is illustrated in Fig. 1. In this solution, a DC-offset circuit occurs in the base band section following the mixer.

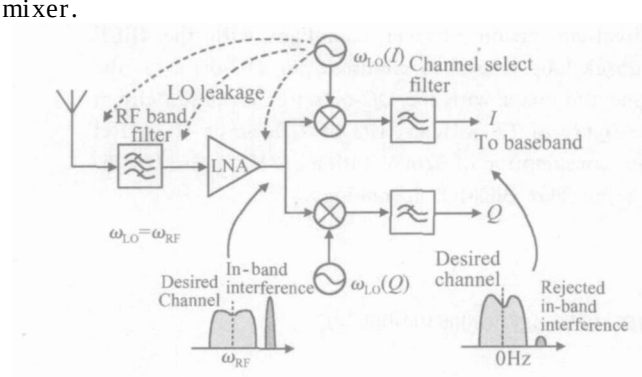

Fig. 1 Direct-conversion receiver

2.2 Mixer design

The circuit schematic of the mixer is shown in Fig. 2, which is a typical Gilbert cell with a single-ended input but a differential output. Inductor L_E is used for emitter degeneration to increase the linearity of the mixer while consuming little voltage headroom. As mentioned in Ref. [8], when the LO is an ideal square wave, the mixer's voltage gain is

$$A_V = \frac{2}{\pi} \times \frac{R_L}{| r_e + j\omega L_E |} \tag{1}$$

where R_L is the load resistance, and r_e is the emitter resistance of Q5 or Q6. Since the mixer's IIP3 is proportional to $\omega G_m L_E$, L_E should be carefully chosen to compromise between the gain and the IIP3. Noise matching is achieved by selecting the sizes of L_E and the transistors and operating the RF transistors at the current density required for minimum noise figure. Combined with the matching network, L_E also achieves simultaneous noise and power matching[8]. Since the current in the quad switching transistors is determined by the RF transistors below, the current density for peak f_T is achieved by sizing the transistors. In this design, they are 1/6 of the RF transistors. The LO signals are applied to the base of the quad transistors through buffers, so that their amplitude can be kept large enough for complete switching. L_f and C_f are tuned on the LO + RF frequency to get rid of the unwanted sideband. The LC tank tuned on the second RF harmonic acts as an AC current source in the emitter of the input transistor pair[7].

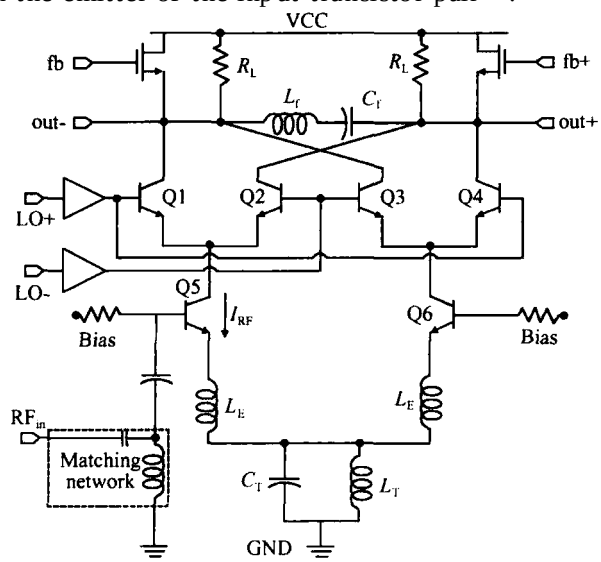

Fig. 2 Schematic of double balanced mixer

2.3 DC-offset analysis of mixer

The bipolar transistors Q5 and Q6 in Fig. 2 are simply modeled as a voltage-controlled current source (VCCS), and transistors Q1～Q4 are regarded as ideal switches. The dominant source of nonlinearity in Q5 and Q6 is assumed to be the input g_m-stage. The nonlinear VCCS is

$$i_{RF}(t) = g_m[v_{in}(t) + k_2 v_{in}^2(t) + k_3 v_{in}^3(t) + \cdots] \tag{2}$$

where k is the n-order nonlinear coefficient. Therefore, the output current of the mixer can be written as

$$i_{out}(t) = i_{RF}(t)\, g_{LO}(t) \tag{3}$$

where g_{LO} is the gate function of the LO signals as a Taylor series. The parts of interest are the fundmental and DC components of i_{out}. Equation (4) shows the DC component in the mixer output:

$$V_{DC} = \eta_{nom} R_L (I_T + g_m k_2 A_{RF}^2)(\Delta\eta + \Delta R) \tag{4}$$

Equation (4) is the ideal DC-offset behavioral model of a double-balanced mixer[9], where η_{nom} is the duty cycle (typically 50 %), $\Delta\eta$ is the mismatch in the duty cycle in the transistors of the LO input, I_T is the mixer static current which is half of the tail current, ΔR is the dominant mismatch in the practical process, and A_{RF} is the amplitude of the RF signal in the mixer input. According to Eq. (4),

the DC term in the IF depends on the collector resistor mismatch, the value of the tail current, and the amplitude modulation component.

2.4 DC-offset cancellation circuit

In parallel with the resistor loads R_L, a pair of pMOS are employed to shunt the output current of the mixer under the control of the feedback loop, as shown in Fig. 2. The feedback network consists of common mode (CM) and differential mode (DM) feedback loops. The output voltage is adjusted by the shunted current, which must have enough tolerance to severely restrict DC-offset voltage. This current is set at about 20 % of the total mixer's collector current in this design.

In the common-mode feedback loop, the common-mode output voltage is compared with a reference voltage. The comparison voltage controls the gate of the pMOS in order to stabilize the common-mode voltage at the mixer output. The common-mode DC-offset voltage is reduced in this way.

In the Gilbert-cell based mixer, a differential-mode DC-offset is predominant at the output. The DM feedback loop circuit is restricted not only by the base-band signal spectrum, but also the noise contributing to the whole receiver. Therefore, the DM DC-offset correction loop amplifier must fulfill three requirements:

(1) The loop must have sufficient gain at DC to provide adequate DC-offset reduction;

(2) The equivalent output noise of the circuit must be low enough to avoid significantly degrading the mixer noise figure;

(3) The loop must have a gain low enough near the lower corner frequency of the sub channel (at frequencies above 150kHz in this case) where the desired signal is not attenuated significantly.

Following these requirements, the differential-mode loop is a low-pass filter with a high gain and a low cutoff frequency. A schematic of the loop is shown in Fig. 3.

The first stage illustrated in Fig. 3 utilizes bipolar transistors in the feedback amplifier, which have higher gain and lower noise than MOSFETs. However, a pair of MOSFETs is placed in the second stage, which generates a Miller multiplication with high input impedance. The two stage loop amplifiers are loaded by pMOS current sources. The total impedance at the output is equal to $r_{01} /\!/ r_{02}$,

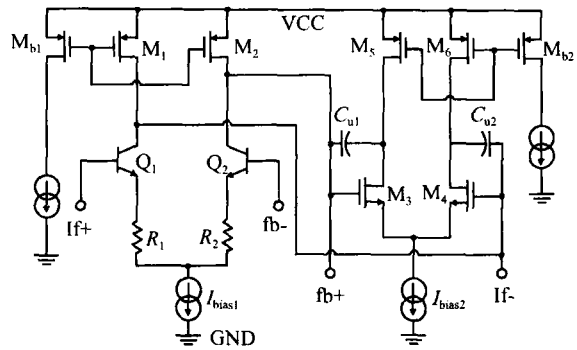

Fig. 3　DM feedback loop with Miller multiplier

and the gain is

$$\text{Gain} = - g_m (r_{01} /\!/ r_{02}) \tag{5}$$

The gain of first stage is 40.3dB at 0Hz, and the phase margin is 130°. With no Miller capacitor, the bandwidth of the amplifier is about 7MHz, and the second stage gain is 45dB. The second stage gain is similar to the first stage, allowing the Miller effect to generate an effective capacitance at the inter-stage of the amplifier. The Miller effective capacitance is mostly equal to the product of the compensation capacitance and the second stage gain.

$$C_{\text{Miller}} = \text{Gain}_{\text{sec}} C_{ui} \tag{6}$$

The configuration is a Miller integrator with 2pF capacitor that is small enough to be integrated on the chip, and the actual effective input capacitor is about 1nF. It is difficult to fabricate a capacitor of 1nF since the capacitors are area-consuming components. The curve in Fig. 5 shows the frequency response of the differential feedback-loop, which is close to the ideal model of former requirements. With the Miller capacitor, the feedback loop has a low enough gain at 150kHz, offering a corner frequency low enough for the 802.11a standard. In Fig. 3, R_1 and R_2 are a couple pair with emitter degeneration to adjust the gain.

3 Results

The circuit was implemented in 0.35μm SiGe BiCMOS technology. A die photograph is shown in Fig. 4, which has an area of 0.65mm ×0.53mm, and the DC-offset cancellation circuit has an addi-

tional area less than 0.1mm^2.

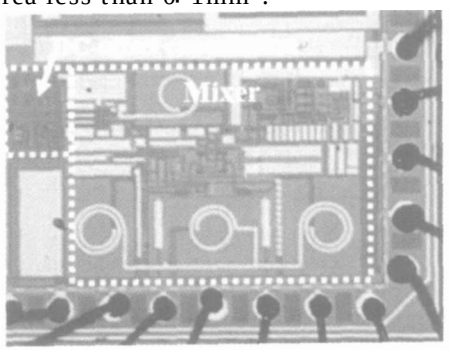

Fig. 4 Die photograph of the full receiver circuit

The measured frequency response of the DC-offset cancellation of the feedback loop is close to the simulation result, as illustrated in Fig. 5. The DC-offset voltage is 1.73mV at the IF output of the mixer, coupled by a pair of capacitors. The DC-offset reduction is 76%. That is less than simulation average value of 98% because of various non-ideal conditions such as mismatching and parasitic components.

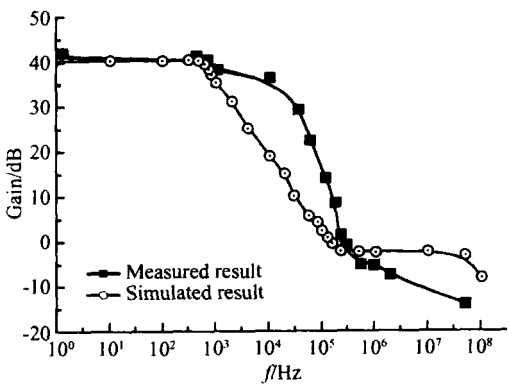

Fig. 5 Measured frequency response of the DM feedback-loop

Figure 6 shows the 1dB compression point with the same RF and LO frequency above and with a load of 50Ω. It shows that the 1dB compression point is -2dBm, which is slightly less than the simulated result (-1.5dBm). Figure 7 shows the conversion voltage gain versus the input signal frequency. The measured result, already computed with a large load resistance, is smaller than the simulated result, possibly due to the input matching and parasitic components of the circuit.

The DC-offset slightly affects the performance of the mixer illustrated in Table 1.

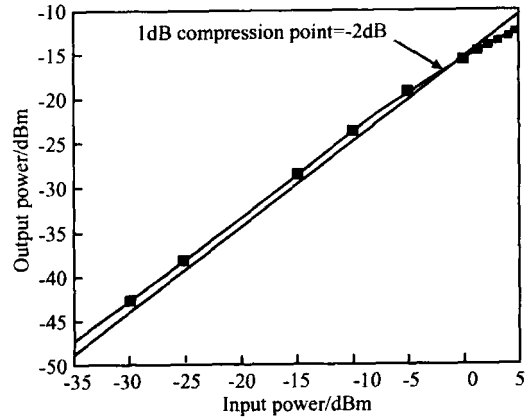

Fig. 6 Measured input 1dB compression point

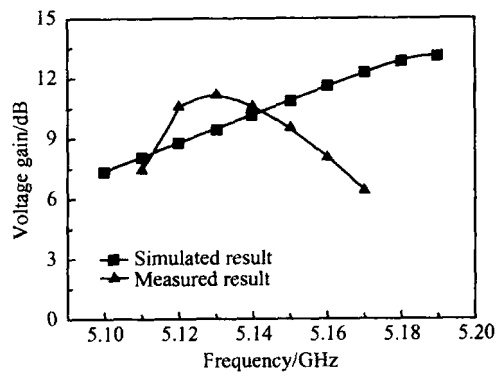

Fig. 7 Measured conversion voltage gain

Table 1 Summary of performance

Parameter	Circuit with DC-offset	Circuit without DC-offset
Noise figure/dB	13.5	12.1
IIP3/dBm	7.6	7.7
Conversion gain	9.5	12.7

4 Conclusion

A direct-conversion mixer with a DC-offset cancellation circuit is presented. It draws a 21.3mA current with a 3.3V supply and provides a conversion voltage gain of about 9.5dB, a noise figure of 13.5dB, and IIP3 of 7.6dBm. The DC-offset cancellation circuit has an additional area less than 0.1mm^2, an added power dissipation of 0.3mW, and it eliminates 76% of the DC-offset voltage. This circuit is easy to be realized and has little influence on the performance of the receiver.

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一种解决无线局域网直下变频接收机直流漂移的方法 *

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摘要: 提出了一种符合 IEEE802.11a 无线局域网的 5GHz 直下变频接收机解决直流漂移的方法. 该方法利用双平衡混频器输出端的模拟反馈环路消除直流漂移. 该混频器经过测试, 在 5.15GHz 频率下具有 9.5dB 的转换增益, 13.5dB 的噪声系数和 7.6dBm 的三阶交调, 在 3.3V 电源电压条件下 67mW 的功耗, 以及 1.73mV 的直流漂移, 并能使直流漂移减少 76%. 该方案及整个直下变频的 WLAN 接收机已经采用 0.35μm SiGe BiCMOS 工艺流片并测试.

关键词: 直流漂移; 无线局域网; BiCMOS

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