30 Gbit/s Parallel Optical Receiver Module *

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Abstract: A 30Gbit/s receptor module is developed with a CMOS integrated receiver chip (IC) and a GaAs-based 1×12 photo detector array of PIN-type. Parallel technology is adopted in this module to realize a high-speed receiver module with medium speed devices. A high-speed printed circuit board (PCB) is designed and produced. The IC chip and the PD array are packaged on the PCB by chip-on-board technology. Flip chip alignment is used for the PD array accurately assembled on the module so that a plug-type optical port is built. Test results show that the module can receive parallel signals at 30Gbit/s. The sensitivity of the module is -13.6dBm for 10^{-13} BER.

Key words: receiver module; parallel; PD array
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1 Introduction

Wave division multiplexing (WDM) and time division multiplexing (TDM) are two important technologies in modern optical communication systems. To support these multiplexing systems, high-speed devices and devices with accurate wavelengths and limited bands, such as LDs, modulators, PDs, and wave-divided guides and de-multiplexers must be developed and produced. The high cost of these devices is acceptable for long distance communication, but in short- or very-short-reach communication systems, WDM and TDM architectures are too expensive.

A parallel optical communication system adopts more than one fiber to transmit signals. Unlike WDM and TDM, it adopts low or medium speed transmitters and receivers. By simply repeating these physical conveyance channels, one can easily obtain a communication system with a transmitting ability that exceeds tens of Gbit/s[1,2]. In what are called VSR (very-short-reach) systems, the scheme of adopting more fiber channels is cost effective. It is worth using parallel optical communication to realize high-speed transmission. Because of the advantage in cost, of the five suggestions for VSR criteria approved by the Optical Internetworking Forum (OIF) from 2000 to 2003[3], three are parallel schemes. Some key devices such as transmitter modules and receiver modules for parallel optical communication systems have been developed and produced by some major equipment vendors[4,5].

In this paper, we present a parallel optical receiver module developed by our group. It has 12 receiver channels working at a wavelength of 850nm. Each channel can work at 2.5Gbit/s. The net data reception speed over 12 channels can achieve 30Gbit/s. The receiver module was fabricated with an integrated chip (IC) and PIN detector array. These two devices were integrated and packaged by chip-on-board technology. The electrical and the optical ports are designed for hot plugging.

2 High speed PIN detector array

The photo detector is a GaAs-based 1×12 PIN array. The dimensions of the PD array are 3400μm in length, 600μm in width, and 200μm in thickness. The diameter of the sensitive area is 80μm. A multimode fiber with a 62.5μm core can

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be easily aligned with the PD array. The distance between the wire bond pads and the sensitive area is extended to 500μm in order to facilitate coupling and bonding.

The average responsivity of the PDs at a wavelength of 850nm is 0. 55W/ A. Under a 10V reverse voltage ,the typical dark current is less than 0. 01nA ,as shown in Fig. 1(b) . The capacitances of the PDs are lower than 0. 5pF. The rise and fall times are less than 80ps. The bandwidth of the PDs can reach 5 GHz.

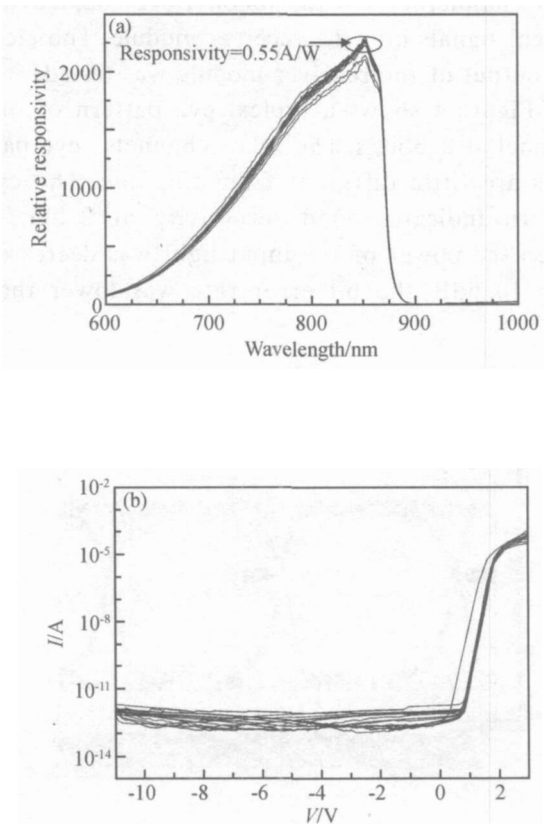

Fig. 1 Opto-electric characteristic of PD array (a) Relative responsivity versus wavelength ; (b) *I-V* curves

3 Optical receiver IC

The optical receiver integrated circuit (IC) was made with standard CMOS technology. It contains twelve amplifier channels ,each of which contains two kinds of amplifiers. The first stage is a trans-impedance amplifier and the second stage is a limiting amplifier. The trans-impedance amplifier with an input capacitance up to 600fF (the intrinsic capacitance of the photo-detector) achieves a - 3dB bandwidth greater than 2. 9 GHz. The limiting amplifier provides a differential CML (current mode logic) output that can be used to drive CML-compatible data or a clock recovery circuit. The sensitivity of the amplifiers can reach 8μA with a 10^{-12} bit error rate. This amplifier design satisfies the sensitivity and bit rate requirements at 2. 5 Gbit/ s.

The receiver IC is supplied by a 3. 3V power , which provides a reverse voltage for each photo detector. To facilitate the wire bonding ,the signal-input pads on the IC chip are spatially arranged in the same way as those on the PDs.

4 Alignment of PD array

A 1 ×12 ribbon fiber with a standard MT connector was used to couple light into the PD array , which was mounted between two pins on a substrate with a device called a pin-holder. The two pins were designed to precisely orient the MT connector and were plugged into a pair of holes on the MT connector. In this way ,light can be coupled into the PD array as long as its sensitive area is aligned with the ribbon fiber ,just like a socket to a plug. For this purpose ,the position of the PD array between the two pins is important ,as it determines the success of the coupling. We designed an approach to guarantee that the PD array is placed in the right position.

First , an alignment mold with holes corresponding to the pins and orientation markings for alignment was precisely fabricated with an electric discharge process. The PD array and the alignment mold were then aligned face-to-face on a flip chip machine. The machine can achieve an alignment precision of 1μm. This precision is high enough to couple a multi-fiber to an 80μm-wide sensitive area. Next , the PD array and the mold were joined with solder at 150 ℃. After these operations , the desired alignment was achieved. The next step was to transfer the PD array from the mold to the pin-holder. The mold with the PD array soldered to it was connected to the pin-holder by inserting the pins into the holes. Because the mold has the same hole positions and precise dimensions as those of the MT connector ,the PD array was then located in the right position between the pins on the pin-holder. After the PD array was fixed with glue ,the mold was heated and taken off. At this point , an optical port , which can be hot-plugged , has been finished. To couple light into PD array , one can

simply plug a fiber ribbon with an MT connector to the pins, as shown in Fig. 2.

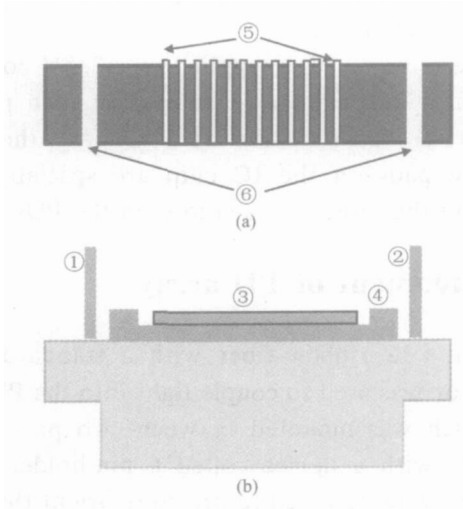

Fig. 2 Schematic of alignment for PD array and 1 ×12 ribbon fiber with MT connector (a) 1 ×12 ribbon fiber with MT connector; (b) Pin-holder ①and ②Alignment pins; ③PD array; ④Protective base; ⑤Multi fibers; ⑥Alignment holes

5 Receiver module assembling and packaging

Chip-on-board (COB) technology is a kind of technology that can provide simple packaging for dies. We adopted it here to package the receiver module. First, the receiver IC was glued to the high-speed PCB. The glue was then solidified by heating. Next, the PCB with the glued-on IC and the pin-holder with the attached PD were assembled into a metallic case. The pads of the IC and the PD array must be adjusted to be on the same plane. Then, gold wire was bonded to connect the circuit in the module. After this, special glue was injected into the case to protect the chips and the connecting wires. Finally, the case was covered and sealed with solder. An optical window was left on the cover to provide an access for the ribbon fiber with the MT connector. A completed receiver module is shown in Fig. 3.

6 Test results

The receptivity and characteristics of the receiver module were tested with a commercial 1 ×12 parallel optical transmitter module. Each channel of

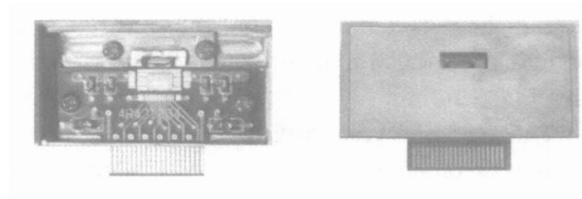

Fig. 3 Completed receiver module

the transmitter can achieve 2.5bit/s. A stream of 2^{23} bits with pseudo-random sequences rate was sent at 2.5bit/s by the transmitter into each channel. A 1 ×12 ribbon fiber coupled the optical signals into the receiver module. The electric output of the receiver module was tested.

Figure 4 shows a typical eye pattern of one channel at 2.5bit/s. The other channels' eye patterns are little different from this one. The eye pattern indicates good receptivity at 2.5bit/s. When the power of the input light was decreased to -13.6dB, the bit error rate was lower than 10^{-13}.

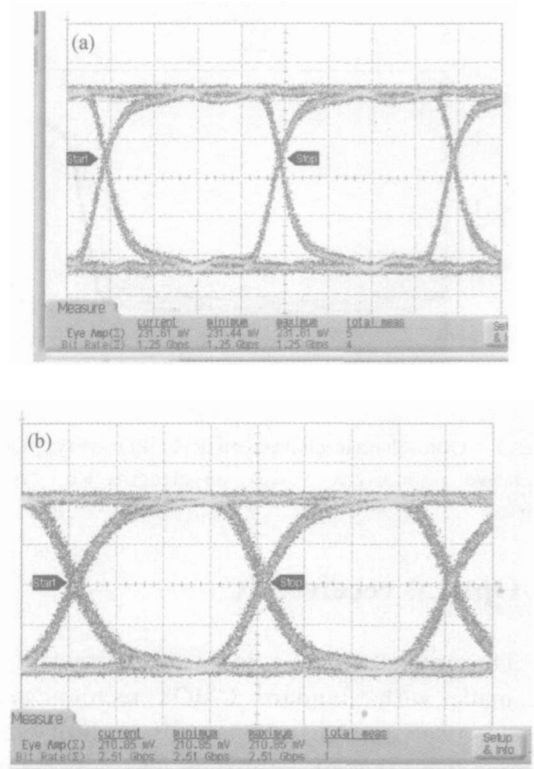

Fig. 4 Typical channel eye pattern for 23bit PBS (a) 1.25Gbit/s; (b) 2.5Gbit/s

7 Conclusion

We have developed a parallel optical receiver module with 12 channels using COB technology. Both the parallel electrical ports and the parallel optical ports support hot-plugging. The receptivity

of the module can reach 30 Gbit/s when each channel is working at 2.5 Gbit/s. The sensitivity of the module is -13.6dBm for 10^{-13} BER.

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30 Gbit/s 并行光接收模块*

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摘要: 报道了一种基于 CMOS 工艺接收电路芯片和 GaAs 工艺 1×12 光电探测器阵列的 30 Gbit/s 并行光接收模块. 该模块采用并行光通信方案, 利用中高速光电子器件实现信号的高速传输. 直接使用未经封装的接收电路裸片和光探测器裸片, 采用电路板上芯片技术封装制作模块, 并通过倒装焊的方式实现了探测器阵列与列阵光纤的精确对准并形成了可插拔的光接口. 测试结果表明模块的接收能力可以达到 30 Gbit/s. 误码率小于 10^{-13} 时, 接收模块的灵敏度可以达到 -13.6dBm.

关键词: 接收模块; 并行; 探测器阵列

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