Sub-1V CMOS Voltage Reference Based on Weighted V_{gs}

Zhang Xun†, Wang Peng, and Jin Dongming

(*Institute of Microelectronics, Tsinghua University, Beijing* 100084, *China*)

Abstract: We propose a voltage reference based on the weighted difference between the gate-source voltages of an nMOS and a pMOS operating in their saturation regions. No diodes or parasitic bipolar transistors are used. The circuit is simulated and fabricated with SMIC 0.18μm mixed-signal technology, and our measurements demonstrate that its temperature coefficient is 44ppm/ °C and its PSRR is -46dB. It works well when V_{dd} is above 650mV. The active area of the circuit is about 0.05mm^2.

Key words: voltage reference; temperature coefficient; power supply rejection ratio
EEACC: 1205; 2560; 2570D
CLC number: TN432 **Document code:** A **Article ID:** 0253-4177(2006)05-0774-04

1 Introduction

The usage of portable devices such as mobile phones is rapidly spreading all over the world. Some simple self-biasing circuits such as voltage references are widely used in these battery-operated devices. In the past, voltage references have usually consisted of bandgap references, which can be implemented using parasitic vertical BJTs in standard CMOS technology[1,2]. However, the parasitic bipolar transistor in a CMOS process is usually not very well characterized, and the power efficiency is not sufficient for low-power operations due to the large dropout voltage. It is expected that the whole system will be able to operate on a single 1V supply in the near future.

In this paper, a sub-1V voltage reference in standard CMOS technology based on the weighted gate-source voltage difference between an nMOS and a pMOS is presented. The design techniques for achieving good performance are also presented in detail.

2 Structure and principles of the sub-1V CMOS voltage reference

The proposed voltage reference is shown in Fig. 1. It is based on the circuit first proposed in Ref. [3] and is composed of a start-up circuit, a low-voltage bias circuit, and a reference core circuit.

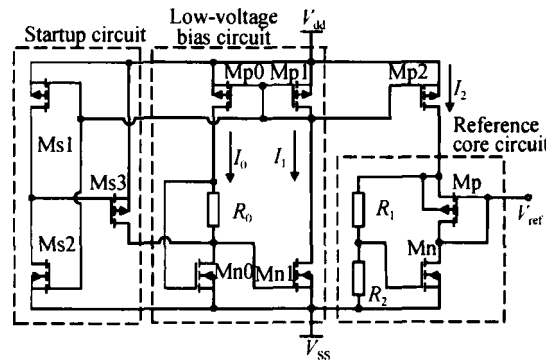

Fig. 1 Sub-1V CMOS voltage reference circuit

Unlike the one in Ref. [3], this new voltage reference uses the sub-threshold region of the MOSFET to generate a current for the reference core circuit, which can lower the supply voltage and power consumption. The combination of high resistance poly (HRP) and n-well resistors cancels the temperature coefficient (TC) of the resistor R_0 in the bias circuit.

The square law equation for MOSFETs in the saturation region is

$$I_d = \frac{\mu C_{ox}}{2} \times \frac{W}{L} (V_{GS} - V_T)^2$$

where the threshold voltage V_T and the mobility μ are temperature dependent and are given by Eqs. (2) and (3)[4~6],

$$V_T(T) = V_T(T_0) - \beta_{V_T}(T - T_0) \quad (2)$$

$$\mu(T) = \mu(T_0) \times \left(\frac{T}{T_0}\right)^{-\beta_\mu} \quad (3)$$

† Corresponding author. Email: zhangxun97@mails.tsinghua.edu.cn
Received 29 October 2005, revised manuscript received 24 January

where β_{VT} and β_{μ} are technology-dependent constants and T_0 is room temperature. From the circuit, the reference voltage is

$$V_{ref} = (1 + \frac{R_1}{R_2}) V_{GSn} - | V_{GSp} |$$
$$= \left[(1 + \frac{R_1}{R_2}) V_{Tn} - | V_{Tp} | \right] +$$
$$\sqrt{\frac{2 I_n}{C_{ox}}} \times \left[\left(1 + \frac{R_1}{R_2} \right) \times \sqrt{\frac{1}{\mu_n (\frac{W}{L})_n}} - \sqrt{\frac{1}{\mu_p (\frac{W}{L})_p}} \right] \quad (4)$$

where V_{GSn} and V_{GSp} are the gate-source voltages of Mp and Mn in Fig. 1, and

$$I_n = I_2 - V_{GSn} / R_2 \quad (5)$$

Reference [3] replaces I_n with I_2 and neglects the current through R_1 and R_2, which results in an error of almost 10 % when R_1 and R_2 are 1MΩ.

In order to get zero TC, the source-bulk voltage of Mp is set to zero to eliminate the body effect and improve the power-supply rejection ratio (PSRR). Moreover, long-channel devices are chosen to minimize the channel-length modulation effect.

In Fig. 1, R_0, Mn0, and Mn1 compose a MOS peaking circuit mirror diagram when operating in the sub-threshold region[7]. The drain current of the MOSFET in the sub-threshold region is determined by the equation[8,9]

$$I_D = \mu C_{ox} \frac{W}{L} N U_T^2 \exp[\frac{1}{N U_T} (V_{GS} - V_{on})] \times$$
$$[1 - \exp(-\frac{V_{DS}}{U_T})] \quad (6)$$

where $N = 1 + C_D / C_{ox}$, $U_T = kT/q$, and $V_{on} = V_T + NU_T$.

If the drain-source voltage $V_{DS} \geq 3U_T$, the formula can be simplified to

$$V_{GS} = N U_T \ln(\frac{I_D}{I_{ES}} \times \frac{1}{W/L}) \quad (7)$$

where $I_{ES} = \mu C_{ox} N U_T^2 \exp(-\frac{V_{on}}{N U_T})$ is a process-dependent parameter.

For

$$V_{GS0} = V_{GS1} + I_0 R_0 \quad (8)$$

if $I_0 = I_1$, then

$$I_0 = \frac{N U_T}{R_0} \ln \frac{(W/L)_1}{(W/L)_0} \quad (9)$$

Equation (9) can be thought of as a proportional to absolute temperature (PTAT) structure if the TC of R_0 is neglected. This is also power supply independent if the channel-length modulation is neglected.

If $I_2 = M I_0$, then from Eqs. (1) and (5) we get

$$\sqrt{I_n} = \frac{-\sqrt{\frac{2}{\mu_n C_{ox} (\frac{W}{L})_n}} + \sqrt{\frac{2}{\mu_n C_{ox} (\frac{W}{L})_n} + 4 R_2 (M I_0 R_2 - V_{Tn})}}{2 R_2} \quad (10)$$

Finally, the temperature dependence of the reference voltage can be obtained by differentiating Eq. (4) with respect to the temperature, and is given by

$$\frac{\partial V_{ref}}{\partial T} = [-(1 + \frac{R_1}{R_2}) \beta_{VTn} + \beta_{VTp}] +$$
$$\frac{\beta_{\mu p} + 1}{T_0} \sqrt{\frac{I_n (T_0)}{2 \mu_p (T_0) C_{ox} (\frac{W}{L})_p}} \times$$
$$[(1 + \frac{R_1}{R_2}) \times \sqrt{\frac{\mu_p (T_0) (\frac{W}{L})_p}{\mu_n (T_0) (\frac{W}{L})_n}} \times \frac{\beta_{\mu n} + 1}{\beta_{\mu p} + 1} \times$$
$$(\frac{T}{T_0})^{\frac{\beta_{\mu n} - 1}{2}} - (\frac{T}{T_0})^{\frac{\beta_{\mu p} - 1}{2}}] \quad (11)$$

To obtain $(\partial V_{ref} / \partial T) |_{T = T_r} = 0$, the linear and nonlinear terms are set to zero by the resistor ratio and transistor size ratio, which are given by

$$\frac{R_1}{R_2} = \frac{\beta_{VTp}}{\beta_{VTn}} - 1 \quad (12)$$

$$\frac{(\frac{W}{L})_p}{(\frac{W}{L})_n} = \frac{\mu_n (T_0)}{\mu_p (T_0)} \times (\frac{T_r}{T_0})^{\beta_{\mu p} - \beta_{\mu n}} \times \frac{\beta_{\mu n} + 1}{\beta_{\mu p} + 1} \quad (13)$$

Equations (12) and (13) show that the TC can be optimized by varying the circuit parameters instead of by refining the process parameters. Optimization can be done on the circuit design level and by on-chip trimming.

In order to cancel the TC of resistor R_0 in the bias circuit, mixed-resistor technology is applied, which combines two resistors, an HRP and n-well, into one that has a different direction TC. In SMIC 0.18μm technology, this can reduce the resistor's TC from 7.5 % to 0.5 %.

However, if the bias current I_2 decreases, Mp and Mn may leave the saturation region and enter the triode region. Thus, the minimum supply voltage must be maintained in order to prevent the current source Mp2 from being forced to operate in the triode region, which means that V_{dd} must be larger than $(1 + R_1 / R_2) V_{GSn} + V_{ov}$ or $V_{Tp} + 2V_{ov} + V_{ref}$, which is about 650mV here in the SMIC 0.18μm process.

3 Simulation, measurement, and layout

Figure 2 shows the simulation and measurement results of the output voltage V_{ref} at different temperatures and power supplies. SMIC 0.18μm technology is used here. The simulation results demonstrate that when the temperature changes from 0 to 100 ℃, TC (V_{ref}) is about 32ppm/ ℃. When V_{dd} > 650mV, the circuit provides a stable reference voltage, and the PSRR is - 51dB. For comparison with the simulation result, the measured TC is 58ppm/ ℃ in the temperature range of 10 ～ 110 ℃ and 44ppm/ ℃ in the range of 10 ～ 96 ℃. It also can be thought of as start-up when V_{dd} is above 650mV, and the PSRR is - 46dB.

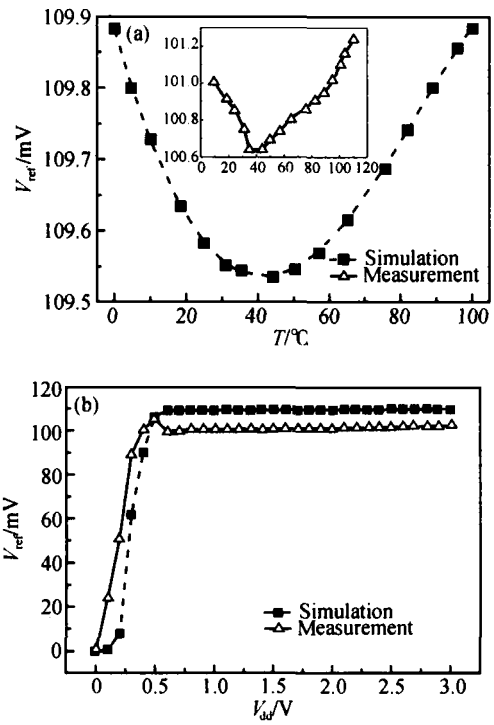

Fig. 2 Simulation and measurement results of sub-1V CMOS voltage reference (a) Reference voltage versus temperature; (b) Reference voltage versus power supply

Since the temperature dependence of the threshold voltage is not perfectly linear and a complete cancellation of the temperature dependence of μ_p, μ_n, and R_0 is not possible in the whole temperature range, a nonlinear temperature-dependent error voltage appears at the reference output voltage.

Repeating the measurements for different chips at a 1V supply voltage demonstrates that the output voltage V_{ref} is between 97.14 and 100.75mV, implying less than 4% relative error. The power consumption is only 12μA. Figure 3 shows the layout of the proposed voltage reference circuit, which is fabricated in SMIC 0.18μm technology. The chip area is about 0.05mm^2.

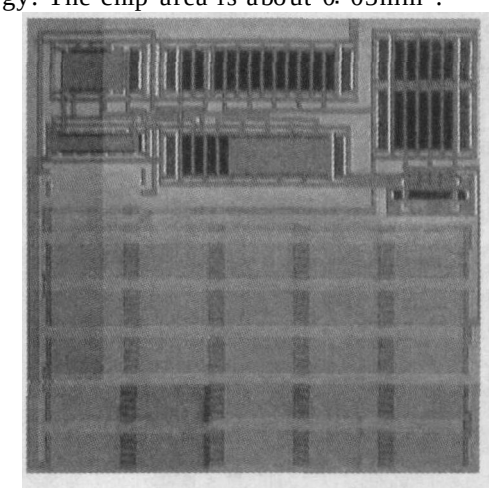

Fig. 3 Layout of sub-1V CMOS voltage reference

Table 1 gives a comparison to voltage references reported from 2002 to 2005.

Table 1 Comparison of voltage reference

Technique	Min V_{dd}/ V	Supply current/μA	TC/ 10^{-5} ℃$^{-1}$	PSRR/ dB	Technology/μm	Area/ mm^2	Year
BVR[2] *1	0.98	18	1.5	NA	0.6	0.24	2002
CMOS[3] *2	1.4	9.7	3.69	- 47	0.6	0.055	2003
BVR[10] *3	3	NA	2.5	NA	0.35	0.13	2004
BVR[11]	0.97	NA	3.6	NA	0.35	NA	2005
CMOS	0.65	12	4.4	- 46	0.18	0.05	This paper

*1 Bandgap voltage reference; *2 CMOS voltage reference; *3 Simulation only

4 Conclusion

A sub-1V CMOS voltage reference that uses the temperature dependence of pMOS and nMOS gate-source voltages is described.

Simulated results using a SMIC 0.18μm CMOS process reveal that this circuit works pro-

perly at a voltage as low as about 650mV and has excellent stability when the supply voltage varies from 0.65 to 3V. Since the circuits work in the sub-threshold region, the supply current is only 12μA. The temperature coefficient is 44ppm/ ℃ and the PSRR is - 46dB. The active area of the chip is about 0.05mm^2.

References

[1] Song B S, Gray P R. A precision curvature-compensated CMOS bandgap reference. IEEE J Solid-State Circuits, 1983, SC-18: 634

[2] Leung K N, Mok P K T. A sub-1V 15-ppm/ ℃ CMOS bandgap voltage reference without requiring low threshold voltage device. IEEE J Solid-State Circuits, 2002, 37: 526

[3] Leung K N, Mok P K T. A CMOS voltage reference based on weighted ΔV_{GS} for CMOS low-dropout linear regulators. IEEE J Solid-State Circuits, 2003, 38(1): 146

[4] Tsividis Y P. Operation and modeling of the MOS transistor. New York: McGraw-Hill, 1987

[5] Sze S M. Physics of semiconductor devices. 2 nd ed. New York: Wiley, 1981

[6] Klaassen F M, Hes W. On the temperature coefficient of the MOSFET threshold voltage. Solid State Electron, 1986, 29: 787

[7] Hunter L P. Handbook of semiconductor electronics. New York: McGraw-Hill, 1970: 10

[8] Gray P R, Hurst P J, Lewis S H, et al. Analysis and design of analog integrated circuits. 4th ed. New York: John Wiley & Sons, 2001

[9] Vittoz E, Fellrath J. CMOS analog integrated circuits based on weak inversion operation. IEEE J Solid-State Circuits, 1977, SC-12(3): 224

[10] Zhu Zhangming, Yang Yintang, Liu Lianxi, et al. Super performance CMOS bandgap voltage reference. Chinese Journal of Semiconductors, 2004, 25(5): 542

[11] Sheng Jinggang, Chen Zhiliang, Shi Bingxue. A CMOS bandgap reference with 1V supply. Chinese Journal of Semiconductors, 2005, 26(4): 826

1V以下基于 V_{gs} 权重的 CMOS 恒压源

张　洵†　王　鹏　靳东明

(清华大学微电子学研究所，北京　100084)

摘要：提出了一种新型 CMOS 恒压源的制作方案，它基于 nMOS 和 pMOS 的饱和区栅源电压随温度变化权重不同的原理，将两者做相关运算，得到零温度系数的恒压源. 该电压源没有采用二极管和寄生三极管，并用 SMIC 0.18μm 数模混合工艺模型参数仿真并制造. 测试结果表明，温度系数达到了 44ppm/ ℃，PSRR 为 - 46dB，650mV 以上的电源电压就可以完全正常工作. 芯片面积约为 0.05mm^2.

关键词：恒压源；温度系数；电源电压抑制比

EEACC：1205；2560；2570D

中图分类号：TN432　　**文献标识码**：A　　**文章编号**：0253-4177(2006)05-0774-04

† **通信作者**. Email: zhangxun97@mails.tsinghua.edu.cn

2005-10-29 **收到**，2006-01-24 **定稿**